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A Study of Gate Length and Source-Drain Bias on Electron Transport Properties in SiC Based MOSFETs Using Monte Carlo Method

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Abstract

Ensemble Monte Carlo simulations have been carried out to investigate the effects of Gate length and different source-drain bias on the characteristics of wurtzite SiC MOSFETs. Electronic states within the conduction band valleys are represented by non-parabolic ellipsoidal valleys centred on important symmetry points of the Brillouin zone. The following scattering mechanisims, i.e, impurity, polar optical phonon, acoustic phonon, alloy and piezoelectric are inculded in the calculation. Ionized imurity scattering has been treated beyound the Born approximation using the phase-shift analysis. Two transistors with gate lengths of 200 and 400 nm are simulated. Simulations show that with a fixed channel length, when the gate length is decreased, the output drain current is increased, and therefore the transistor transconductance increases. Moreover, with increasing temperature the drain current is reduced, which results in the reduced drain barrier lowering. The simulated device geometries and doping are matched to the nominal parameters described for the experimental structures as closely as possible, and the predicted drain current and other electrical characteristics for the simulated device show much closer agreement with the available experimental data.

Keywords*: Ensemble Monte Carlo, channel length, transconductance, Brillouin zone.*

1. Introduction

Wide bandgap SiC has two main uses in commercial devices, providing bright LEDs emitting at ultraviolet-blue green wavelengths for CD-ROM and sensor applications and heterojunction field effect transistors (HFETs) which can sustain high current densities at elevated temperatures [1-3]. It has been shown that SiC has large peak electron velocity and can be an important candidate for high frequency application. A wide energy bandgap leads to a low intrinsic carrier concentration, which enables a more precise control of free carrier concentration over a wide range of carrier concentration over a wide range of temperatures, and hence the devices made of this kind of material will be operable at high temperatures with large breakdown voltage. The development of SiC based transport devices is hampered by the nonavailability of detailed knowledge of the transport properties and transport parameter. Keeping in mind its huge technological prospect, we need a better understanding of these materials. The MOSFET transistor is one of the most favored devices in the construction of large scale integrated circuits because of its simplicity of construction, the comparative lack of doping diffusion problems and the resultant high packing densities possible [1-5]. Whilst the preferred semiconductor is still silicon, industry is now tooling up for wide band gap semiconductor like SiC production, which offers high electron mobility and hence the prospect of greater frequency operating rates. Its direct bandgap furthermore allows easier integration with optical devices. For this reason SiC MESFETs have received much attention in the literature, particularly with respect to their simulation in an attempt to understand the basic principles of their operation. SiC offers the prospect of mobility comparable to other group III-V materials and is increasingly being developed for the construction of optical switches. Other authors have also pointed out the potential importance of SiC and a few simple devices have been simulated. The MOSFET transistors have been found to be more effective than ordinary transistors made from the semiconductor materials [6-8]. In MOSFETs the forming layer of the transistor channel is very thin and the sub-base current is also zero because of their insulation. Hence, carriers are closer to the gate, so the gate will have a greater control over the channel current. In this transistor, the effect of drain voltage on threshold voltage is less than in comparison with other devices [9-10].

In this study, two thin transistors were investigated. The channel length was held constant, but the gate length covers part or all of the channel length. Then by holding the channel length constant, the effect of the change of the gate length on the characteristics of the transistor was studied. It has been indicated that in nano transistors made with carbonic nano pipes if the gate connection does not cover a part of the channel, some characteristics of the transistor will improve [14]. In this study, a nano transistor made of SiC was used. Stimulation for two transistors with gate lengths of 200, 400 nm were carried out. This article is organized as follows. Details of the simulation methods are presented in section 2, and the results of the change in gate length on the gate current-voltage curve with regard to different drain voltages, and the comparison of threshold voltage are presented in section 3.

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2. Research Method

An ensamble Monte Carlo simulation have been carried out to simulate the electron transport properties in SiC MOSFET. The method simulate the motion of charge carriers through the device by following the progress of 10^4 super particles. These particles are propagated classically between collisions according to their velocity, effective mass and the prevailing field. The selection of the propagation time, scattering mechanism and other related quantities is achieved by generating random numbers and using this numbers to select, for example, a scattering mechanism. Our self-consistent Monte Carlo simulation was performed using an analytical band structure model consisting of five non-parabolic ellipsoidal valleys. The scattering mechanisms considered in the model are acoustic, polar optical, ionized impurity, piezoelectric and nonequivalent intervalley scattering. The nonequivalent intervalley scattering is between the Γ_1, Γ_3, U, M and K. The device structure characteristics is as follows. The overall device length is 6 µm in the x -direction and the device has a 200 or 400 nm gate length. The source and drain have ohmic contacts and gate is in Shottky contact in 1 eV to reperesent the contact potential at the Au/Pt. The source and drain regions are doped to 5×10^{23} m^{-3} and the top and down bu.er layers are doped to 2×10^{23} m^{-3} and 1×10^{22} m^{-3}, respectively.

The effective source to gate and gate to darin separation are 0.1 µm. The large dimensions of the device need to a long simulation times to ensure convergence of the simulator. The device is simulated at room temperature.

3. Results and Analysis

The electric field in the device as a function of position is shown in figure 1 for source-drain voltages between 0 and 5 V. It is apparent from this figure and from figure 2 that essentially all the potential is dropped in the under the gate. However, as a result of the inhomogeneous space charge the field does vary substantially with position, reaching a maximum magnitude near the drain.

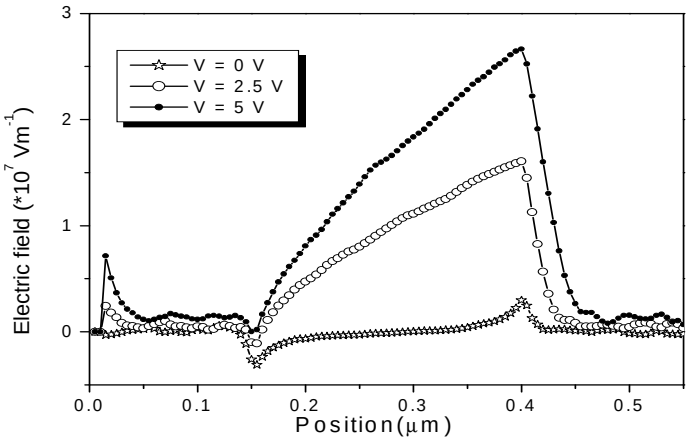

Figure 1. The electric field in the simulated SiC MOSFET for source-drain voltages between 0 and 5 V at room temperature.

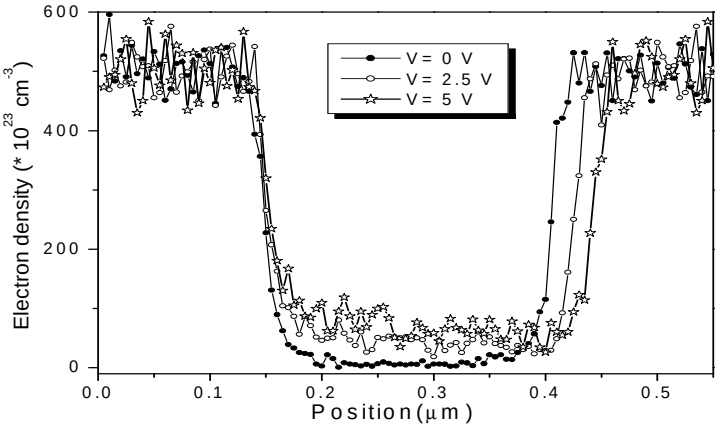

Figure 2. Electron density as a function of position in the model SiC MOSFET at room temperature for different source-drain voltages.

Figures 2 and 3 show some features of the state of the device at room temperatures when the applied voltage is up to 5 volts. The free electron concentration through the device is plotted in figure 2. The electrons diffuse from the source into the buffer layer and are accelerated towards the drain by the field. The resulting space charge causes the departure from a uniform electric field clearly apparent in figure 3. Figure 3 shows that the average drift velocity in the active layer has a maximum value of about 2.3×10^5 ms^{-1} at 300 K.

The effect of gate length on electron transport in SiC based MOSFETs with 200 and 400 nm gate lengths has been illustrated in figure 4. This figure shows drain current versus drain-source voltage for different gate lengths. It is apparent from this figure that higher velocities are reached as the gate length is reduced as a result of the increase in longitudinal electric field and velocity overshoot effects. It follows that the electron transit time under the gate is reduced in two ways; there is a reduction in the transit length and also the electron velocity is larger. The high value of the field at the source-end of the gate is responsible for the almost ballistic acceleration of the electrons as soon as they enter the channel region under the gate.

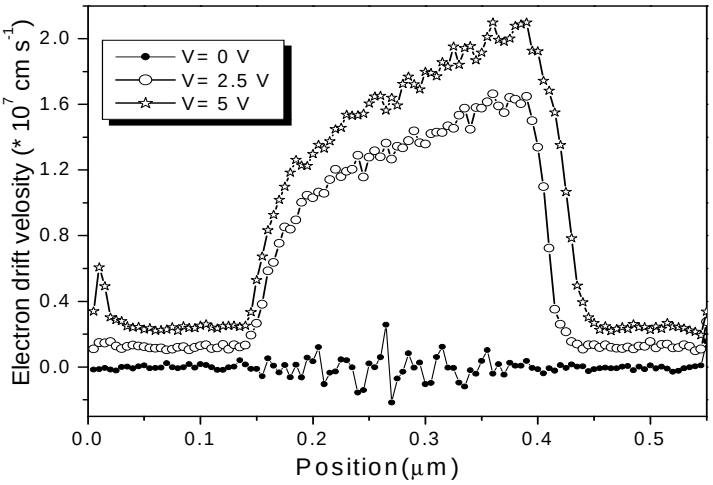

Figure 3. Electron drift velocity as a function of position in the model SiC MOSFET at room temperature for different source-drain voltages.

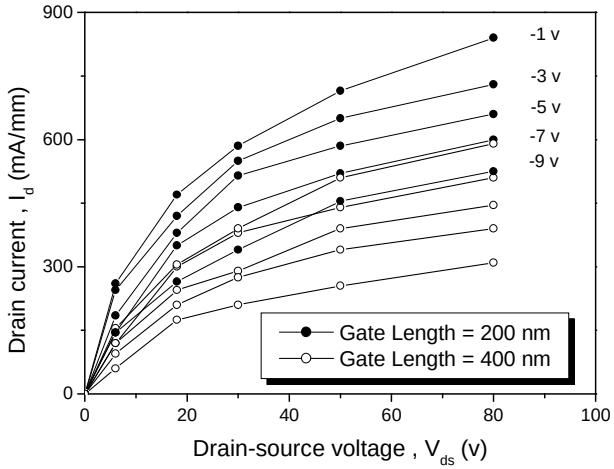

Figure 4. The effect of gate length on the electrical characteristics of SiC MOSFET. I-V characteristics for gate lengths of 200 and 400 nm has been illustrated.

4. Conclusion

The effect of gate length on electron transport in SiC MOSFETs has been studied. The I-V characteristics show that higher velocities are reached as the gate length is reduced as a result of the increase in longitudinal electric field and velocity overshoot effects.

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