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Experimental Validation of Shared Inverter Topology to Drive Multi AC-Loads

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ABSTRACT

Many reduced-switch-count (RSC) inverter topologies have been proposed in the literature. As the number of switches required to produce a set of voltages in RSC inverters are less than that in conventional inverter, as a result utilizing RSC inverters in a certain system reduces its size and cost. In this paper, a novel RSC shared inverter topology consisting of fifteen switches and capable of driving four three-phase AC-loads independently is proposed and experimentally verified. A carrier-based pulse width modulation (PWM) technique that employs the zero-sequence-signal injection principle is developed to drive the proposed inverter along with adequate DC voltage bus utilization between the shared loads for common frequency (CF) as well as different frequency (DF) modes. The structure and the principle of operation of the proposed inverter are introduced and intensively verified using simulation and field-programmable-gate-array (FPGA)-in-the-loop simulation under linear and nonlinear loads. Then, Inverter prototype was built and the proposed inverter has been verified experimentally. The experimental results verify the applicability of the proposed inverter and the employed PWM.

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1. INTRODUCTION

Many electrical systems involve more than one load that requires independent control. The conventional solution for such a problem is to use a single conventional six-switch inverter (CSSI) for each load. Using separate inverters increases the volume and the cost of the system. Another solution to the problem is to use multi−output reduced-switch-count inverters. One of the mostly used inverters for that is the five leg inverter (FLI) that was introduced in [1]. The FLI consists of ten switches distributed on five legs, two switches per leg. In the FLI one leg will be shared between the two loads. The FLI reduces the number of switches needed to drive two three-phase loads from twelve in conventional inverters to ten. The FLI is widely employed in motor drives [2-6]. The authors in [2] employed the FLI to supply two three phase induction motors. The authors in [3] used the FLI to drive one motor and one two-phase compressor motor. Hence, this arrangement eliminated the need of the split dc capacitors for the compressor motor. In [4], the authors proposed a model predictive controller (MPC) to drive two permanent magnet synchronous motors (PMSMs) using FLI. A dual hysteresis current-control (DHCC) method was employed in [5] to independently drive two PMSMs. In [7], a control of dual-PMSM using space vector PWM has been presented.

Another multi-output inverter that is widely used in the RSC topologies field is the nine-switch inverter (NSI) that was introduced in [8]. The NSI consists of nine switches distributed on three legs, three switches per leg. The NSI encapsulates two inverters, the upper and the middle switches form the first inverter, while the middle and the lower switches form the second inverter. The authors in [9] presented dual transformerless hybrid filter for power level applications based on the concept of NSI. Two passive LC-filters are linked with two ac outputs of the converter. A phase-shift carrier-based space vector modulation technique for the NSI was introduced by the authors in [10].This technique minimizes the effect of the crossover between the upper and the lower modulation signals that causes distortion in current and voltage waveforms.

A lot of works are done to reduce the number of switching per period and hence the switching losses of the NSI [11-15]. The authors in [11] presented a systematic approach that gives the ability to choose any PWM technique. The proposed generalized PWM strategy reduces the power losses by reducing the total number of switching in each switching cycle, and clamping the output voltage when the corresponding output current is at its peak as that avoids high switching losses. The authors in [12] introduced a space vector modulation (SVM) [16] technique for the NSI that also reduces the total number of switches in each switching cycle. SVM technique was developed to reduce the total harmonic distortion (THD) [17]. In [13], the authors presented an optimal PWM technique for the NSI with the objective of minimizing the switching losses. Both common frequency (CF) and different frequencies (DF) modes were investigated. In [14], the authors presented a systematic and straight generalized scalar PWM to reduce switching losses of NSI with a specific distribution parameter that reduces the number of switchings. The concept of NSI is also applied in power system application as active power filter in [15] to reduce size, cost, and weight of grid-tie converters. The authors in [18] investigated the current stresses on the switches of the NSI. In [19], the authors proposed a nine-switch converter for AC/AC conversion as a replacement for the conventional back-to-back (B2B) converter. The authors developed a carrier-based PWM scheme for both constant frequency (CF) and variable frequency (VF) modes. The aforementioned solutions are capable of driving two three-phase loads independently. To drive four three-phase loads, one simply can choose either to use the classical solution which will consist of twenty-four switches, or by utilizing either two FLIs or two NSIs, one for each two loads. Which will make the total number of switches equals to twenty, eighteen, respectively. Although the extended five-leg inverter [20] principle is applicable here, it will reduce the total number of switches to be eighteen switches.

In this paper, a new inverter topology, the fifteen-switch inverter (FSI) is proposed. The FSI consists of fifteen switches and it is capable of driving four three-phase AC loads independently. This solution is far superior to the aforementioned solutions in term of the total switch count. The remaining of this paper is organized as follows: the structure and the principle of operation of the FSI are introduced in Section 2. Proof of concept of the proposed topology is provided in Section 3 by means of simulation modelling. Experimental results are introduced in Section 4 to verify the practical validity of the proposed inverter. Finally, conclusions are introduced in Section 5.

2. THE PROPOSED FIFTEEN-SWITCH INVERTER

The schematic diagram of the proposed FSI is introduced in this section along with the adapted modulation technique that is used to realize the gate pulses for the proposed inverter. To fully highlight the potential of the proposed inverter topology, all of the possible operation modes are investigated and discussed.

2.1. The Schematic Diagram of the Fifteen-Switch Inverter

The schematic diagram of the FSI is shown in Figure 1(a). The FSI consists of fifteen switches, five upper switches, five middle switches, and five lower switches. The FSI encapsulates four three-phase inverters as shown in Figure 1(b) and Table 1. One of the legs of the FSI is common to all the loads. In this paper, without loss of generality, it is assumed that phase ‘c’ of each load is connected to the common leg.

Table 1. The four inverters and their associate power switches

Inverter	Participatory switches
First inverter	SH1, SH2, SH3, SM1, SM2, and SM3
Second inverter	SH3, SH4, SH5, SM3, SM4, and SM5
Third inverter	SM1, SM2, SM3, SL1, SL2, and SL3
Fourth inverter	SM3, SM4, SM5, SL3, SL4, and SL5

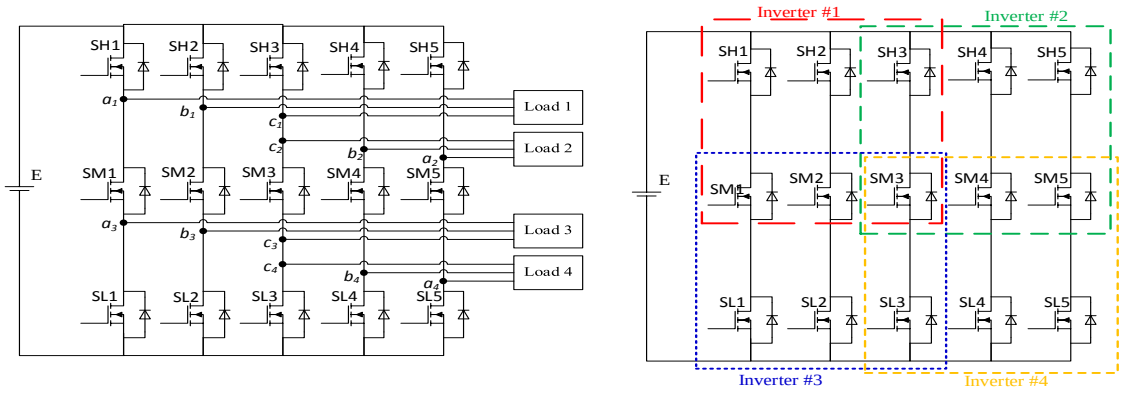

Figure 1. The proposed fifteen-switch inverter, (a) the schematic diagram, (b) the inverters encapsulated in the FSI

2.2. Modulation Technique

A carrier-based PWM technique with zero-sequence injection is adapted to drive the FSI and achieve independent control of each of the four loads of the proposed inverter. The zero-sequence injection improves the voltage utilization and reduces the current ripple [21]. The block diagram of the proposed technique is shown in Figure 2.

Let the voltage references (for $i=1,2,3,4$) of the four loads be given as follows:

$$\begin{aligned} v_{ai}(t) &= A_i \cos(2\pi f_i t + \theta_i) \\ v_{bi}(t) &= A_i \cos(2\pi f_i t + \theta_i - 2\pi/3) \\ v_{ci}(t) &= A_i \cos(2\pi f_i t + \theta_i + 2\pi/3) \end{aligned} \quad (1)$$

where f_1, f_2, f_3, and f_4 are the power frequencies; A_1, A_2, A_3, and A_4 are the amplitudes; and θ_1, θ_2, θ_3, and θ_4 are phase shifts.

For $i=1,2,3,4$, the voltage references are first added up in a manner shown in (2) to extract the zero-sequence component of the signals, and the extracted zero-sequence signal is injected back to the voltage references to come up with a new set of references as shown in (3).

$$v_{zsi} = -\frac{1}{2}\left[\max(v_{ai}, v_{bi}, v_{ci}) + \min(v_{ai}, v_{bi}, v_{ci})\right] \quad (2)$$

$$\begin{aligned} v_{ia} &= v_{ai} + v_{zsi} \\ v_{ib} &= v_{bi} + v_{zsi} \\ v_{ic} &= v_{ci} + v_{zsi} \end{aligned} \quad (3)$$

From those references, the following ten modulation signals shown in (4) can be extracted:

$$\begin{aligned} m_1 &= \frac{k\times(v_{1a}+v_{2c})}{E} + \alpha; & m_6 &= \frac{k\times(v_{3a}+v_{4c})}{E} + \beta \\ m_2 &= \frac{k\times(v_{1b}+v_{2c})}{E} + \alpha; & m_7 &= \frac{k\times(v_{3b}+v_{4c})}{E} + \beta \\ m_3 &= \frac{k\times(v_{1c}+v_{2c})}{E} + \alpha; & m_8 &= \frac{k\times(v_{3c}+v_{4c})}{E} + \beta \\ m_4 &= \frac{k\times(v_{2a}+v_{1c})}{E} + \alpha; & m_9 &= \frac{k\times(v_{4a}+v_{3c})}{E} + \beta \\ m_5 &= \frac{k\times(v_{2b}+v_{1c})}{E} + \alpha; & m_{10} &= \frac{k\times(v_{4b}+v_{3c})}{E} + \beta \end{aligned} \quad (4)$$

where E is the voltage of the DC bus, α and β are defined as shown in (5) and (6). k is a scaling factor that depends on the method of defining the voltage references.

$$\alpha = \frac{A_1 + A_2}{A_1 + A_2 + A_3 + A_4} \tag{5}$$

$$\beta = \frac{A_3 + A_4}{A_1 + A_2 + A_3 + A_4} \tag{6}$$

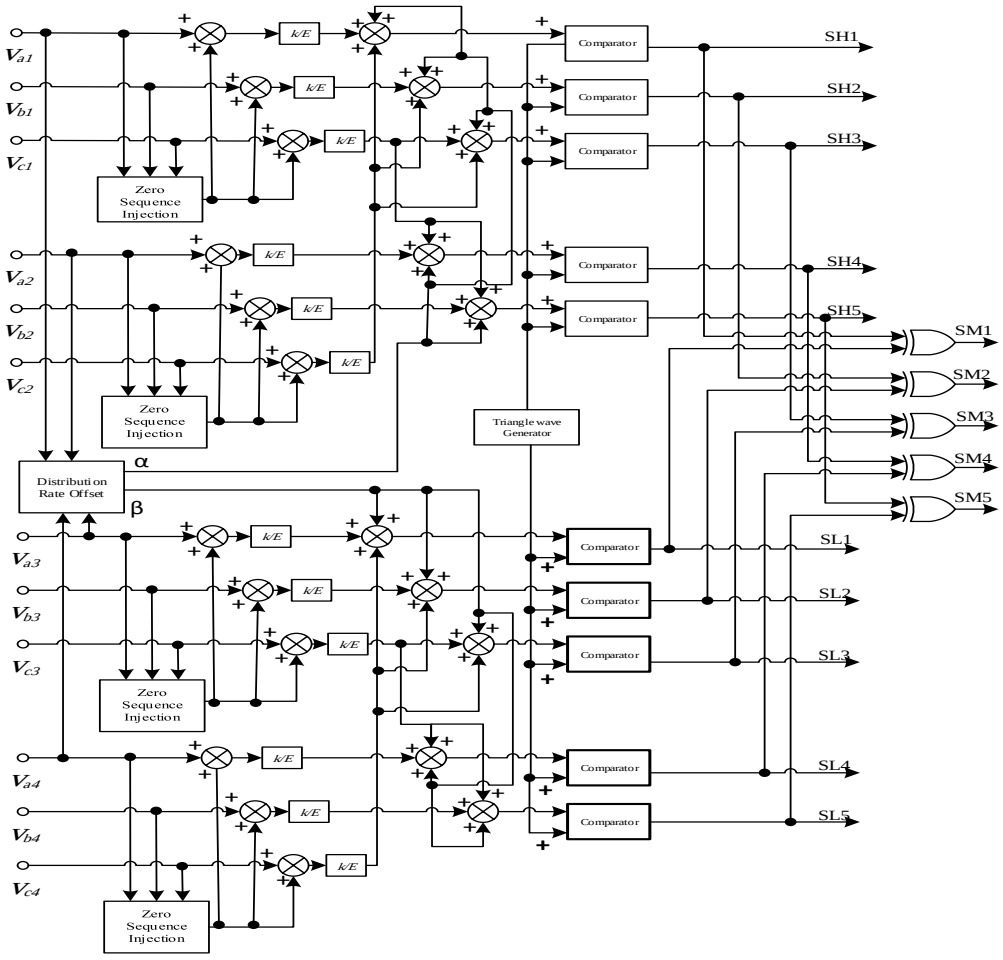

Figure 2. PWM block diagram of the FSI

It can be noticed that $\alpha + \beta = 1$, α and β are distribution rate offsets, they allow for variable voltage utilization among the loads. Using the proposed modulation technique, the DC voltage utilization can be divided unequally among the loads with only one constraint. That is, the sum of the modulation indices of the four loads doesn't exceed the maximum limit, which is 1.15 here due to the zero-sequence injection. The modulation indices of the four loads are defined as follows:

$$M_1 = \frac{k \times A_1}{E}; M_2 = \frac{k \times A_2}{E}; M_3 = \frac{k \times A_3}{E}; M_4 = \frac{k \times A_4}{E} \tag{7}$$

The first five modulation signals are used to generate the pulses of the upper switches, each of them is compared to the carrier to produce an ON pulse if it is greater than the carrier, and an OFF pulse otherwise.

The other five modulation signals are used to generate the pulses of the lower switches, each of them compared to the carrier to produce an ON pulse if it is less than the carrier. For each leg, the state of the middle switch is the output of XORing the states of the upper and the lower switches.

2.3. Operation Modes

The terms 'active inverter' and 'inactive inverter' are used to indicate the following: an active inverter is an inverter whose reference voltage is nonzero, while the inactive inverter is an inverter whose reference voltage equals to zero. '1' will be used to indicate an active inverter, while '0' will be used to indicate an inactive inverter. For example, the mode '1100' indicates that the first and the second inverters are active, and the third and the fourth inverters are inactive. According to whether an inverter is active or not, there are sixteen possible operation modes. For only one active inverter, there are four possible operation modes, which are 1000, 0100, 0010 or 0001 in which the only active inverter is the first, the second, the third or the fourth inverter, respectively. Following the same logic, the mode '1111' describes the status were the four inverters are active and '0000' is associate with the mode where the four inverters are inactive.

The topology offers similarity between the operation modes. Therefore, it is sufficient to discuss the representative modes to fully understand the principle of operation of the proposed inverter topology. From operational point of view, the modes '1110', '1101', '1011', and '0111' are similar; the modes '1100', and '0011' are similar; the modes '1010', and '0101' are similar; the modes '1001', and '0110' are similar; and the modes '1000', '0100', '0010', and '0001' are similar. Hence, only one mode in each group will be selected and discussed. Namely, the modes '1110', '1100', '1010, '1001' and '1000', beside the mode '1111'. The mode '0000' is a trivial mode where all the switches are simply OFF. Therefore, it will not be discussed.

The Operation Mode '1111': all the inverters are active. In shared inverter topologies, the key is to supply the loads one at a time while neutralizing the other loads at a high switching frequency. Understanding how inactive inverters behave gives a good understanding how loads are neutralized in this mode of operation. When a specific inverter is inactive, i.e. its voltage reference is zero, it has to behave in a manner such that the load connected to that inverter has no current flowing through it. This can be accomplished either when the load terminals are all shorted together or all are floating. To clear the picture, for the remaining operation modes, only the behaviour of the inactive inverters or associated switches will be discussed.

The Operation Mode '1110': only the fourth inverter is inactive. If switches SL3, SL4, and SL5 were all closed, then the terminals of the fourth load will be shorted together to the negative terminal of the DC source and no current will flow through the fourth load. However, switch SL3 is a part of the third inverter which is an active inverter in this operation mode. Thus, it cannot hold only one status, the ON status in this case. The topology will not work properly if such thing cannot be handled and this is the beauty of the proposed modulation strategies and gate pulse generation. To handle this, switches SL4 and SL5 will follow the status of SL3. That is, the three switches are switched ON and OFF together. When they are ON, the terminals of the fourth switch will be shorted together to the negative terminal of the DC source, and there will be no current flow across the load. The proposed gating strategy forbids the case in which both the upper and the lower switches are OFF. So, when switches SL3 to SL5 are OFF, switches SH3 to SH5 will be ON, and so will be switches SM3 to SM5. And the terminals of the fourth load will be shorted together to the positive terminal of the DC source.

The Operation Mode '1100': In this operation mode, all the lower switches (SL1 to SL5) are closed, and the terminals of the third and the fourth loads are shorted together, so there will be no current flow through either of them. And the upper and middle switches will simply operate in a manner similar to the FLI to supply the first and the second loads.

The Operation Mode '1010': the state of switches SH4 and SH5 follows the state of SH3, and the state of switches SL4 and SL5 follows the state of SL3. Now, if the upper switches were ON and the lower switches were OFF, the middle switches will be ON and the terminals of the two loads (the second and the fourth loads) will be shorted together to the positive terminal of the DC source. If the upper and the lower switches were ON, the middle switches will be OFF. The terminals of the second load will be shorted together to the positive terminal of the DC source, and the terminals of the fourth load will be shorted together to the negative terminal of the DC source. Finally, if the upper switches were OFF and the lower switches were ON, the middle switches will be ON and the terminals of both loads will be shorted together to the negative terminal of the DC source.

The Operation Mode '1001': the state of switches SH4 and SH5 is identical to the state of switch SH3, and the state of switches SL1 and SL2 is identical to the state of switch SL3. Now, when switch SH3 is ON, so will be SH4 and SH5, and the three terminals of the second load will be shorted together and there will be no current-flow through them. And when it is OFF, and so are SH4 and SH5, switches SL3 to SL5

will be ON. And as a result, switches SM3 to SM5 will be ON, and the terminals of the second load will be shorted together to the negative terminal of the DC source and there will be no current-flow through the second load. The same scenario goes for the third load.

The Operation Mode '1000': Only the first inverter is active in this mode of operation. The state of switches SH4 and SH5 will follow the state of SH3 to make sure that no current will flow through the second load. All the lower switches (SL1 to SL5) will be always ON, and the states of the middle switches (SM1 to SM5) will be the complement of the states of upper switches (as the lower switches are always ON).

3. SIMULATION RESULTS

The Simulink® model shown in Figure 3 of the proposed inverter is conducted to prove the validity of the inverter and its capability of driving different loads at different voltage levels and frequencies. It is important to point here that the common leg between loads can be selected to be any leg and then PWM must follow up this selection. In Figure 1, the common leg is the third while in the simulation and the experimental work, the fifth leg is the common leg. Four RL loads were used with their values shown in Table 2. The references of the loads are shown in Table 3. The voltage of the DC source is 180V, and the frequency of the carrier is 10 kHz. The results regarding only the representative modes (the modes '1111', '1110', '1100', '1010, '1001' and '1000') will be presented as they are sufficient to prove the validity and the concept of the proposed inverter topology.

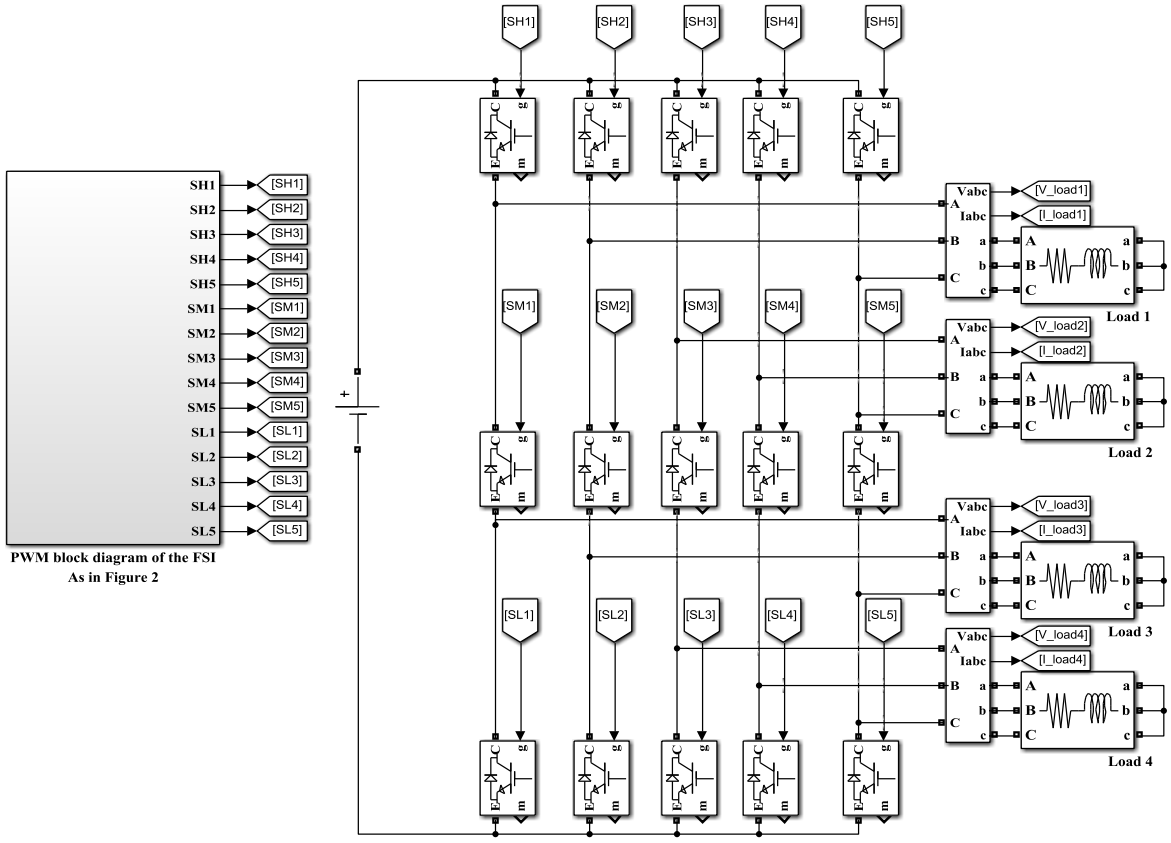

Figure 3. Simulink model of the proposed FSI

Table 2. The loads parameters

Load	Inductance (mH)	Resistance (Ω)
Load #1	12.5	6.8
Load #2	12.5	6.8
Load #3	12.5	6.8
Load #4	1.5	6.8

Table 3. References of the loads

Load	Amplitude (V)	Frequency (Hz)
Load #1	60	100
Load #2	30	50
Load #3	40	25
Load #4	50	150

The current waveforms of the four loads for the representative modes, i.e. the modes '1111', '1110', '1100', '1010, '1001' and '1000', are shown in Figure 4 and Figure 5, respectively. The voltage waveforms for operation mode '1111' only are shown, and that is enough to investigate the behaviour of the proposed inverter from this point of view. The phase voltages of the four loads for the operation mode '1111' are shown in Figure 6(a), while the line voltages are shown in Figure 6(b).

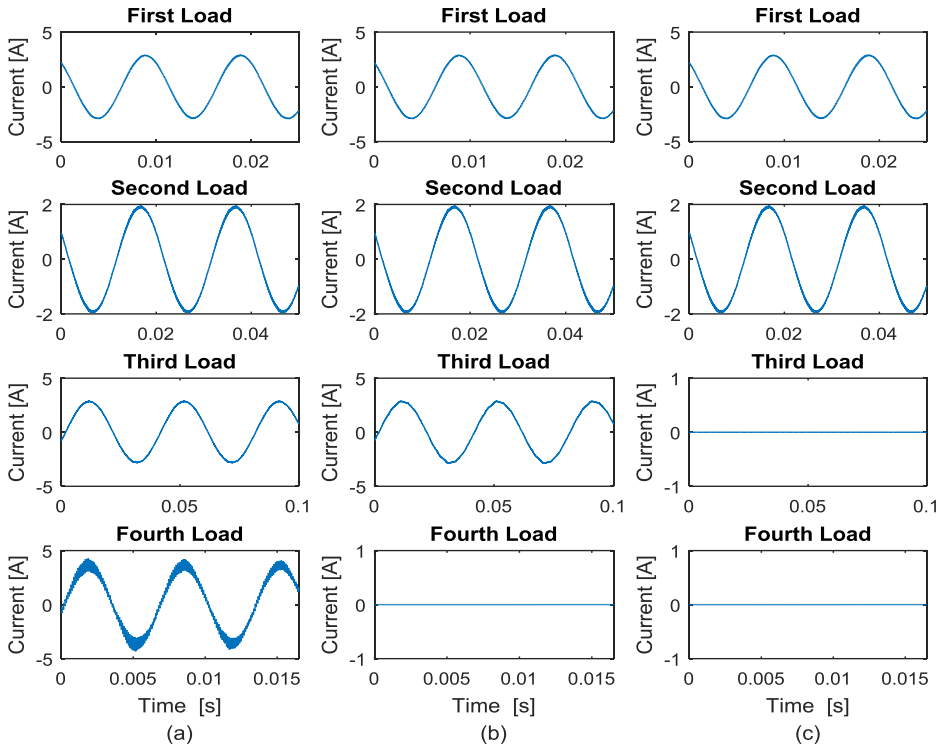

Figure 4. Current waveforms for the four loads, (a) operation mode '1111', (b) operation mode '1110', (c) operation mode '1100'

The results shown in Figures 4 through 6 verify the validity of the proposed inverter, as it managed to drive each load at its desired frequency and voltage level. The results also validate the independency between the loads, as changing the reference of a particular load has no significant impact on the output of the other loads. The currents flowing in the inactive loads are included for further verification of the independent operation of the loads without interference. After the experimental verification, the FPGA-in-the-loop (FIL) test was conducted. In the FIL test, an HDL code representing the proposed PWM scheme was used to reconfigure the FPGA [22], to generate the gate pulses and use them to drive the software model of the proposed inverter, the FIL makes it possible to observe the behaviour of the controller before building the full experimental bed. The FIL results were the same as the results obtained using simulation software only. Which means that the built hardware pulse-generation subsystem is ready to be connected to physical model of the proposed inverter.

The proposed topology is not limited to linear loads. To prove the independency of the four loads, the first load is replaced by nonlinear [23] uncontrolled three-phase rectifier feeding resistive load (34 Ω) shown in Figure 7. The voltage at the dc side is shown in Figure 8 with and without adding 50 µF C-filter at the dc-side. Then, the impact of this nonlinear load on the other loads is investigated as in Figure 9. It is clear

that there is no any interaction between the loads and the other three loads are not affected and independently controlled.

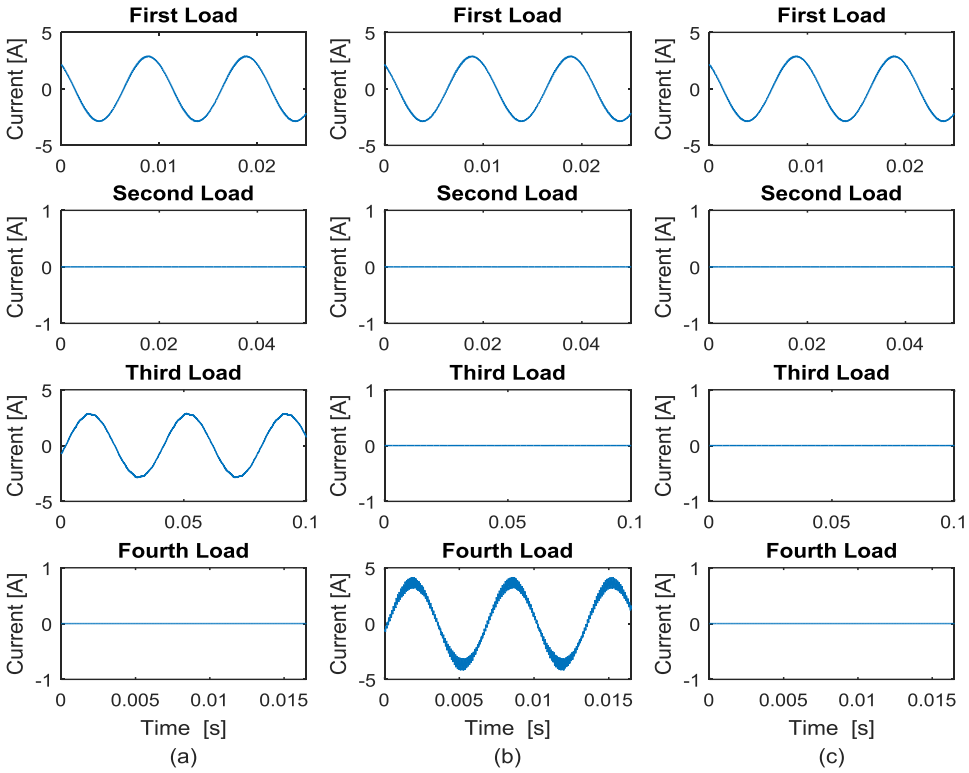

Figure 5. Current waveforms for the four loads, (a) operation mode '1010', (b) operation mode '1001', (c) operation mode '1000'

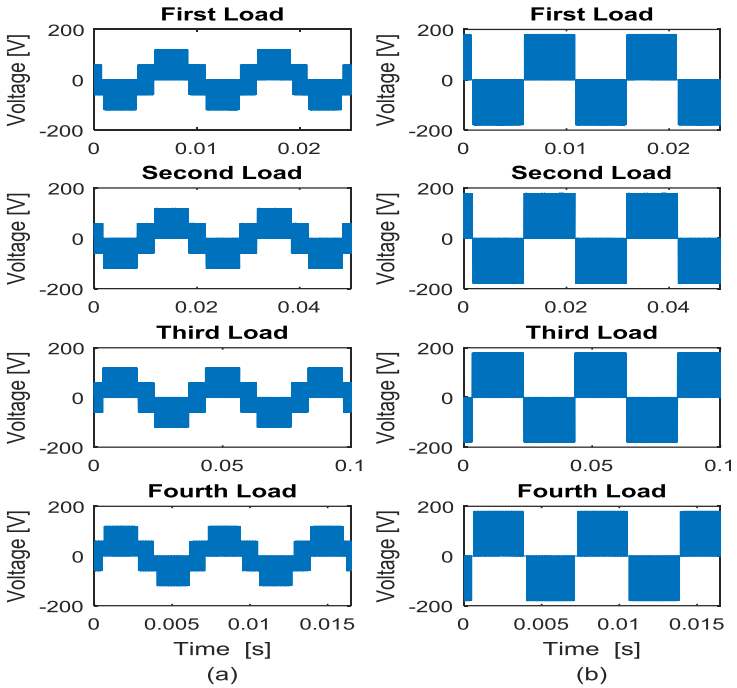

Figure 6. Voltage waveforms for operation mode '1111', (a) phase voltages, (b) line voltages

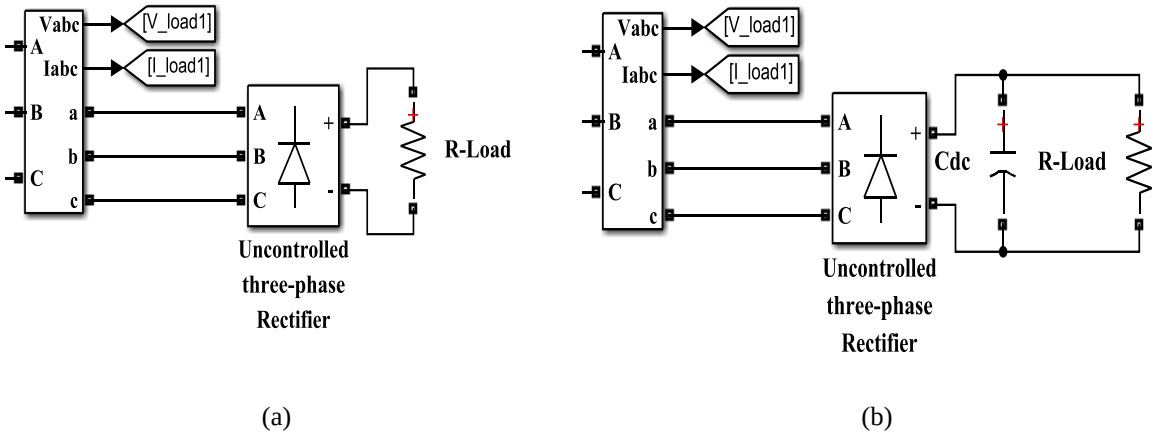

Figure 7. Simulink nonlinear dynamic model of load 1, (a) without C-filter at the dc-side, (b) with C-filter at the dc-side

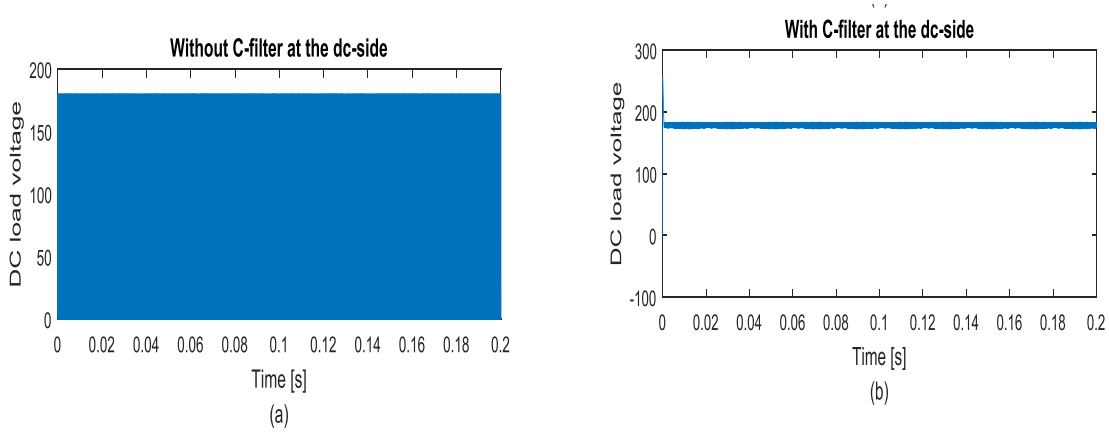

Figure 8. The voltage at the dc-side, (a) without C-filter, (b) with C-filter

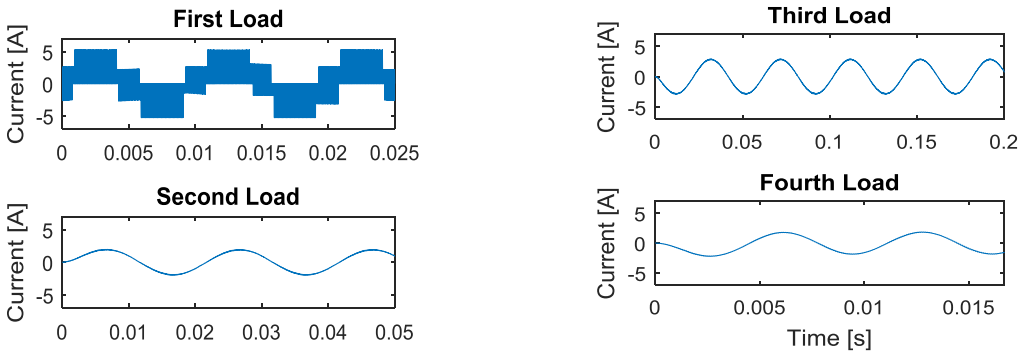

Figure 9. The phase currents of the four loads without adding C-filter at the dc-side

4. EXPERIMENTAL RESULTS

Provide a statement that what is expected, as stated in the "Introduction" chapter can ultimately result in "Results and Discussion" chapter, so there is compatibility. Moreover, it can also be added the prospect of the development of research results and application prospects of further studies into the next (based on result and discussion).

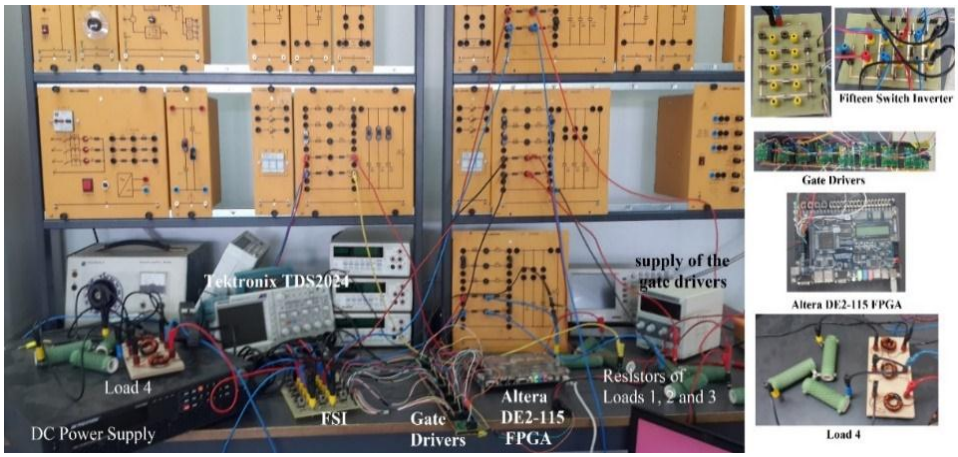

Figure 10. Experimental test bed

The experimental test was conducted using FPGA to generate the pulses required to drive the proposed inverter as shown in Figure 10. The loads used in the experimental test are RL loads with the same parameters used in the simulation test as seen in Table 2. The value of the DC source, the carrier frequency, and the references assigned to each load are the same as those used in the simulation test as seen in Table 3. The purpose of choosing identical parameters for both the experimental and the simulation test is to make the tests more fruitful as that allows for easier comparison between the experimental and the simulation results. The current waveforms for the representative modes are shown in Figure 11 and Figure 12. The phase voltage waveforms and the line voltage waveforms for operation mode '1111' are shown in Figure 13(a) and Figure 13(b), respectively.

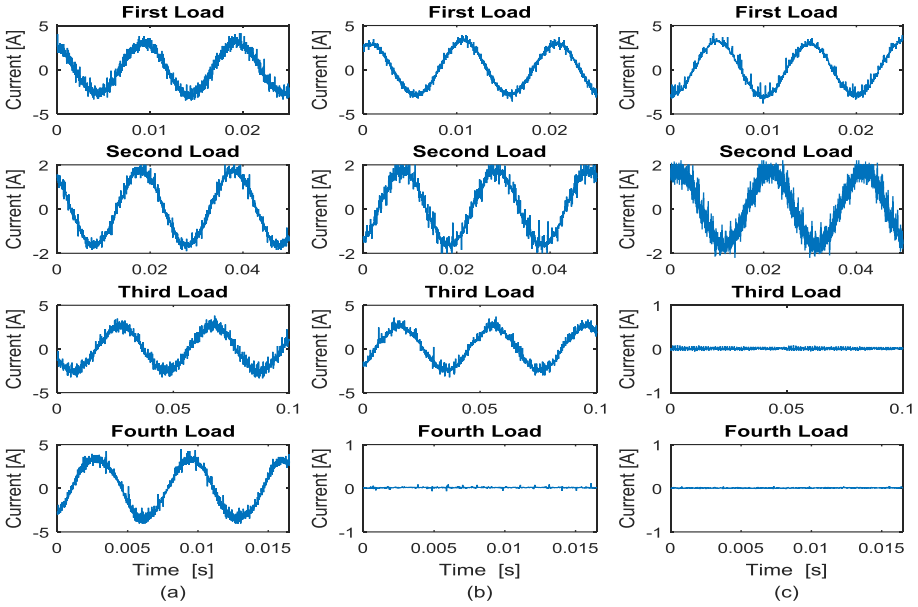

Figure 11. Experimental current waveforms for the four loads (a) Operation mode '1111', (b) Operation mode '1110' (c) Operation mode '1100'

Experimental tests were conducted and the load voltages and currents were measured using Tektronix TDS-2024B digital oscilloscope. The experimental results for different operation modes are shown in Figure 11 to Figure 13, respectively. Figure 11 shows the current waveforms for 1111, 1110, and 1100 operation modes, respectively. The experimental results for modes 1010, 1001, and 1000 are shown in

Figure 12, respectively. Figure 13 shows the phase and line-to-line voltages for operation mode 1111. The experimental results verify the practical validity of the proposed inverter

The experimental results are almost the same as those obtained using software simulation presented in section 3. The proposed inverter successfully utilized the voltage among the loads according to their assigned references. The frequency and the voltage level of each load are exactly the same as the references demand. It is evident from the results that the loads are independently controlled without any significant interference from one load on another. There is a very small interference between the loads that is shown on a small scale through Figure 11 and Figure 12.

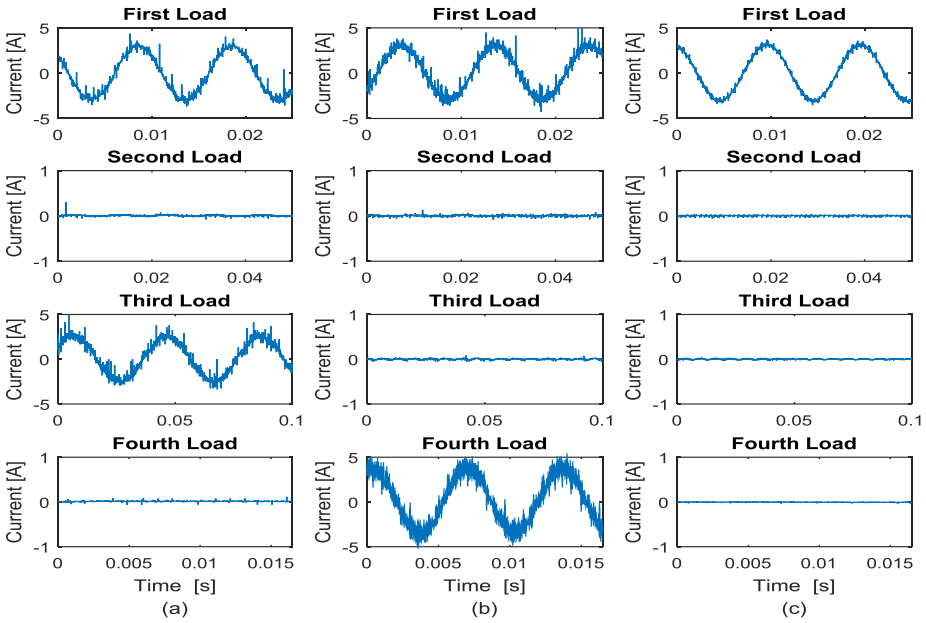

Figure 12. Experimental current waveforms for the four loads, (a) operation mode '1010', (b) operation mode '1001', (c) operation mode '1000'

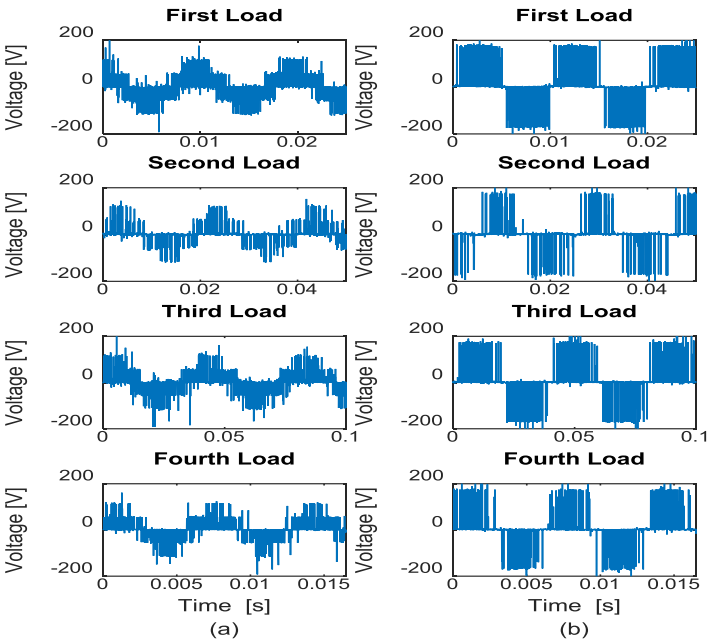

Figure 13. Experimental voltage waveforms for operation mode '1111', (a) phase voltages, (b) line voltages

5. CONCLUSION

In this paper, a new shared inverter topology is introduced. The proposed inverter is capable of independently driving four linear/nonlinear three-phase loads at different frequencies and voltage levels. As a proof of concept, simulation test for all the possible operation modes was conducted, and the results regarding the representative operation modes were introduced. The results verified the capability of the proposed inverter to independently drive the loads. After that, as a mid-stage between the simulation and the experimental tests, the FIL test was conducted. The results obtained using the FIL were identical to those obtained using the simulation test. Finally, to validate the applicability of the proposed inverter in practical application, experimental test using FPGA was conducted. The results were satisfactory as the proposed inverter successfully operated each load at its desired frequency and voltage level in a decoupled manner. As a common problem in shared inverter topologies, there was a very small interference between the loads, although it is small; future work to further reduce or eliminate it is considered. The proposed inverter is suitable for applications involving many loads requiring different frequencies and voltage levels such as production lines in factories and multi-joint robots in robotic applications.

ACKNOWLEDGEMENTS

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