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An approach to Measure Transition Density of Binary Sequences for X-filling based Test Pattern Generator in Scan based Design

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ABSTRACT

Switching activity and Transition density computation is an essential stage for dynamic power estimation and testing time reduction. The study of switching activity, transition densities and weighted switching activities of pseudo random binary sequences generated by Linear Feedback shift registers and Feed Forward shift registers plays a crucial role in design approaches of Built-In Self Test, cryptosystems, secure scan designs and other applications. This paper proposed an approach to find transition densities, which plays an important role in choosing of test pattern generator We have analyze conventional and proposed designs using our approache, This work also describes the testing time of benchmark circuits. The outcome of this paper is presented in the form of algorithm, theorems with proofs and analyses table which strongly support the same. The proposed algorithm reduces switching activity and testing time up to 51.56% and 84.61% respectively.

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1. INTRODUCTION

Power dissipation is a challenging problem in large circuits in very large scale integration VLSI industry and system-on-chips (SoCs) design. The power dissipation of a circuit in test mode is more than in normal mode [1]. The reasons behind increase in power can be:

a. High Switching activity among the patterns
b. Extra power consumed by design for test circuits
c. Low correlation between consecutive vectors which increases the switching activity and power dissipation of the circuit.

This extra power consumption (average or peak power) can create problems such as instantaneous power surge that can create circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product lifetime and yield. Power consumption is of two types: static power and dynamic power. Static power is mainly due to leakage current in the circuit when circuit is in static state i.e. not working, there is still a leakage current flowing in the Complementary Metal Oxide Semiconductor (CMOS) operating in sub threshold region. The leakage current can be given as:

$$il=is(eQ-1) \quad (1)$$

where Q=qv/kT, is reverse saturation current, V is diode voltage, q is electronic charge, k is Boltzmann constant and T is temperature. The product of supply voltage and leakage current gives the value of Static Power dissipation for circuit. If there are m numbers of devices in the circuit then the sum of leakage current of all the devices is taken into consideration to give the average static power dissipation in the circuit as:

$$Ps= (\text{supply voltage} * \text{leakage current}) \quad (2)$$

Dynamic power is mainly due to the switching transient current and charging & discharging of load capacitance [2], [4]. It depends on many factors like load capacitance, supply voltage and frequency of operation. Average dynamic power dissipation in circuit is given by:

$$Pd=CL*Vdd*f \quad (3)$$

This paper [3] address the problem of estimating the average power dissipated in VLSI combinational and sequential circuits, under random input sequences switching activity is strongly affected by gate delays and for this reason, They used a general delay model in estimating switching activity and proposed methods to probabilistically estimate switching activity in sequential circuits. These methods automatically compute the switching rates and correlations between flip-flop outputs [6].In our approach a systematic mathematical method to calculate above parameters.

The switching activity plays a major role in dynamic power consumption. Hence it is important to determine αT while going for low power design. Also switching takes place at all nodes of the circuit, making it difficult to calculate all switching activities simultaneously. Switching activity is responsible for bus power consumption at the nodes. Dynamic Power consumption is not only limited to designing part in VLSI, but also in testing part it is of great concern. A considerable amount of power is consumed while testing digital circuits. Hence low power testing is desired solution. The different solutions to reduce power consumption while testing of a digital circuit are low switching test pattern generators. The low transition activity is preferred in memory testing, designing of low switching address generators, neural networks [7].

The remainder of the paper is organized as follows: In Section 1.1 and 1.2 we describe the definitions and explain the test pattern generators. In Section 2, we discuss the design methodology and the algorithm and their respective proofs to calculate switching activity.In Section 3 explains the results and discussion on transition densities of pattern generator and testing time reduction of our proposed approach.Finally, the paper is concluded with conclusion in Section 4.

1.1. Definitions

Some of the definitions related to the topic are as follows:

a. Signal Probability (P_x)-It is defined as the likelihood that a signal will have the logic value of '1'. A Zero Probability ($\overline{Px}$) means that the signal is always low.
b. Transition Probability-It is defined as the probability that a signal value experiences a transition from 0 to 1, or 1 to 0.
c. Toggle density-It is the number of switches per unit time; the unit is generally one clock cycle.
d. Switching Activity/Activity factor (α_T)-It is defined as the measurement of change in values of a signal.
e. Signal inactivity ($\overline{\alpha T}$)-It is defined as the probability that the signal value remains in the same state
f. Transition Density/Signal activity/Node Transition factor (TD)-It is defined as the average switching rate at a circuit node.

$$TD=\text{Total no of bit transitions/Total no of bits} \quad (4)$$

1.2. Test pattern generators

Pseudo random binary sequences (PRBSs) are also known as pseudo noise (PN) sequences which are easily generated by recursive procedures, such as Linear Feedback Shift Register (LFSR). In a PN, the number of stages gives the sequence length (2n-1) while the clock frequency decides the bit rate. PRBSs have an advantageous feature from the computational viewpoint, and they tend to have useful structural properties. These structural properties, binary sequences have many applications; for example, Direct Sequence Spread Spectrum (DSSS), PN generation, Built-in Self Test (BIST), Decryption–Encryption System (DES) and Error detection [8] Error Correction and Detection codes [9] and other applications include Digital Signal Processing, Wireless Communications, Data Integrity check sums, Data Compression, Scrambler/descrambler, Optimized Counters [10]-[12].

The above mentioned applications use the basic hardware of Linear Feedback Shift Registers (LFSR) to generate Pseudo Random Binary Sequence (PRBS). LFSR consists of two parts: a shift register and a feedback function, as shown in Figure 1. The shift register is a chain sequence of n-bits of D-type of Flip-Flops (FFs). Each time a new bit is needed to load the first bit (D-FF1) of the chains of D-FFs and all the others bits in the shift register are shifted one bit to the right. The feedback function is simply the Exclusive-OR (EOR) operation logic of certain bits of the register.

The new left most bit's state (first bit of D-flip-flop, D-FF1) is computed as a function of the existing feedback taps of LFSR. The output of the feedback shift register is one bit at each clock, often the most significant bit a clock before. The period p of a shift register is the length of the output sequence before it starts repeating [13], [14]. The Linear feedback shift registers make extremely good PN sequence generators of desired period length. A maximal length of p=2n-1 can be generated through an n-bit LFSR. When the flip-flops are loaded with a seed (initial condition) value (anything except all 0s, which would cause the LFSR to produce all 0 patterns) and when the LFSR is locked, it will generate a PN sequence of 1s and 0s. It is important to note that the only signal necessary to generate PN sequence is the clock and initial loading of LFSR [15]. LFSRs are widely used in a wide range of applications because:

a. LFSRs are easy to implement in hardware devices
b. Many LFSRs are combined to achieve better security
c. LFSRs have good statistical properties
d. LFSRs can generate sequences of large periods with different frequencies.

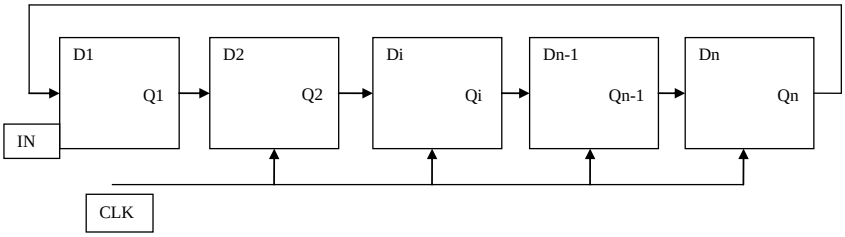

Figure 1. N-bit shift register

Figure 2 shows a 5 bit EOR LFSR structure.
Table 1 shows the next State Patterns for the 5-bit Shift Register.

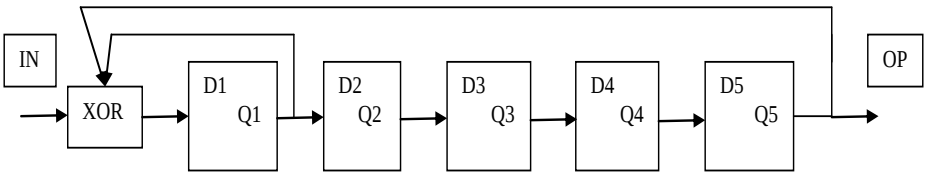

Figure 2. A 5 bit EOR LFSR structure

Table 1. Next State Patterns for the 5-bit Shift Register

Clock	Q1	Q2	Q3	Q4	Q5	Output (OP)
T_1	1	0	0	1	0	0100 …….0
T_2	1	1	0	0	1	
T_3	1	1	1	0	0	
T_4	1	1	1	1	0	
.	.	.	.	.	.	
.	.	.	.	.	.	
T_{32}	1	0	0	0	0	

2. DESIGN METHOD

The procedure used is briefly summarized in the form of a flowchart as shown below:
The algorithm to calculate the number of transitions is as follows:
Step 1: Begin

Step 2: Find number of one's(1's) in the sequence
Step 3: Find size of marix from step 2 row matrix
Step 4: Based on value of LSB and MSB value of step 1
Step 5: Calculate Switching Activity (SA)
Step 6: If LSB = 0, MSB = 0
SA r- α c do
If LSB = 0, MSB = 1
SA = r- α c do
If LSB = 1, MSB = 0
SA = r- α c do
If LSB = 1, MSB = 1
SA = r- α c do
end do
end do
end do
end do
Step 7: Compile the result for Theorem 1
Compile the result for Theorem 2 and Theorem 3
Compile the result for Theorem 4
end

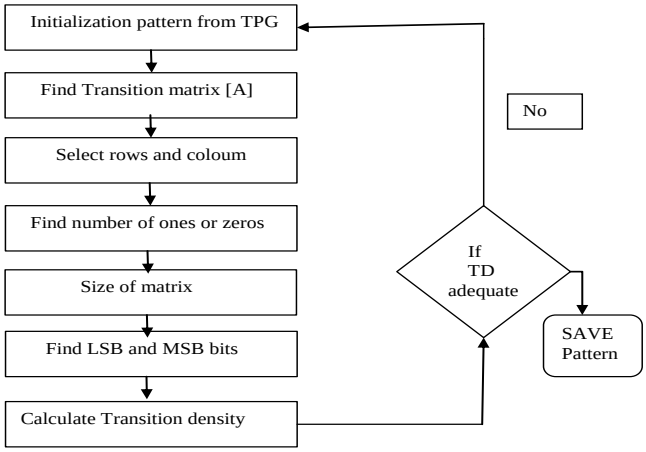

Figure 3. Flow chart

2.1. Study

The study part describes the switching activity (SA) equations for different values of LSB and MSB in any n-length binary pattern

a. Theorem

An n-bit LFSR the output response patterns in th form of matrix [A], where the size of matrix [A] is r x c, the number of row and Colum in matrix [A] is "r" and "c" if LSB(L) is logic "0" and MSB(M) is logic"0" and switching activity SA is given by SA= r-α c where α = 1. Proof. Consider a 4 bit length binary array as test sequence (TS) and compute measurement, area and size of matrix (A) to calculate switching activity (SA).

TS = [0 1 1 0]
A = size(out)
SA= SA= A(1,2)-1*A(1,1) = 2

Thus. SA constituting A(1,2) and A(1,1) are column and row values of matrix A, which gives the final switching activity of n length test sequence.

b. Theorem

An n-bit LFSR the output response patterns in th form of matrix [A], where the size of matrix [A] is r x c, the number of row and Colum in matrix [A] is "r" and "c" if LSB(L) is logic "0" and MSB(M) is logic "1" and switching activity SA is given by SA= r- α c where α = 2.

c. Theorem

An n-bit LFSR the output response patterns in th form of matrix [A], where the size of matrix [A] is r x c, the number of row and Colum in matrix [A] is "r" and "c" if LSB(L) is logic "1" and MSB(M) is logic "0" and switching activity SA is given by SA= r- α c where α = 2. Proof. Consider a 4 bit length binary array as test sequence (TS) and compute measurement, area and size of matrix (A) to calculate switching activity (SA) (proof for theorem 2 and 3).

TS = [0 1 1 1]
A = size(out)
SA = SA = A(1,2)-2*A(1,1) = 1

Thus, SA constituting A(1,2) and A(1,1) are column and row values of matrix A, which gives the final switching activity of n length test sequence. Thus, SA constituting A(1,2) and A(1,1) are column and row values of matrix A, which gives the final switching activity of n length test sequence.

d. Theorem

An n-bit LFSR the output response patterns in th form of matrix [A], where the size of matrix [A] is r x c, the number of row and Colum in matrix [A] is "r" and "c" if LSB(L) is logic "1" and MSB(M) is logic "1" and switching activity SA is given by SA= r- α c where α = 3. Proof. Consider a 4 bit length binary array as test sequence (TS) and compute measurement, area and size of matrix (A) to calculate switching activity (SA).

TS = [1 0 0 1]
A = size(out)
SA= SA= A(1,2)- 3*A(1,1) = 2

Thus, SA constituting A(1,2) and A(1,1) are column and row values of matrix A, which gives the final switching activity of n length test sequence. Consider generated pattern of LFSR in the form of matrix [T] to calculate switching activity in row wise and column, In testing of VLSI digital circuits Switching activity represents the transitions in the bits of the input test vector or the test pattern. It is essential for measuring power in digital circuits, the total power consumption of a circuit during test by reducing the transitions among patterns. The transitions are reduced in two dimensions one is between consecutive patterns used to test combinational circuit, For example Test vectors and second is between consecutive bits used in sequential circuit, For example Test vectors, shown in the below equations

T1 = 10111 SA = 2 (6)

T2 = 10110 SA = 3 (7)

T3 = 10111
T4 = 11110 SA = 2 (8)

In Equations (4) and (5) switching activity measure in between consecutive bits, here switching is changing from 0→1 or 1→0, In equation (6) switching activity measure in between consecutive patterns T3 and T4. The Matrix [T] of the Type II LFSR shown below, If the seed value of the flip flops are x0=1, x1=1, x2=1, X3=0 then the generated patterns shown below as matrix [T] with dimensions rxc is 4x17.

$$\begin{bmatrix} 1&0&0&0&1&1&1&1&0&1&0&1&1&0&0&1&0 \\ 0&1&0&0&0&1&1&1&1&0&1&0&1&1&0&0&1 \\ 0&0&1&0&0&0&1&1&1&1&0&1&0&1&1&0&0 \\ 0&0&0&1&1&1&1&0&1&0&1&0&1&1&0&0&0 \end{bmatrix}$$

Select first row from matrix [T] and apply theorem 2 to obtain switching activity, similarly for row 2,3 and 4 apply theorem 2,1 and 1 respectively. Apply transpose matrix TT=T. TT = [1 0 0 0, 0 1 0 0, 0 0 1, ……., 0 1 0 0] dimensions r x c is 17 x 4, apply theorem 1 to 4 depends on LSB and MSB values.

3. RESULT AND DISCUSSION

The transition density (TD) can be measure mathematically shown in Equation (9), but we need to calculate probability of one i.e P1 in generated test patterns. Transition density is twice of the product of probabailty of one and zero, where probability of zero can be expressed as (1-P1).

$$TD = (1-P1)\ P1 + P1\ (1-P1) = 2P1\ (1-P1) \quad (9)$$

The time reduction in scan chain will be dominated by the largest scan chain and for a transition density TD and the overall frequencies of system that is "f ", system hardware configuration are 3.60 GHz intel core i5 processor with 4.0 GB memory RAM and 64x86 linux operating system.

$$\text{Test time reduction} = 0.5\ (1- TD) – 0.5\ f \quad (10)$$

Table 2, show the switching activity and average probability for LFSR and proposed SIC test pattern generators.switching activity calculated for N=5 between consecutive patterns as shown in Equations (6)-(8).Our method reduces activity up to 51.56%. The average probability of 1 for each pattern calculated and improves up to 14.73%. The effectiveness of ramdom values for transition density and probability shown in Figure 4. It can be seen that above parameters measure for 31 clock cycles and huge randon also can be observed,this characteristics of randomness improves fault covege effectively in testing of VLSI circuits.

Table 2. Manual clock wise Transition Density Comparison

Clk	LFSR [1], [6], [9], [12]	Zero Fill and One Fill (X-FILLING)
0	1 1 1 1 1	0 0 0 0 0
1	0 1 1 1 1	0 0 0 0 1
2	0 0 1 1 1	0 0 0 1 1
3	0 0 0 1 1	0 0 0 1 0
….	….	…..
26	0 0 1 1 0	1 0 0 1 1
27	1 0 0 1 1	1 0 0 1 0
28	1 1 0 0 1	1 0 1 1 0
29	1 1 0 1 0	1 0 1 1 1
30	1 1 1 1 0	1 0 1 0 1
31	1 1 1 1 1	1 0 1 0 0
	Transitions = 64	Transitions = 31

Table 3 shows the TPG Comparison of bit length N=5.

Table 3. TPG Comparison of bit length N=5

TPG	Bit lenght (N)	Switching activity	Average probability P (1)
LFSR [1][6][9][12]	5	64	19
Proposed	5	31	16.2
Saving (%)	-	51.56	14.73

Gray encoder in Figure 4 is used to encode the counter's output C[n-1:0] so that two successive values of its output GC[n-1:0] will differ in only one bit. Gray encoder can be implemented by following equations.

GC[0] = C[0] XOR C[1]
GC[1] = C[1] XOR C[2]
GC[2] = C[2] XOR C[3]
…
GC[n-2] = C[n-2] XOR C[n-1]
GC[n-1] = C[n-1]

The seed generating circuit modified LFSR structure to apply swapping between the neighboring bits. The last bit is the selection line for the swapping process. If the last bit is '0', then swapping is performed, else nothing will change. The final test patterns are implemented as following equations.

SG[0] = X[0] XOR GC[0]
SG[1] = X[1] XOR GC[1]
SG[2] = X[2] XOR GC[2]
…
SG[n-1] = BF[n-1] XOR GC[n-1]

The X-filler clock will be TCK/2m due to the control signal. As SICG's cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too. Xfillng used 0-fill,1-fill and Adjacent fill techneques to generate seed value, generated seed value further xored with SIC generated value. On the other hand transition density of SG value measure with flow chart shown in Figure 3, generated pattern with lesser TD chose to test benchmark circuits. For testing purpose we used adk.atpg library along with non scan netlist generated fron leonarto spectrum given to as shown in Figure 5.

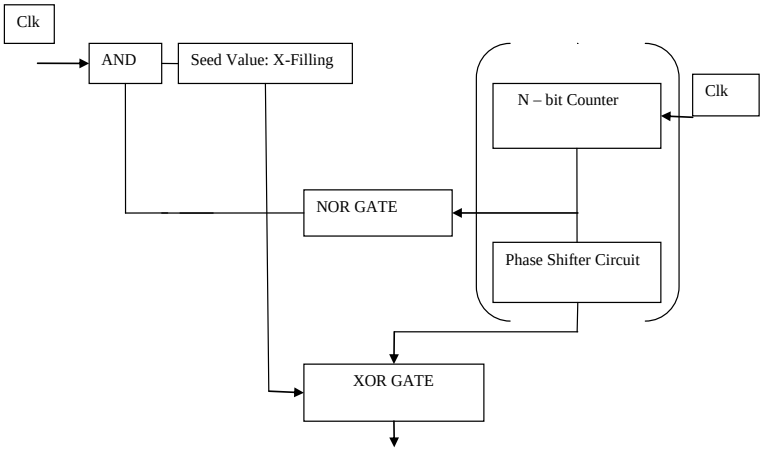

Figure 4. SIC-TPG with X-filling Technique

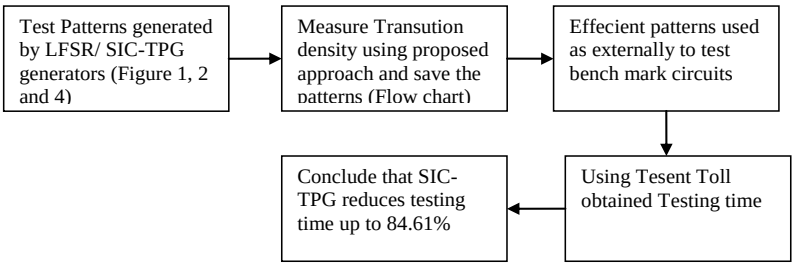

Figure 5. Complete folw to measure transition densities and testing time

Further, TD and test time reduction can be calculated using Equations (9) and (10). Table 4, shown the SA and TD for different lengths N (4 bit to 256 bit) , It can be observed that for each length, find least and most significant bits and applies theorm 1 to 4 to calculate SA and TD values. Table 5, describes the complete CPU timing analysis for ISCAS 85 and 89 benchmark circuits between LFSR and proposed method, this can obtained using Mentor graohics Tessent tool, where effective pattaern inserted in standard template and applied externally, the adk.atpg library along with .do file and test procedures file have been used to test the circuits.

Table 4. SA and TD Table for different Lengths

N	LSB	MSB	Theorem	SA	TD
4	0	0	1	2	50
8	0	1	2	5	62.5
16	1	0	3	11	68.75
32	1	1	4	24	75
64	0	0	1	48	75
128	0	1	2	95	74.2
256	1	1	4	190	74.2

Table 5. Execution CPU time for ISCAS 85 and 89 Benchmark circuits

Circuits	Size (#Flip Flops + #Gates)	Total CPU Testing Time (Sec)
ISCAS 85and 89	Area	[1], [6], [9], [12]	Proposed
C17	0+6	1.3	0.1
C432	0+16	1.2	0.2
C499	0+546	1.3	0.2
C3540	0+1669	1.4	0.3
S27	3 +10	1.2	0.2
S271	14+133	1.2	0.2
S298	14+119	1.3	0.2
S344	59+160	1.3	0.2
S349	57+161	1.3	0.2
S382	21+158	1.3	0.2

4. CONCLUSION

The main purpose of above proposed algorithm is to find out switching activity and transition densities for n length sequence and also proposed the four theorems along with their proofs, The SA depends on LSB and MSB values of n length sequence. This algorithm is helpful in finding of efficient test patterns generator, a, further thses patterns can be used externally to test VLSI circuits. The proposed method reduces switching activity and testing time up to 51.56% and 84.61% respectively.This approach can also be used for various applications such as DFT crypto systems, Coding theory and techniques and Communication systems.

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