International Journal of Electrical and Computer Engineering (IJECE)
Vol. 9, No. 3, June 2019, pp. 1598~1605
ISSN: 2088-8708, DOI: 10.11591/ijece.v9i3.pp1598-1605

Fault modeling and parametric fault detection in analog VLSI circuits using discretization

Baldev Raj[1], G. M. Bhat[2], Sandeep Thakur[3]
[1]Department of Electronics and Communication Engineering, GCET India
[2]Institute of Engineering and Technology, Kashmir University, India
[3]Department of Electronics and Communication Engineering, Global Institute of Engg. and Technology Markpur, India

Article Info

Article history:

Received Oct 29, 2017
Revised Nov 14, 2018
Accepted Dec 21, 2018

Keywords:

Analog VLSI circuit
Discretization
Fault modeling
MATLAB
Parametric faults

ABSTRACT

In this article we describe new model for determination of fault in circuit and also we provide detailed analysis of tolerance of circuit, which is considered one of the important parameter while designing the circuit. We have done mathematical analysis to provide strong base for our model and also done simulation for the same. This article describes detailed analysis of parametric fault in analog VLSI circuit. The model is tested for different frequencies for compactness and its flexibility. The tolerance analysis is also done for this purpose. All the simulation are done in MATLAB software.

Corresponding Author:

Baldev Raj,
Department of Electronics and Communication Engineering,
Government College of Engineering and Technology Jammu, India.
Pin:181121 Cell Phone No: 9906359745
Email: baldev.gcet@gmail.com

1. INTRODUCTION

In present scenario analog VLSI circuits are used in wide number of applications such as multimedia, cellular communication, digital signal processing and data acquisition. The testing of analog VLSI circuit is a major task before designing and fabrication of any product. The fault detection in analog VLSI circuits is very difficult task due to complexity nature of analog circuits. There is no simple fault model for analog VLSI circuits at present in digital circuits. There are two types of fault model are present in analog circuits. These are catastrophic fault model and parametric fault model. In catastrophic, there is large deviation at output due to large variation in component values (due to short or open circuit). In parametric model, the component value will change from nominal value to certain extent. The parametric fault is caused by variations in component values due to time and environment. Sometimes the parametric fault causes the change in output behavior of the system. But catastrophic fault changes the behaviour of circuit completely [1], [2], [3].

2. BASIC PRINCIPLE

A large number of analog VLSI circuits can be represented by linear state variable equations [4], [5], [6]. For simplicity here we take single output state variable circuit where the output of every block contains a capacitor (memory element.). The state equation for the circuit is given by

$$\dot{X}(t) = A\,X(t) + B\,U(t) \quad (1)$$

$X(t) = [x_1(t), x_2(t), \dots, x_n(t)]^T$ is state vector containing n variable.

$\dot{X}(t) = [\dot{x}_1(t) + \dot{x}_2(t), \dots, \dot{x}_n(t)]^T$

Here $\dot{x}_1(t)$ is derivative with time. The output of the system is given by y (t).

$$y(t) = C\ X(t) + D\ U(t) \quad (2)$$

By taking Laplace transform we change state variable equation from time domain to frequency s domain that is given by

$$sX(s) = A\ X(s) + BU(s) \quad (3)$$

From these equations we can derive from signal flow graph [7], [8]. Here we are taking example of Biquadratic Filter circuit. In Figure 1 and Figure 2 the circuit diagram and signal flow graph of biquadratic filter circuit are shown. The biquadratic filter circuit contain three op-amp. First operational amplifier is inverting op-amp, second is integrator and third is lossy integrator.

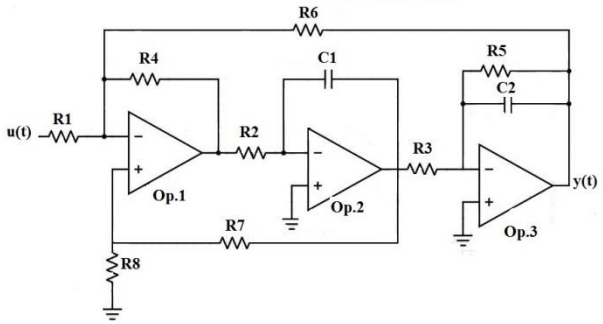

Figure 1. Circuit diagram of biquadratic filter

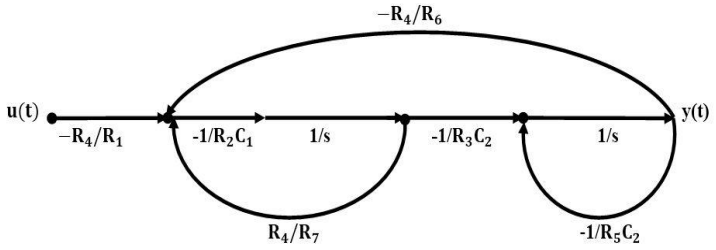

Figure 2. Signal flow graph of biquadratic filter circuit

By using all the resistor value equal to R and all capacitor value equal to C. Then we have ω_0=1/RC. From Figure 2 we can write state equation

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \begin{bmatrix} -\omega_0 & \omega_0 \\ -\omega_0 & -\omega_0 \end{bmatrix} \begin{bmatrix} \frac{x_1(s)}{s} \\ \frac{x_2(s)}{s} \end{bmatrix} \begin{bmatrix} \omega_0 \\ 0 \end{bmatrix} u(s) \quad (4)$$

By applying bilinear transform we get z transform from s domain. In bilinear transform

$$s = \frac{2}{t_s} \frac{z-1}{z+1} \quad (5)$$

Here t_s is sampling time.
By using (4) and (5) we get

$$Z_A = (2/t_s\, I - A)^{-1}(2/t_s\, I + A) \tag{6}$$

$$Z_B = (2/t_s\, I - A)^{-1}B \tag{7}$$

So that we can write

$$X(z) = Z_A z^{-1}X(z) + Z_B z^{-1}(u(z) + u(z)) \tag{8}$$

Here z^{-1} is delay. This equation can be write in time domain

$$X(t_k) = Z_A X(t_{k-1}) + Z_B(u(t_{k-1}) + u(t_k)) \tag{9}$$

Here u(t) is input for simulation of biquadratic filter circuit. And sampling rate is $1/t_s$. And sampling frequency is $f(s) = 1/t_s$. In biquadratic filter circuit we use R=10k and C=0.02µF and we get $\omega_0 = 5000Hz$ and using nyquist criterion t_s=0.0001sec. By using these parameter we find state equation in Z domain.

$$\begin{bmatrix} x_1(z) \\ x_2(z) \end{bmatrix} = \begin{bmatrix} 0.538 & 0.308 \\ -0.308 & -0.538 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.192 \\ -0.038 \end{bmatrix} (u(z) + z^{-1}.u(z)) \tag{10}$$

By applying sinusoidal input u(t)=0.1sin(2π.500t).We simulate biquadratic filter circuit.

3. MODELING OF FAULTS

For the measurement of different fault occuring in circuit one should have complete fault list. There are two types of faults occur in analog VLSI circuits. These are parametric fault and catastrophic fault. Parametric faults occur in circuit due to some manufacturing defects (change in some parameter like due to doping level and due to oxide thickness). Due to parametric faults in circuit the tolerance of component will vary to certain value. In these types of faults the circuit output may or may not be changed. The value of component is increase or decrease to certain value, these type of faults we can be removed with the help of knowing the tolerance of component (ie. If there is some change in value then how much output of system is changed). Catastrophic faults are completely changed the output of the circuit. These cause the short circuit or open circuit. These are also called hard fault. Due to this type of fault the behavior of system changed drastically. These are random faults [9], [10].

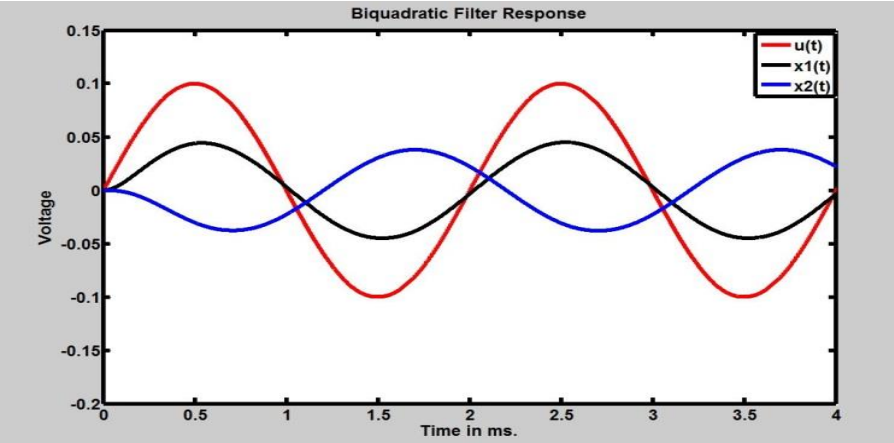

Figure 3. Biquadratic filter simulation using MATLAB for different inputs

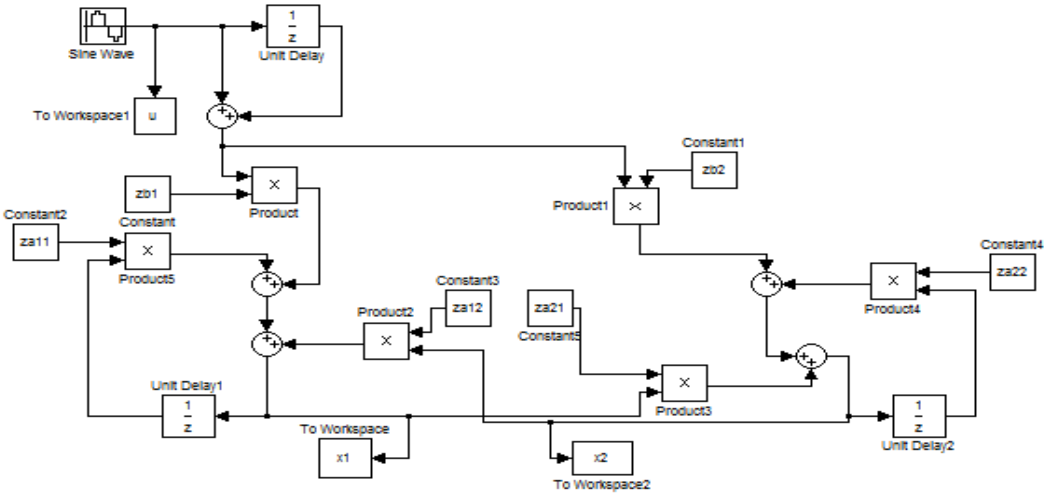

Figure 4. Biquadratic filter in discrete form (using Simulink)

4. EFFECTS CAUSE BY SINGLE FAULT IN CIRCUIT

When we simulate the circuit with fault the z domain state equation is assumed as discrete network as shown in Figure 4. Here the coefficient of multiplier are za_{ij} andzb_i. These are the elements from $Z_A$andZ_B. Single fault appears with multiple faults in discrete circuit [8]. For example there is fault in R_5. That is the value of R_5 is changed from its original value. The original value of R_5=10k due to fault is changed to R_5=1k**.** This fault effect the entire matrices of s domain where R_5 is present. Where as it effects both in z domain that is $Z_A$andZ_B. The change in state equation due to fault occur in circuit.

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \begin{bmatrix} -5000 & 5000 \\ -5000 & -500 \end{bmatrix} \begin{bmatrix} x_1(s)/s \\ x_2(s)/s \end{bmatrix} + \begin{bmatrix} 5000 \\ 0 \end{bmatrix} u(s)$$

By in z domain it is given as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \end{bmatrix} = \begin{bmatrix} 0.526 & 0.372 \\ -0.372 & -0.860 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.191 \\ -0.047 \end{bmatrix} (u(z) + z^{-1}.u(z))$$

Number of states changed due to single fault in circuit is shown. The major cause of circuit failure is parasitic capacitance. For example here we consider capacitance C_f effect which is at negative terminal of operational amplifier first and output terminal of operational amplifier. Due to this capacitance faulty state is generated which will increase the states. Here we represent it as faulty state (x_f).

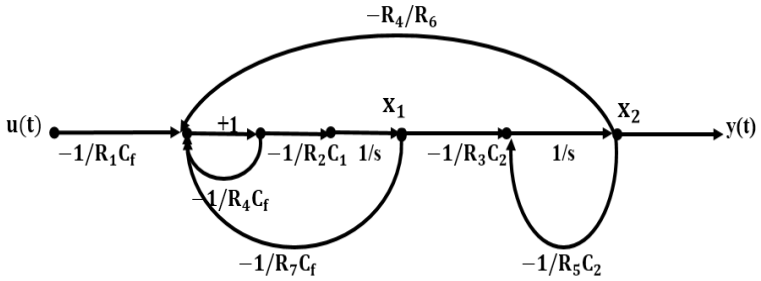

Figure 5. Signal flow graph with increased states for biquadratic filter

Due to the presence of parasitic capcitance the state equation is also changed and can be written as.

$$\begin{bmatrix} x_1(s) \\ x_2(s) \\ x_3(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -5000 \\ -5000 & -5000 & 0 \\ 5000 & -5000 & -5000 \end{bmatrix} \begin{bmatrix} x_1(s)/s \\ x_2(s)/s \\ x_3(s)/s \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 5000 \end{bmatrix} u(s)$$

And in z domain are given below

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ x_f(z) \end{bmatrix} = \begin{bmatrix} 0.887 & 0.075 & -0.377 \\ -0.377 & -0.585 & 0.075 \\ 0.453 & -0.302 & 0.509 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.047 \\ -0.009 \\ -0.189 \end{bmatrix} (u(z) + z^{-1}.u(z))$$

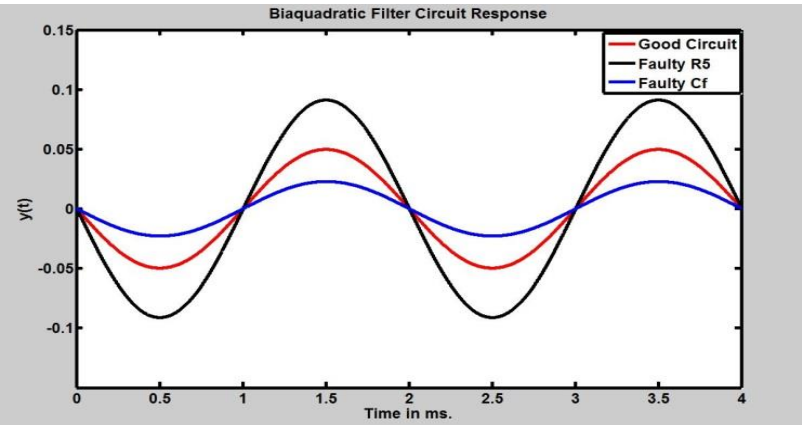

Figure 6. Fault Free and Response of Biquadratic filter at f=500Hz using MATLAB

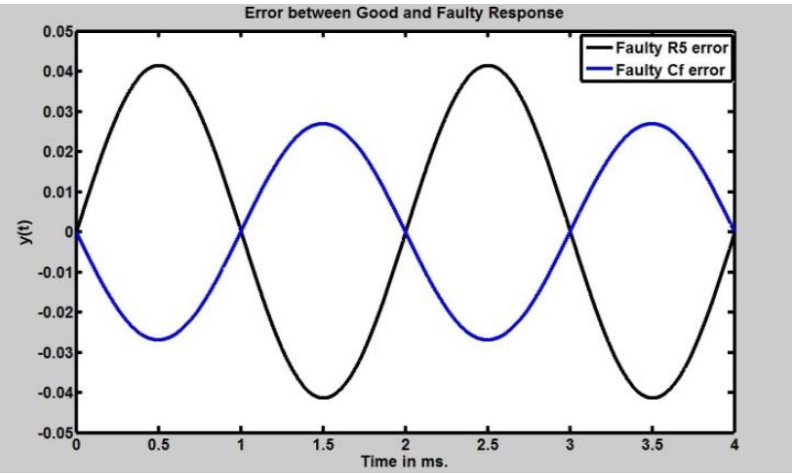

Figure 7. Error Difference between the good and faulty response of Biquadratic filter circuit using MATLAB Tool

5. FAULT SIMULATION

Our approach work serially for analog VLSI not like parallel approaches, because is not possible to detected all the faults in the circuit. Here we apply this approach to the parametric fault occuring in the analog VLSI circuit that is when the value of the component changes slightly and the output response of the circuit is changed completely. So it is very necessary to detect this fault. Here in first case we assume fault in

R_5 resistor in the biquadratic filter. Then with the help of our approach we detect the response of the good and faulty biquadratic filter circuit. This approach is applicable to all types of circuit which we can convert into the signal flow graph. Our approach is simple and efficient as compared to the methods used now a days [8].

6. IMPLEMENTATION OF ALGORITHM

The algorithm for fault modelling and detection is constructed with the help of MATLAB and Simulink [10]. The entire algorithm to compute fault in circuits is shown in Figure 8.With the help of given algorithm we can easily detect the fault in analog VLSI circuit. In this paper we applied our algorithm to two circuit first is Biquadratic filter circuit and second circuit is leap frog filter circuit. Both circuit are benchmark circuit. Before the implementation of testing method, the method should be applicable to these circuits [11].

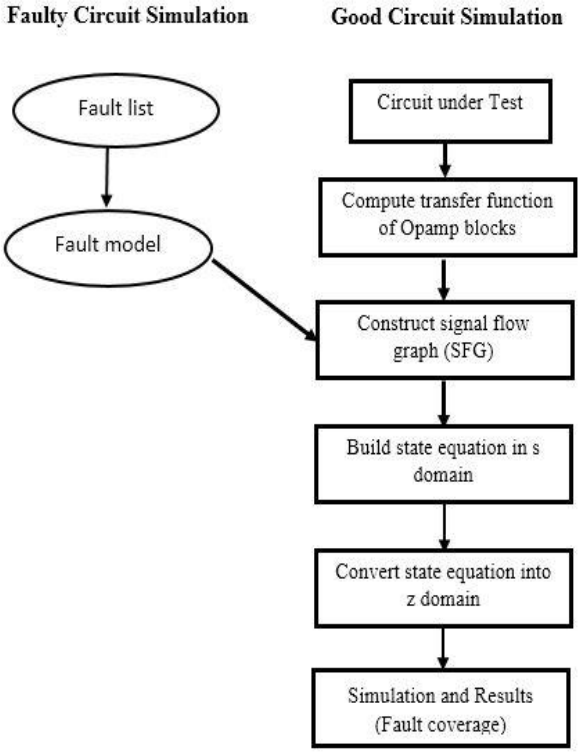

Figure 8. Algorithm to compute fault in circuits

7. TOLERANCE ANALYSIS USING SENSITIVITY

Sensitivity analysis of analog circuit provide us the information about various component present in the circuit. The design engineer need to choose as many inexpensive components as possible, by keeping the circuit performance stable, he need to decide which elements are sensitive and how much value they required for the tolerance. With the help of sensitivity analysis we also know about the component characteristics variation in circuit and its effect on performance of system output [12].

8. SENSITIVITY ANALYSIS

8.1. Sensitivity analysis approach

A simple definition of sensitivity is how much specific system behavior/characteristic changes as a individual component value changes [11], [12]. The general equation for sensitivity analysis is given below.

$$S_x^y = \lim_{\Delta x \to 0} \frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} = \frac{x}{y}\frac{\partial y}{\partial x} \quad (11)$$

Equation (11) is the general mathematical definition of circuit sensitivity: Where S represent sensitivity, X represent changing element/component and Y is the characteristic of circuit which one want to evaluate as component value is varied. The middle part of this equation shows that the percentage that the dependent variable Δy/y changes, relative to the percentage that the independent variable Δx/x changes.

The sensitivity analysis done by using these formulae derived below. Let's take a transfer function H(s).

$$\mathrm{H(s)} = \frac{N(s)}{D(s)} \tag{12}$$

HereN(s) represent the numerator part of transfer function and D(s) represent the denominator part of transfer function. From (11) and (12), we write a new equation which is same as (13), but its variable name are changed to make our calculation easy. In general, the AC-sensitivity is given by the following equation:

$$\mathrm{Sens(H(s), W)} = \frac{\mathrm{W}}{\mathrm{H(s)}} \frac{\partial \mathrm{H(s)}}{\partial \mathrm{W}}$$

Substituting equation (11) into (12) and applying the chain rule have

$$\mathrm{Sens(H(s), W)} = \mathrm{W}\left(\frac{1}{\mathrm{N(s)}} \frac{\partial \mathrm{N(s)}}{\partial \mathrm{W}}\right) - \left(\frac{1}{\mathrm{D(s)}} \frac{\partial \mathrm{D(s)}}{\partial \mathrm{W}}\right) \tag{13}$$

Here W is the component which one want to vary w.r.t. circuit transfer function. By using above (13) we can calculate the sensitivity of circuit any circuit.

8.2. Sensitivity analysis of voltage divider circuit

Here we consider voltage divider circuit in Figure 9 and by applying above formulae of sensitivity we derive these equations. This is the simplest example we have taken here. By using this example, we get information about the components of the circuit which are sensitive (according to their value).

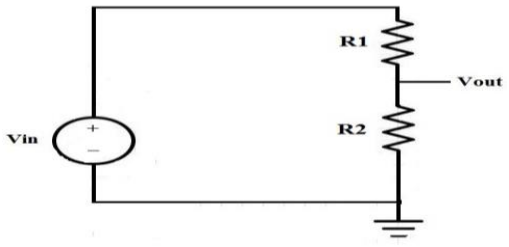

Figure 9. Voltage divider circuit

The DC transfer function of is given in equation below

$$\mathrm{H(s)} = \frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = \frac{R_2}{R_1+R_2} = \frac{\mathrm{N(s)}}{\mathrm{D(s)}}$$
$$S_{T_{DC}}^{R_1} = -\frac{R_1}{R_1+R_2} \tag{14}$$

By using equation (13), we calculate the sensitivities transfer function w.r.t. $\mathrm{R_1}$ and$\mathrm{R_2}$.

$$S_{T_{DC}}^{R_2} = \frac{R_1}{R_1+R_2} \tag{15}$$

In above equation shows that the DC transfer function is changes w.r.t. $\mathrm{R_1}$ and $\mathrm{R_2}$. As shown in (14) contain negative sign this implies that if $\mathrm{R_1}$ increases then corresponding transfer function decreases. But in case of $\mathrm{R_2}$ it is opposite that when $\mathrm{R_2}$ increases then transfer function also increases.

In first case, let us assume $\mathrm{R_1}$ is very large then the equation becomes $-\frac{\mathrm{R_1}}{\mathrm{R_1}} = -1and\frac{\mathrm{R_1}}{\mathrm{R_1}} = 1$. This shows that the transfer function changed by nearly 1% for 1% change in either resistor under these

conditions. In second case if R_2 is very large this results sensitivity equation equal to zero when R_1=0 and R_2=∞. Due to this transfer function changed very small when there is variation in resistor value. In third case, let us take R_1=R_2 then transfer function becomes 0.5 and sensitivities are -0.5 and 0.5. Now we expect that the transfer function will changed to 0.5% for 1% variation in either resistor. But by increasing R_2 to 1% and transfer function is 1/2.01=0.498 which is reduction of 0.5%. In similar manner we increase R_1 by 1% which gives 1.01/2.01= 0.502, which is increase of 0.5%. This is sensitivity analysis of very simple circuit which contain only resistor. Now we calculate the sensitivities of circuits which contain resistor, capacitor and inductor.

9. CONCLUSION

Here we have proposed a new approach for fault detection in linear analog VLSI circuits. This approach is done by using discretizing the circuit in z domain and sampling frequency is chosen to achieve maximum accuracy. In this study all the simulations and calculations for transfer function, state equation in s domain as well as z domain are done with the help of MATLAB and algorithms of all models are constructed with the help of SIMULINK. This approach is very effective to linear analog VLSI circuits and our proposed algorithm is applicable to mostly all analog VLSI circuits.

ACKNOWLEDGEMENTS

We express our gratitude & appreciation to Dr. Bhopinder Singh, Dr. Subash Dubey, Dr. Sameru Sharma, Dr. M. Tariq Banday, Dr. Sarbjeet Singh, Dr. Simmi Dutta, Er Rouf Ahmed Khan, Er Major Singh, Ms.Sharda Kumari, Er. Mohit Bharti, Mr. Abhiluv Bharti and Ms.Kashish Bharti for their technical and moral support. Last but not least we are thankful to our parents for their encouragement.

REFERENCES

[1] Y. Lu and R. Dandapani, "Hard Fault Diagnosis in Analog Circuits Using Sensitivity Analysis," *Proc. of the IEEE VLSI Test Symp*., pp. 225–229, 1993.
[2] S. Thakur, "A Complete Analysis of Channel Estimation and Peak to Average Power Ratio in Wireless Communication Using Discrete Fourier Transform," 2016.
[3] A. C. Sanabria-Borbon and E. Tlelo-Cuautle, "Symbolic sensitivity analysis in the sizing of analog integrated circuits," *Computing Science and Automatic Control*, 2013.
[4] R.P. Sallen, and E.L. Key, "A Practical Method of Designing Active Filters," IRE Transactions on Circuit Theory, March, vol. CT-2, pp.74-85, 1955.
[5] L.P. Huelsman, and P.E. Allen, "Introduction to the Theory and Design of Active Filters," McGrawHill, New York, 1980.
[6] L. Milor and V. Visvanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits*," IEEE Trans. on Computer-Aided Design*, vol. 8, pp. 114–130, 1989.
[7] S. Thakur, K. V. V. Satyanarayana and K. C. M. Reddy, "Diagnosis of parametric faults in linear analog VLSI circuits," 2016 10th International Conference on Intelligent Systems and Control (ISCO), Coimbatore, pp. 1-5, 2016. doi: 10.1109/ISCO.2016.7727099
[8] N.B. Hamida and B. Kaminska, "Multiple Fault Analog Circuit Testing by Sensitivity Analysis," *J. Electronic Testing: Theory and Applications*, vol. 4, pp. 331–343, 1993.
[9] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Heurtas, B. Kim, A. Rueda and M. Soma, "Analog and Mixed-Signal Benchmark Circuits First Release*," IEEE International Test Conference*, Washington DC, 1997.
[10] S.-J. Tsai, "Test Vector Generation for Linear Analog Devices*," Proc. of the IEEE Int'l. Test Conf*., Oct., pp. 592–597, 1991.
[11] N. Balabanian, T.A. Bickart and S. Seshu, "Electrical Network Theory," John Wiley & Sons, Inc., chap. 9, (1969), pp. 646–647. [11] The Math Works Inc. MATLAB User's Guide, 2009.
[12] S. Thakur and A. Naithani, "A novel approach for calculation of component tolerance in analog VLSI circuits using ISFG technique," 2016 Online International Conference on Green Engineering and Technologies (IC-GET), Coimbatore, pp. 1-5, 2016. doi: 10.1109/GET.2016.7916792