

Simplified Space Vector Pulse Width Modulation based on Switching Schemes with Reduced Switching Frequency and Harmonics for Five Level Cascaded H-bridge Inverter

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ABSTRACT

This paper presents a simplified control strategy of spacevector pulse width modulation technique with a three segment switching sequence and seven segment switching sequence for high power applications of multilevel inverters. In the proposed method, the inverter switching sequences are optimized for minimization of device switching frequency and improvement of harmonic spectrum by using the three most desired switching states and one suitable redundant state for each space vector. The proposed three-segment sequence is compared with conventional seven-segment sequence for five level Cascaded H-Bridge inverter with various values of switching frequencies including very low frequency. The output spectrum of the proposed sequence design shows the reduction of device switching frequency, current and line voltage THD, thereby minimizing the filter size requirement of the inverter, employed in industrial applications, where sinusoidal output voltage is required.

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1. INTRODUCTION

With ever increasing demand, of electrical energy and depleting fossil fuel reserves, the efficiency utilization of existing resources have become compelling requirement. High efficiency power electronic converter topologies with optimized control strategies are required to minimize the energy waste and improve the power quality. The design of controlled medium voltage drives is faced with challenges that relate to the topologies and control of the and motor side converters. The voltage and currents wave forms are effected by factors like topology used the control algorithm the filter size, choice of switching frequency and the application .The switching on of medium voltage semi conductor devices also make up the major part of device losses, their reduction allows the maximum output power while the other side the reduction of switching frequency causes the increased harmonic distortion of motor side waveforms. Thus the area need careful consideration for efficient drive system[1]. Multi level converter after many advantages like good power quality, low switching losses, high voltage capability, low dv/dt stress [2].

The three bench mark topologies for high power medium voltage applications are neutral point clamped, series cascaded H-bridge, flying capacitor converter cascaded H bridge VSC has been applied for high power and power quality industrial requirement due to it series expansion capabilities in industrial main applications include, active filter, reactive power compensation, electric vehicles photo voltaic power conversion, ups etc. this topology can be operated at different switching frequencies for different application [3]. The H-bridge is supplied by isolated d.c. sources, composed of multiphase diode rectifiers. Among the various switching algorithms. Proposed in the literature for multi level converters, SVM is the most

promising one, which offers greatest flexibility in optimizing the switching pattern design and also well suited for digital implementation [4]. SVM with 7-segment sequence is generally used for 2-level and 3-level inverter topologies. For higher level inverter because of difficulty due to overwhelming complexity of switching sequence design and heavy relative compilation load. The compilation load have been successfully reduced by simplifying the required calculation of reference vector location duty cycle calculation. These are number of publications in the literature covering various aspects such as neutral point stabilization over modulation common mode voltage reduction SVM [5]-[13]. The main focus of this paper is on the implementation of switching sequence design. This paper presents simplified and generalized SVM algorithm with 3-segment and 7-segment switching sequence inducing over modulation operation to improve the output voltage spectrum by minimizing the device switching frequency. The performance of the proposed sequence design is analyzed through extensive simulations for five level Cascaded H-bridge inverter.

2. SPACE VECTOR MODULATION METHOD

For a typical three, five, and seven-level cascaded H-bridge inverter, with a separate dc power supply is used for each H- Bridge. Its corresponding space voltage vector diagram is illustrated in Figure 1. For the 5-level inverter, there are 96 small triangles and the vertex of each triangle represents a space vector. The hexagonal vectors can be divided into six major triangular sectors (I to VI). Only the first sector of the coordinate is used because the vectors located in the other sectors can be transformed to first sector by clockwise rotating by an angle of $k * \pi/3$, $k = (1,2,3,4,5$ for sector 2 to 6). As all the sectors are identical, only details of sector 1 is given in Figure 2.

For N-level inverter there are N^3 switching states that lie over $6(N-1)^2$ triangles. Figure 2 gives the representation of all the space vectors of the inverter in 60° co-ordinate system, the location of the reference vector is identified according to the condition given in Table 1 and all the coordinates are obtained and dwell times are calculated based on volt-second balance principle. After identifying all the switching states, out of many redundant states desired and suitable redundant states are utilized for the sequence, in the implementation of the proposed switching sequence the most desired switching state along with suitable redundant state are utilized based on the nature of the co-ordinates (g,h) of the reference vector the triangles are classified as Type-I, Type-II and Type-III.

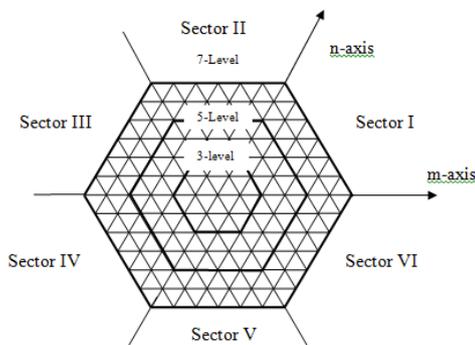


Figure 1. Voltage vectors of 3,5 and 7 - level voltage source inverters

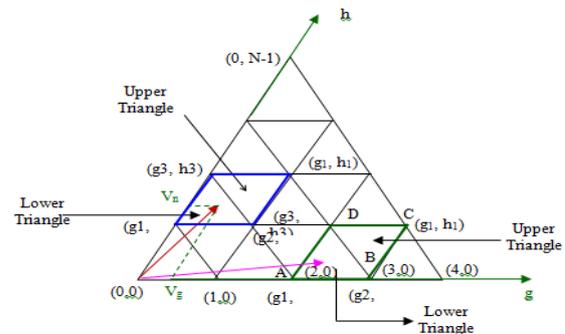


Figure 2. Voltage vectors in 60° co-ordinate system of five level inverter

Table 1. Determination of triangle of Reference Vector	
$(V_g + V_h) > (g + h + 1)$	$(V_g + V_h) \leq (g + h + 1)$
Reference Vector lies in triangle BDA	Reference Vector lies in triangle CBD
$g_1 = g + 1; h_1 = h + 1$	$g_1 = g; h_1 = h$
$g_2 = g + 1; h_2 = h$	$g_2 = g + 1; h_2 = h$
$g_3 = g; h_3 = h + 1$	$g_3 = g; h_3 = h + 1$

$$g_1 T_1 + g_2 T_2 + g_3 T_3 = T_{ref} V_g \tag{1}$$

$$h_1 T_1 + h_2 T_2 + h_3 T_3 = T_{ref} V_h \quad (2)$$

$$T_1 + T_2 + T_3 = T_{ref} \quad (3)$$

All the triangles of the space vector diagram are classified as Type-I, II, and III based on the integer coordinates of the reference vector in 60° axis and are given as:

Type-I: where both (g, h) are odd or even the three most desired states for the three vertices of (g1,h1) (g2,h2) (g3,h3) are $([SR_i, SY_i, SB_i]_{i=1,2,3})$ and one redundant state $S'_{jr} = [S'_{Rr}, S'_{Yr}, S'_{Br}]_{r=2}$ that exists for space vector (g2,h2).

Type-II: for the location of reference vector Vr is g1 is even and h1 is odd, the three most desired states are $([SR_i, SY_i, SB_i]_{i=1,2,3})$ and the redundant state $S'_{jr} = [S'_{Rr}, S'_{Yr}, S'_{Br}]_{r=1}$ for the space vector (g1,h1).

Type-III: if g1 is odd and h1 is even the most desired state $([SR_i, SY_i, SB_i]_{i=1,2,3})$ and the redundant state $S'_{jr} = [S'_{Rr}, S'_{Yr}, S'_{Br}]_{r=1}$ for the space vector (g1,h1).

3. SWITCHING SEQUENCE DESIGN

The unique switching stator in each triangle are determined using three most desired switching states $([S_{ji}]_{i=1,2,3})$ and one switching redundant state $(S'_{jr} = [S'_{Rr}, S'_{Yr}, S'_{Br}]_{r=1,2,3})$ are utilized for implement 7 segment and 3-segment switching sequence.

In conventional SVM Seven-segment switching sequence is implemented for two level or 3-level SVM but for real time because of increased computational burden because of large number of switching states of multilevel inverter implementation for higher level becomes overwhelming. In the proposed SVPWM method the optimum switching states are selected for the sequence such that there will be only one voltage level charges per commutation. The Generalised seven segment switching sequence for different types of triangles is:

Type-I: The sequence for Type-I triangles are

$$[S_{j2}] \left(\frac{T_2}{4} \right) \rightarrow [S_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S'_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{4} \right) \quad (4)$$

Type-II: The sequence for Type-II triangles are

$$[S_{j1}] \left(\frac{T_1}{4} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S'_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S_{j1}] \left(\frac{T_1}{4} \right) \quad (5)$$

Type-III: The sequence for Type-III triangles are

$$[S_{j1}] \left(\frac{T_1}{4} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S'_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S_{j3}] \left(\frac{T_3}{2} \right) \rightarrow [S_{j1}] \left(\frac{T_1}{4} \right) \quad (6)$$

Generalized three or five segment switching sequence consisting of three most desired states $[S_{ji}]_{i=1,2,3}$ of three types of triangle is expressed as

Type-1: The sequence for Type-I triangles are

$$[S_{j2}] \left(\frac{T_2}{2} \right) \rightarrow [S_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j3}] (T_3) \rightarrow [S_{j1}] \left(\frac{T_1}{2} \right) \rightarrow [S_{j2}] \left(\frac{T_2}{2} \right) \quad (7)$$

Type-II: The sequence for Type-II triangles are

$$[S_{j1}]\left(\frac{T_1}{2}\right) \rightarrow [S_{j2}]\left(\frac{T_2}{2}\right) \rightarrow [S_{j3}](T_3) \rightarrow [S_{j2}]\left(\frac{T_2}{2}\right) \rightarrow [S_{j1}]\left(\frac{T_1}{2}\right) \quad (8)$$

Type-III: The sequence for Type-III triangles are

$$[S_{j1}]\left(\frac{T_1}{2}\right) \rightarrow [S_{j3}]\left(\frac{T_3}{2}\right) \rightarrow [S_{j2}](T_3) \rightarrow [S_{j3}]\left(\frac{T_3}{2}\right)[S_{j1}]\left(\frac{T_1}{2}\right) \quad (9)$$

In three-segment switching sequence the leading and trailing state over a switches period is same as seven-segment switching sequence.

4. CALCULATION OF SWITCHING FREQUENCY

For any multilevel inverter the switching devices may not have the same device switching frequencies. The average switching frequency is defined as total number of switching of all the switches per second to the number of active devices of the inverter (F_{avg_sw})

$f_{(avg_sw)} = F_{(ideal_Avg_sw)}$. If leading state of the next sequence is equal to trailing state of the proceeding sequence.

$$F_{ideal-Avg-Sw} = \frac{(N_{ph})(N_s)fs}{N} \quad (10)$$

N_{ph} – Number of commutating phases

N_s – Number of complete switching actions ('on' and 'off' transition) per phase

N – Number of devices per commutation

fs = switching frequency

Table 2. Frequency Components for Seven-segment and Three-segment Switching Patterns for Five Level Cascaded Inverter

Frequency	Frequency components of different switching patterns	
	7-segment-switching sequence	3-segment-switching sequence
$F_{(ideal-avg-sw)}$	$\frac{(3 \times 1) \times 2fs}{24} = \frac{fs}{4}$	$\frac{2 \times \left(\frac{1}{2}\right) \times 2fs}{24} = \frac{fs}{12}$
Equivalent inverter frequency	$fs = 4F_{(ideal-Avg-sw)}$	$fs/2 = 6F_{(ideal-Avg-sw)}$

For the same ideal average switching frequency, the inverter equivalent frequency for three-segment will be double that of seven-segment sequence (50% more). For the same inverter equivalent frequency, the ideal average switching frequency for three segment is equal to two third of the corresponding seven-segment sequence number of extra commutations also increases the device frequency and average switching frequency.

5. RESULTS AND DISCUSSIONS

The performance of the above switching sequences for SVPWM technique is evaluated for Five level cascaded H- Bridge Inverter with DC input voltage of 100V. Corresponding to the modulation index of 0.87. The parameters of Induction motor for simulation are, stator resistance(R_s)=2.3Ω, rotor resistance(R_r)=2.5Ω, statorleakageinductance=0.28H, mutualinductance=0.24H, Numberofpoles=4, ratedfrequency=50Hz, Moment of inertia=0.0025J, Damping coefficient(B)=0.000124. From Table 3 it is shown that for the same inverter switching frequency the ideal average switching frequency for three segment switching sequence is 2/3 of the ideal average switching frequency for seven segment switching sequence. From Table 4 it is shown that for the same ideal average switching frequency, the inverter switching frequency for three segment switching sequence is 50% higher than that of seven segment switching sequence.

Table 3. Ideal Average Device Frequency of Seven-segment and Three-segment Switching Sequences for different Switching Frequencies

Inverter Equivalent Frequency in Hz	Ideal Average device frequency of seven-segment switching sequence $F_{(ideal-avg-sw)}$ in Hz	Ideal Average device frequency of three-segment switching sequence $F_{(ideal-avg-sw)}$ in Hz
600	150	100
900	225	150
1050	262	175
2100	525	350
3000	750	500

Table 4. Inverter Equivalent Frequency of Seven-segment and Three-segment Switching Sequences for different Ideal Average Device Switching Frequencies

Ideal Average device frequency of seven-segment switching sequence $F_{(ideal-avg-sw)}$ in Hz	Inverter Equivalent Frequency of seven-segment switching sequence $F_{(ideal-avg-sw)}$ in Hz	Inverter Equivalent Frequency of three-segment switching sequence $F_{(ideal-avg-sw)}$ in Hz
150	600	900
225	900	1350
262	1050	1572
525	2100	3150
750	3000	4500

Figure 3 gives the line voltage spectrum over broader range (12500Hz) with inverter switching frequency of 2100Hz. The harmonics appear as side band around inverter equivalent frequency. The ideal average device switching frequency being 525Hz. The THD obtained for seven-segment sequence is 19.41%. Figure 4 gives the line voltage spectrum over broader range (12500Hz) with inverter switching frequency of 3150Hz. For the same ideal average device switching frequency (525), the inverter is simulated for three-segment switching sequence. The harmonics appear as side band around inverter equivalent frequency of 3150Hz. The magnitude of harmonics is reduced to larger amount giving lesser value of THD which is 16.32%. Figure 5 shows the line voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching sequence with switching frequency of 4745Hz.

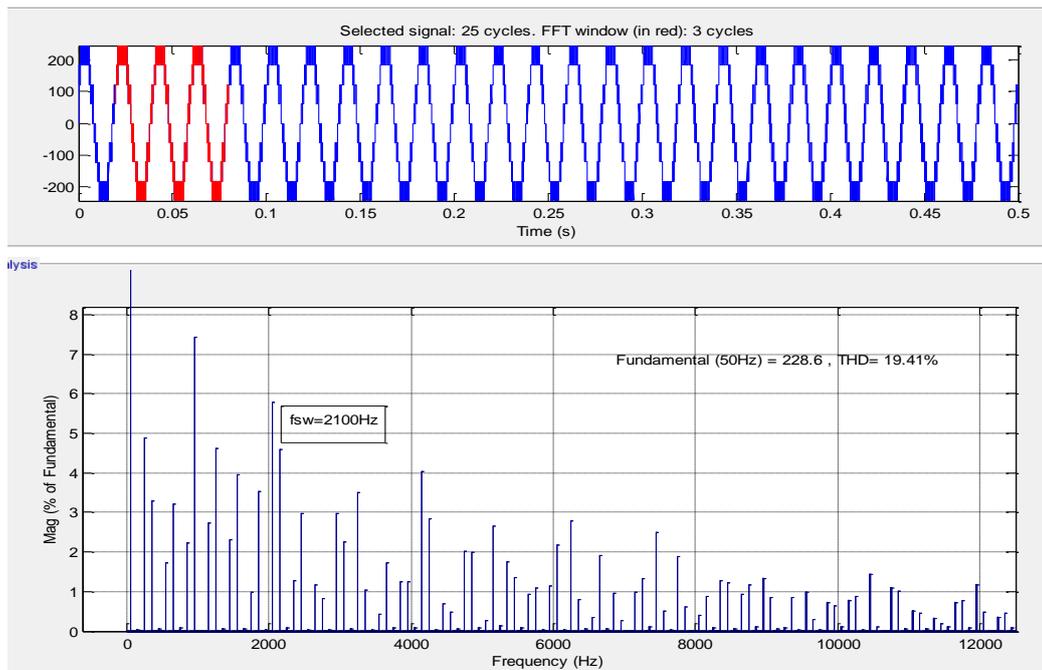


Figure 3. Line Voltage spectrum of five level cascaded inverter over 12.5KHz with seven-segment switching sequence

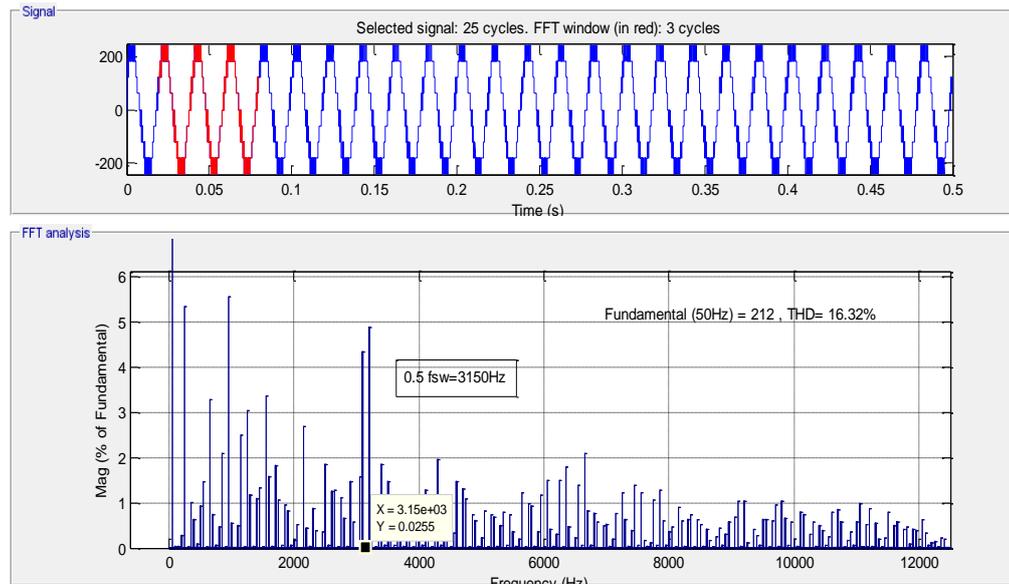


Figure 4. Line Voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching sequence for switching frequency of 3150Hz

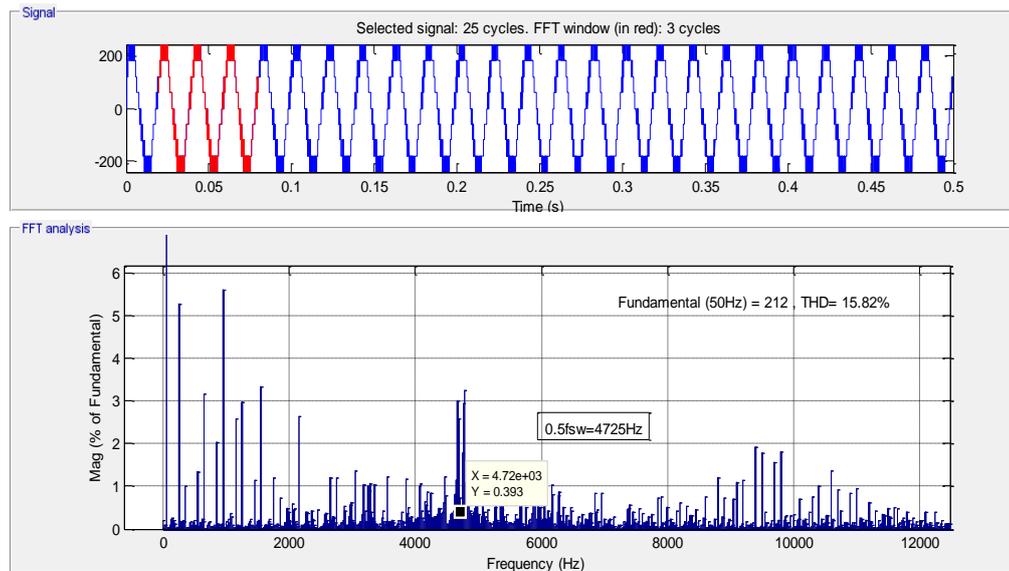


Figure 5. Line Voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching sequence with switching frequency of 4745Hz

Figure 6 gives the line voltage spectrum over broader range (12500Hz) with inverter switching frequency of 1125Hz. The harmonics appear as side band around inverter equivalent frequency (switching frequency). The THD obtained is 16.92%.

Figure 7 gives the line voltage spectrum over broader range (12500Hz) with inverter switching frequency of 750Hz. For the same ideal average device switching frequency (187Hz), the inverter is simulated for seven-segment switching sequence. The harmonics appear as side band around inverter equivalent frequency of 750Hz. From Figure 8 it is shown that the phase voltage THD increases at higher inverter frequencies in case of three-segment switching pattern compared to seven-segment switching pattern. Table 5 shows the THD of line phase and current of five level cascaded inverter for seven-segment

switching sequence. Table 6 shows the THD of line phase and current of five level cascaded inverter for three-segment switching sequence.

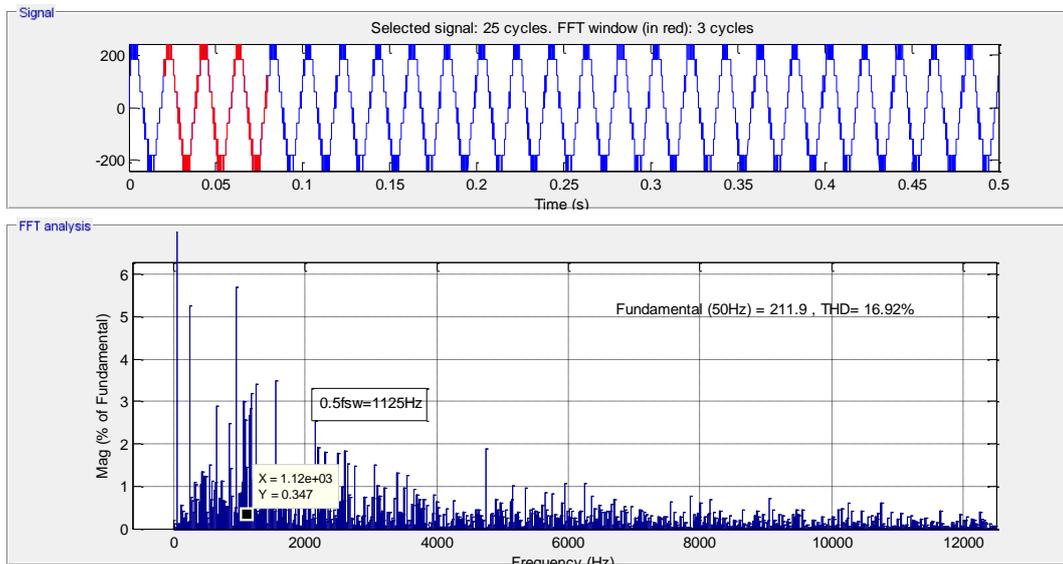


Figure 6. Line Voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching sequence with switching frequency of 1125Hz

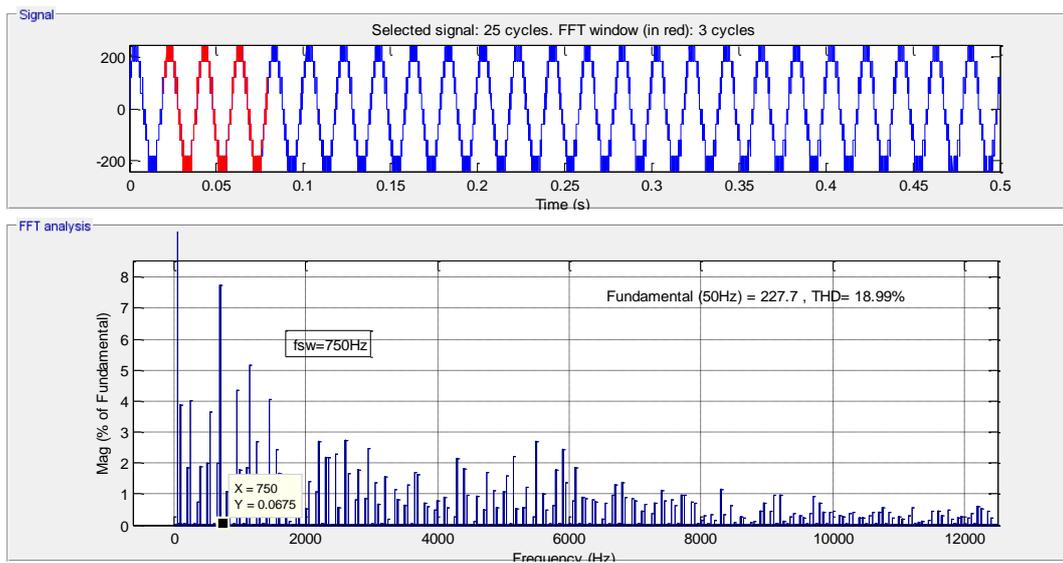


Figure 7. Line Voltage spectrum of five level cascaded inverter over 12.5KHz with seven-segment switching sequence with switching frequency of 750Hz

Table 5. THD of Line Phase and current of five level Cascaded Inverter for Seven-segment Switching Sequence

Inverter switching Frequency	V _L Line voltage THD As a % of fundamental	V _{Ph} Line voltage THD As a % of fundamental	I(current) THD As a % of fundamental
600	12.04	23.51	5.39
900	12.62	33.41	5.07
1050	11.29	27.08	5.66
2100	11.39	29.03	5.04
3000	10.34	26.64	5.35
4200	10.24	26.73	5.46

Table 6. THD of Line Phase and Current of Five Level Cascaded Inverter for Three-segment Switching Sequence

Inverter switching Frequency	V_L Line voltage THD As a % of fundamental	V_{Ph} Line voltage THD As a % of fundamental	I(current) THD As a % of fundamental
600	10.51	30.21	4.22
900	9.50	29.33	4.32
1050	9.66	28.93	4.42
2100	8.37	28.05	4.47
3000	7.84	27.85	4.43
4200	7.95	27.35	4.45

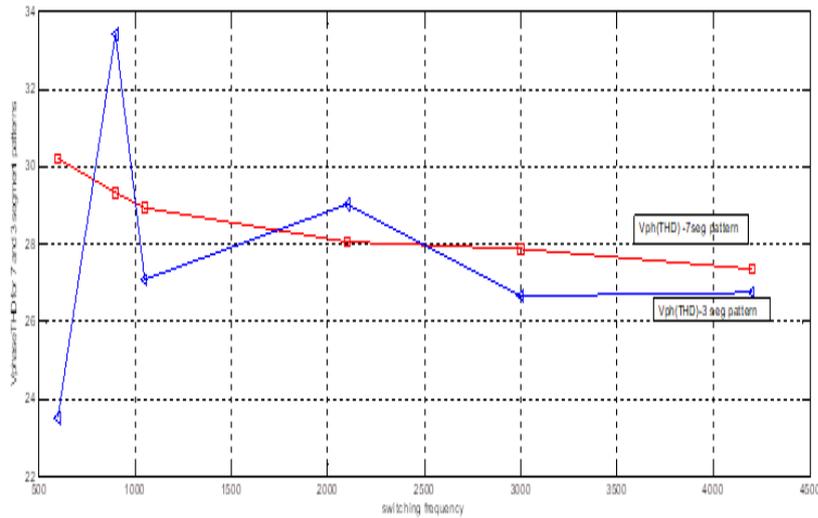


Figure 8. Phase Voltage THD at various inverter frequencies for 7- segment and 3- segment switching Patterns

From Figure 9 it is shown that the Line voltage THD and current THD decreases at higher inverter frequencies in case of three- segment switching pattern compared to seven – segment switching pattern.

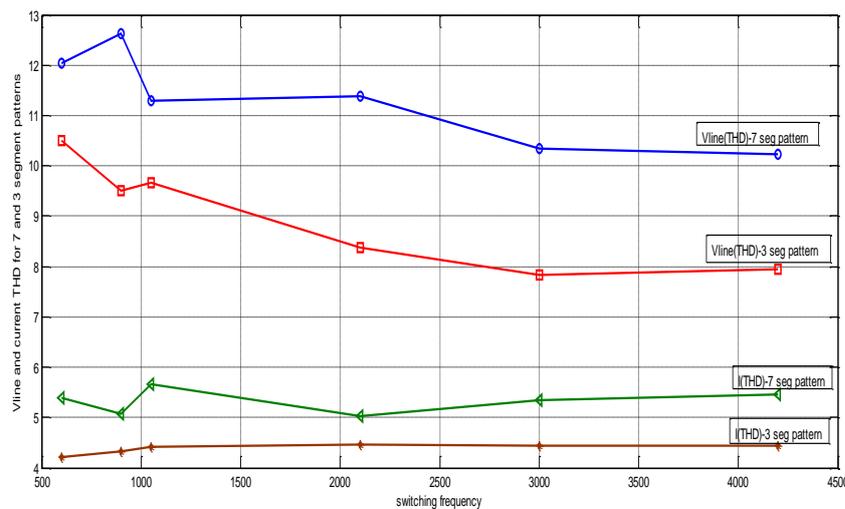


Figure 9. Line Voltage and current THDs at various inverter frequencies for 7- segment and 3- segment switching patterns

6. CONCLUSION

This paper presents general SVPWM technique based on seven-segment and three-segment online switching patterns for N-level inverter. The two switching patterns are simulated for five level cascaded inverter. One of the important feature of this technique is that, out of large number of switching states of the five level inverter, the desired switching states and most suitable redundant states are selected for the both sequence patterns such that, the technique is implemented online with no need of lookup table. In the three-segment switching sequence, the inverter equivalent frequency is 50% higher than that of seven-segment, harmonics appear as sideband around high inverter frequency, and the magnitude of lower order harmonics is reduced for three segment giving lesser value of Line voltage and current THDs when compared to that of seven-segment switching pattern.

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