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Design and Implementation of Low Power Multiplier Using Proposed Two Phase Clocked Adiabatic Static CMOS Logic Circuit

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ABSTRACT

This paper presents a design and implementation of 2*2 array and 4*4 array multiplier using proposed Two Phase Clocked Adiabatic Static CMOS logic (2PASCL) circuit. The proposed 2PASCL circuit is based on adiabatic energy recovery principle which consumes less power. The proposed 2PASCL uses two sinusoidal power clocks which are 180^0 phase shifted with each other. The measurement result of 2*2 array proposed 2PASCL multiplier gives 80.16 % and 97.67 %power reduction relative to reported 2PASCL and conventional CMOS logic and the measurement result of 4*4 array proposed 2PASCL multiplier demonstrate 32.88 % and 82.02 %power reduction compared to reported 2PASCL and conventional CMOS logic. Another advantage of the proposed circuit is that it gives less power though the number of transistors in proposed and reported 2PASCL circuit is same. From the result we conclude that proposed 2PASCL technology is advantageous to application in low power digital systems, pacemakers and sensors. The circuits are simulated at 180nm technology mode.

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1. INTRODUCTION

Power reduction has now become a key concern for the design of portable and wireless devices. In the design of digital circuits which uses complementary metal oxide semiconductor, the power reduction can be achieved by scaling down the transistor threshold voltage in accordance with supply voltage [1]. It will impose limitation as reducing the threshold voltage below a certain limit will increase leakage current. Switching event in CMOS circuits is another cause of power dissipation which can be decrease by reducing the switching activity [2]. Power dissipation in CMOS circuits during charging and discharging of node capacitances is given by the

$$E = C_L V_{DD}^2 \quad (1)$$

from the equation (1) it is apparent that energy can be reduced by reducing supply voltage and decreasing switching activity in CMOS circuits [3]-[4].

Various other techniques are available for low power reduction which includes reversible logic [5], GDI logic [6] and domino logic [7] at circuit level. But taking into account the limitations of power reduction in CMOS circuits. A novel approach called Adiabatic computing have been proposed [8],[9] which uses the

energy recovery principle. it uses time varying voltage supply instead of constant supply [10] as that of used in CMOS circuits. The varying supply voltage charge the circuit during specific phases and supplied charge is recovered during discharging event. The equation for the energy dissipation for Adiabatic logic is given as

$$E = \left(\frac{RC_L}{T} \right) C_L V_{dd}^2 \quad (2)$$

Where R is resistor in charging and discharging path, C_L is the load capacitance, Vdd is supply voltage, T is total time required for charging and discharging the node capacitance. By increasing the time T, energy can be reduced. For various low power applications many adiabatic logic circuits with different clocking scheme have been proposed and analyzed [8]-[9].

In this paper, we focused on Two Phase Clocked Adiabatic Static CMOS logic (2PASCL) circuit [11] because of its lower switching activity. We proposed improved structure for two phase clocked adiabatic static CMOS logic (2PASCL). power dissipation of the proposed 2PASCL is less compared to the reported one. It utilizes two sinusoidal power clock which are 180^0 phase shifted with each other.

The rest of this paper is organized as follows. Section 2 describes proposed and reported 2PASCL structure. In section 3 we designed the half adder, full adder ,nand gate , 2*2 and 4*4 array multiplier using proposed logic style .Its simulation results and power dissipation is shown. As proposed logic gives less power dissipation, the comparative power dissipation is summarized in section 4. Section 5 includes the conclusion.

2. PROPOSED AND REPORTED TWO PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC (2PASCL) CIRCUIT

2.1. Reported Two Phase Clocked Aadiabatic Static CMOS Logic (2PASCL)

Two phase clocked adiabatic static CMOS logic [12]-[14] utilizes the principle of adiabatic switching in which power dissipation occurs through the threshold voltage and transistor resistance. Figure 1 shows the structure of 2PASCL. The circuit uses two sinusoidal power clock which are 180^0 phase shifted to each other nodes.

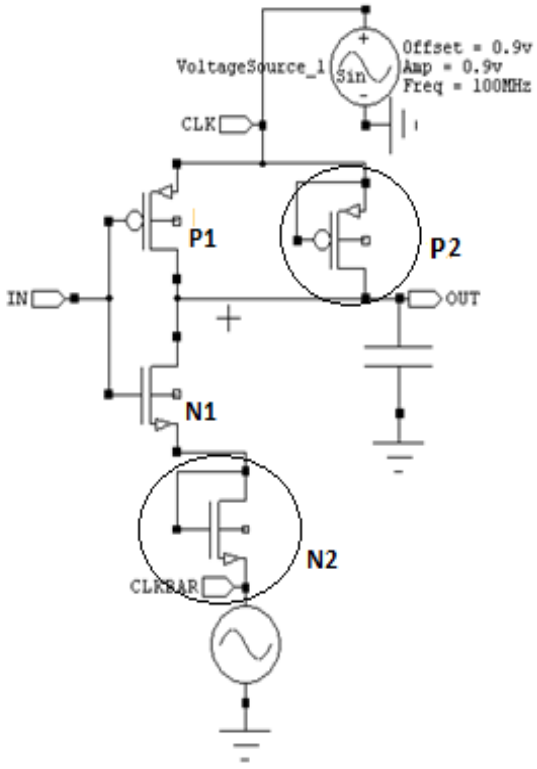

Figure 1. Structure of 2PASCL

The operation is performed in two phases Evaluation and Hold phase. The charging path is provided by transistor P1 and discharging path is provided by transistor P2 and N1, N2. The expression for energy dissipation is given as

$$E = E_{charging(P1)} + E_{Discharging(P2)} + E_{Discharging(N1,N2)}$$
$$= 0.5C_L V_{tp}^2 + 0.5C_L V_{clk} V_{tp} + 0.5C_L (V_{clkbar} - V_{tn}) V_{tn}$$
$$= 0.5C_L \{V_{tp}^2 + V_{clk} V_{tp} + (V_{clkbar} - V_{tn}) V_{tn}\}$$

Where C_L is the load capacitance, V_{tp} and V_{tn} are the threshold voltages of PMOS and NMOS transistor. Vclk and V_{clkbar} are sinusoidal supply voltages which are 180^0phase shifted with each other and peak to peak voltage of 1.8v. Figure 2 shows waveform of 2PASCL inverter circuit. It gives output low when input is high and it passes the clock signal for input logic at low. The proposed structure tries to keep the output logic at high when input is low instead of passing the clock signal as in case of reported 2PASCL.

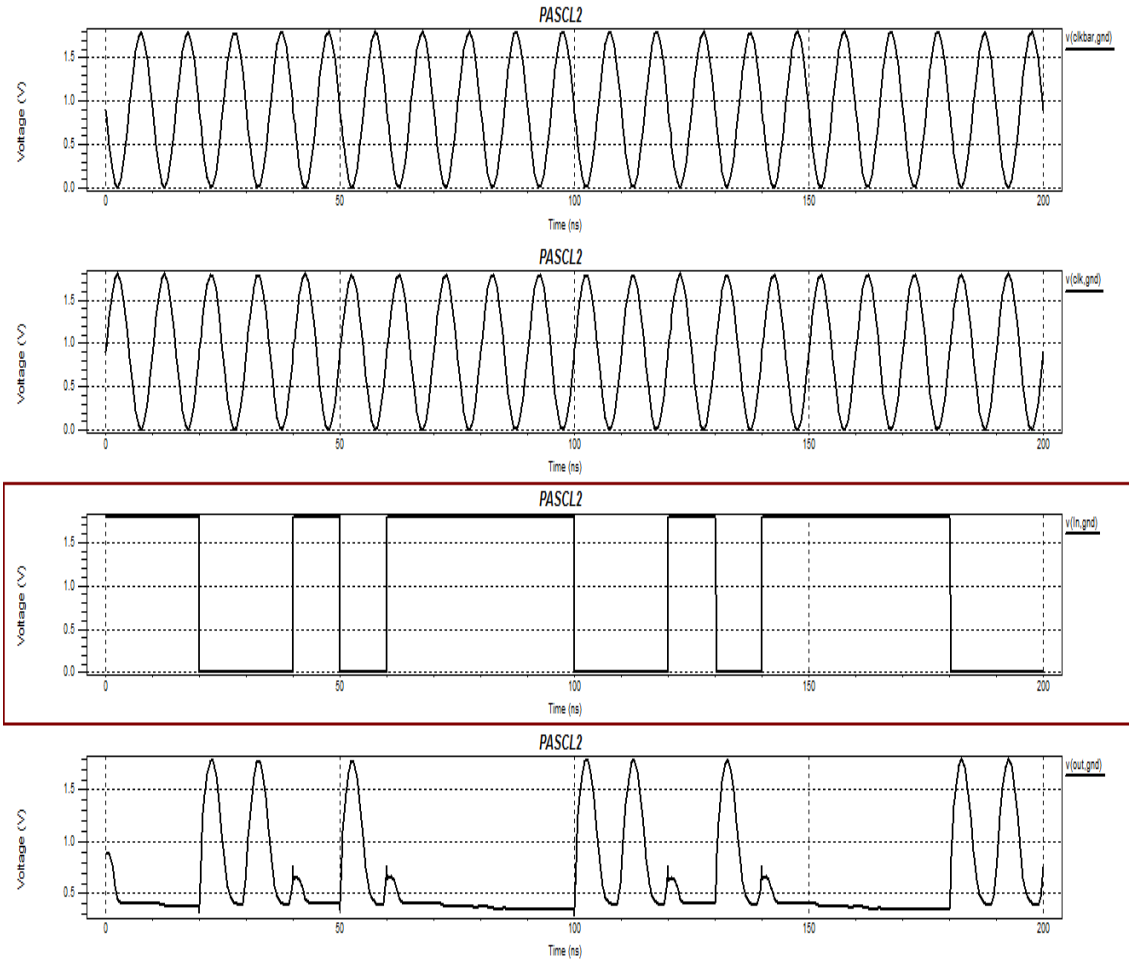

Figure 2. Simulation Waveform for 2PASCL Inverter

2.2. Proposed Two Phase Clocked Aadiabatic Static CMOS Logic (2PASCL)

The Proposed 2PASCL [15] structure is shown in Figure 3. The gate terminal of transistor N2 is connected to CLK and gate terminal of P2 is connected to CLKBAR. The operation of the circuit is performed in two phases i.e. Evaluation phase and Hold phase.

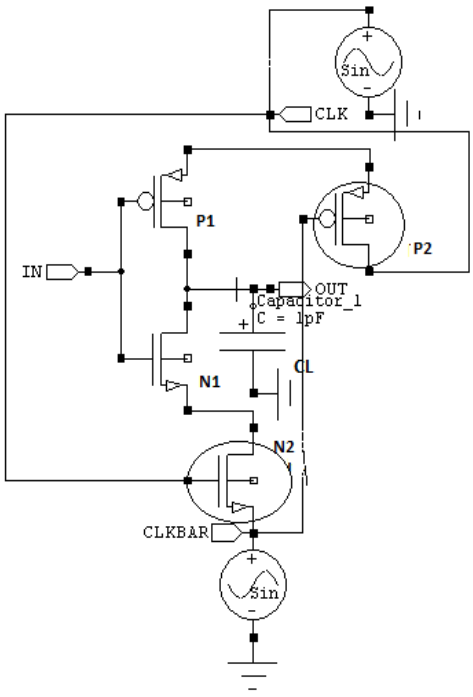

Figure 3. Structure of proposed 2PASCL

Circuit operation:

1. Evaluation phase: In Evaluation phase CLK goes high and CLKBAR goes low. When P1 transistor is on and output is at logic low then C_L is charged through P1 transistor and output reaches at logic high. When output is high, Output load capacitor discharges through transistor N1 and N2 causes the output at low level.
2. Hold phase: In hold phase CLK goes low and CLKBAR goes high no transitions occur as both the transistor P2 and N2 will be off. Due to the hold phase, dynamic switching is reduced and hence energy dissipation is reduced.

The Expression for the energy dissipation is given as

$$E = E_{charging(P1)} + E_{Discharging(N1,N2)}$$
$$= 0.5C_L V_{tp}^2 + 0.5C_L (V_{clkbar} - V_{tn}) V_{tn}$$
$$= 0.5C_L \{V_{tp}^2 + (V_{clkbar} - V_{tn}) V_{tn}\}$$

Thus from the expression of energy dissipation itself it is clear that in the proposed structure energy dissipation through transistor P2 will not occur as in the reported structure.

Figure 4 shows simulation waveform for proposed 2PASCL inverter at clock frequency of 100 Mhz and input signal frequency at 50 MHz. The proposed Inverter circuit saves 40.74% power over reported 2PASCL and 88.71% power over conventional CMOS inverter at clock frequency of 100 MHz and input signal frequency of 50 MHz.

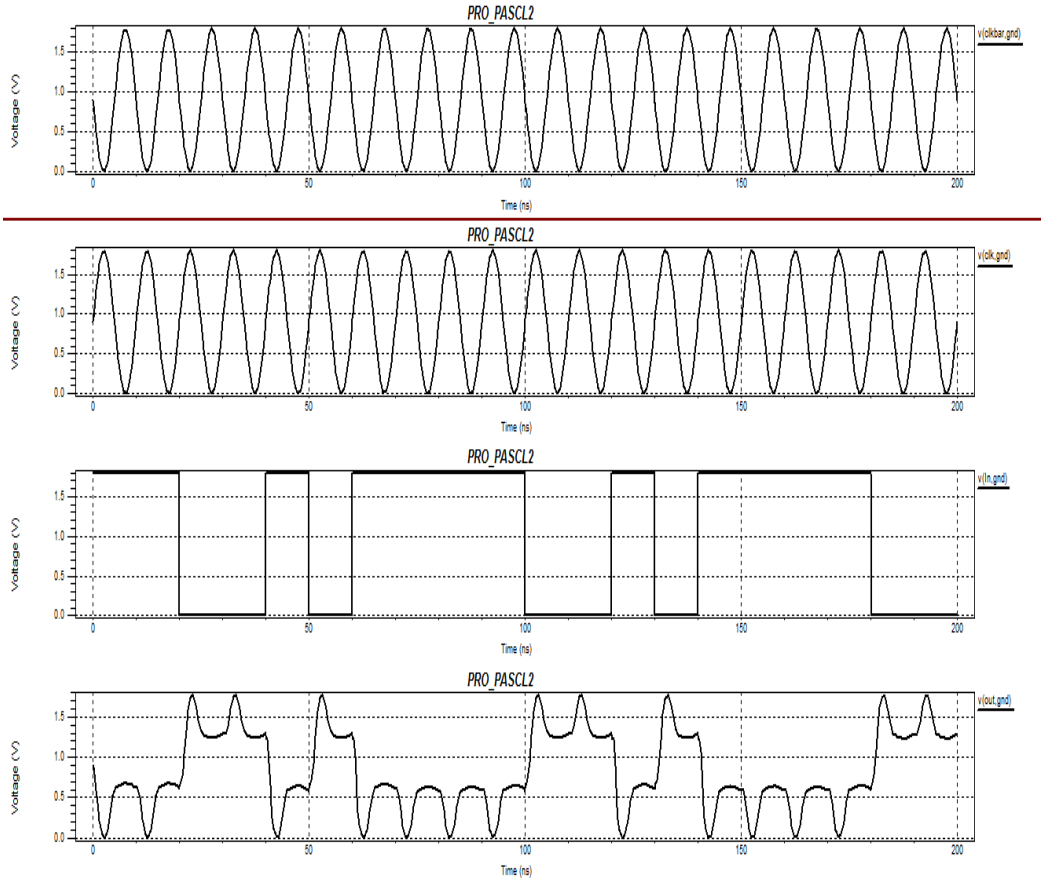

Figure 4. Simulation Waveform for proposed 2PASCL Inverter

3. MULTIPLIER STRUCTURE

First we designed the circuits which are required for multiplier structure such as NAND, half adder, full adder using both the logic style.

3.1. Half Adder

The design of half Adder using NAND gate is shown in Figure 5. A and B are the inputs and sum and carry are the output of Half Adder. The simulation waveform of half adder using proposed 2PASCL is shown in Figure 7. The proposed Half Adder circuit saves 65.92% power over reported 2PASCL and 93.49% power over conventional CMOS logic at clock frequency of 100MHz and input signal frequency of 50 MHz. Thus proposed 2PASCL Half adder shows improvement of 13% power conventional CMOS logic compared with reported 2PASCL.

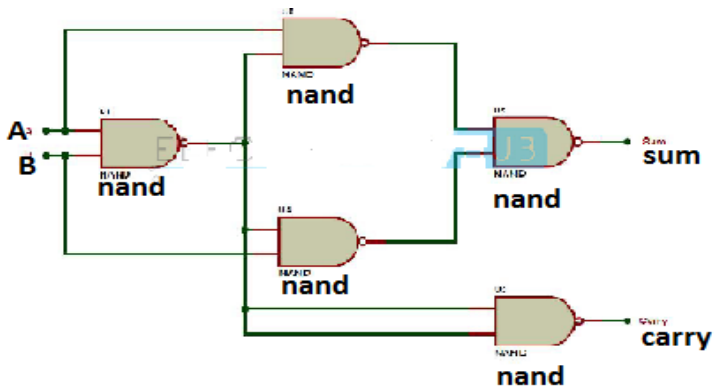

Figure 5. Block diagram of Half Adder

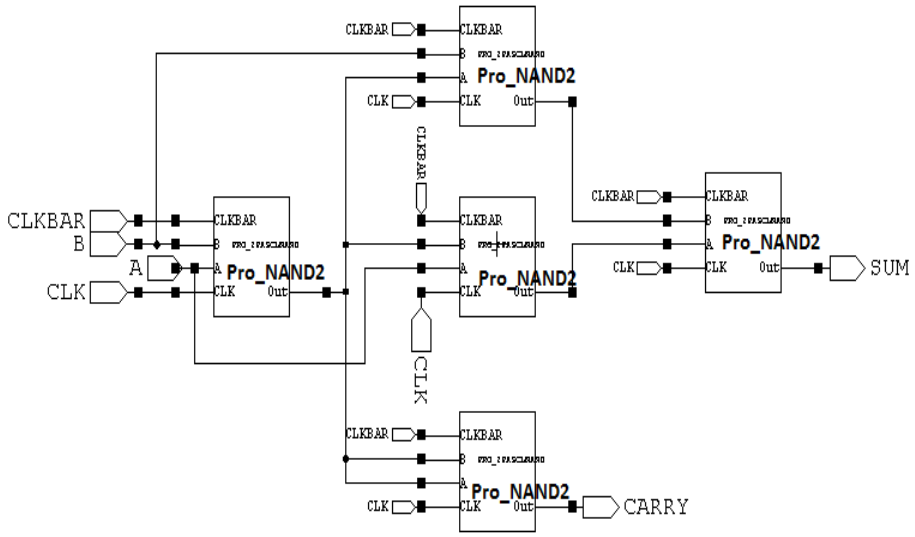

Figure 6. Design of Half Adder gate using Proposed 2PASCL

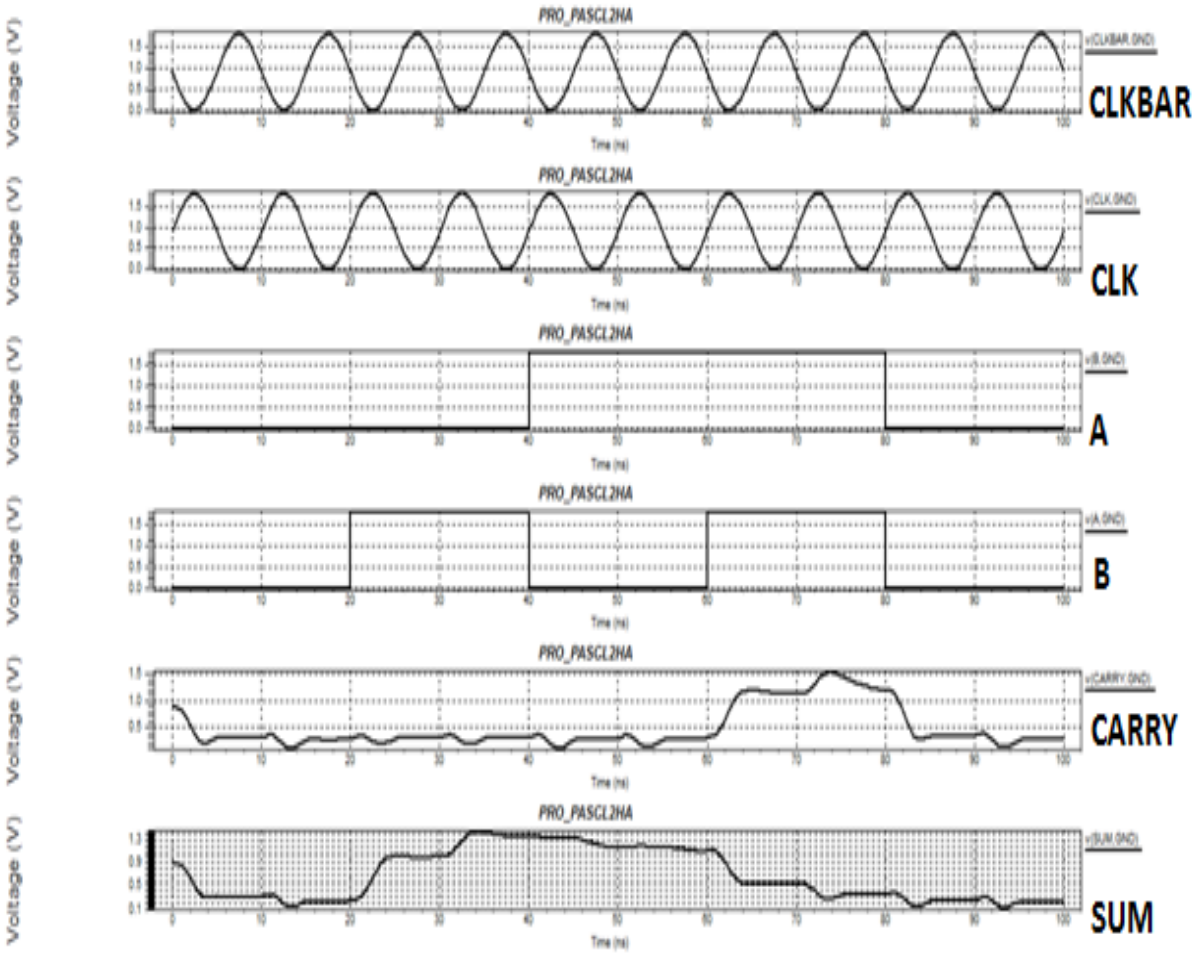

Figure 7. Simulation Waveform for proposed 2PASCL Half Adder

3.2. Full adder

The design of Full Adder is shown in Figure 8. Two half adders with addition of an OR gate to combine their carry output Full adder is designed. A, B and Cin are three inputs sum and carry are the output of Full adder circuit. The proposed Full Adder circuit saves 78.35% power over reported 2PASCL and 88.63% power over conventional CMOS logic at clock frequency of 100MHz and input signal frequency of 50 MHz. Thus proposed 2PASCL Full Adder shows improvement of 41.15% power conventional CMOS logic compared with reported 2PASCL.

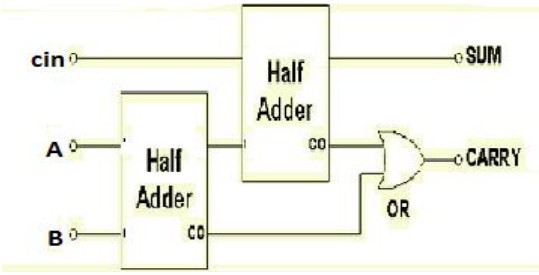

Figure 8. Block diagram of Full Adder

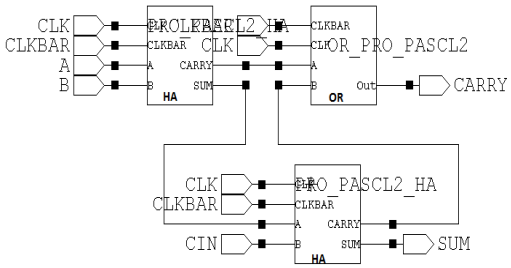

Figure 9. Design of Full Adder using Proposed 2PASCL

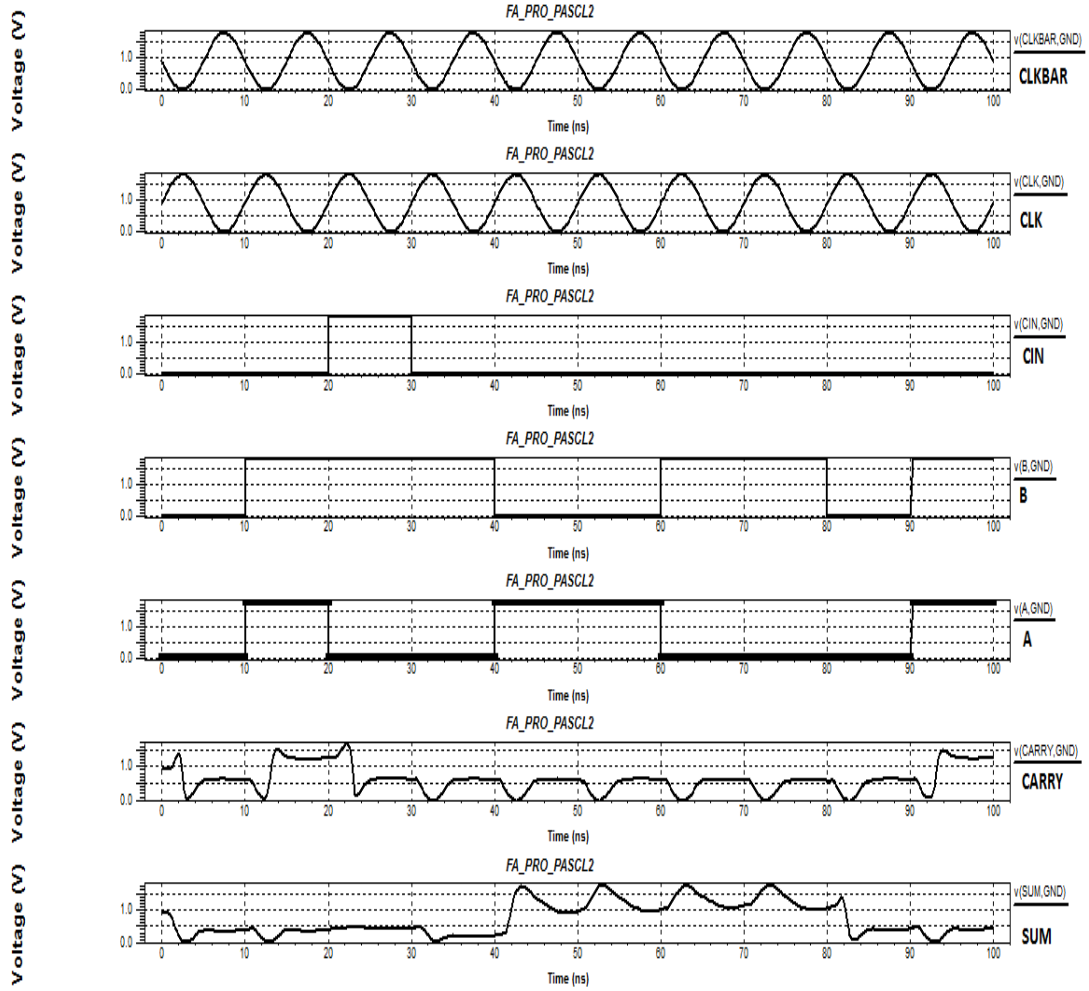

Figure 10. Simulation Waveform for proposed 2PASCL Full Adder

3.3. 2*2 Array Proposed 2PASCL Multiplier

Multiplication is one of the basic arithmetic operation and multiplier is fundamental functional unit in most of the processors. Multiplier can be Array or parallel multiplier [16]-[17]. Both the type of multiplier possesses high execution speed but the array multiplier has regular structure and occupies less space compared with parallel multiplier. Figure 11 structure of array multiplier using half adder and AND gate. Multiplier is designed using proposed logic style shown in figure 12, reported logic and conventional logic.for 2*2 array multiplier inputs are a0,a1 and b0,b1 and p0,p1,p2,p3 are the outputs. For the Input 1111, output is 1001 which can be verified from the simulation results shown in Figure 13.

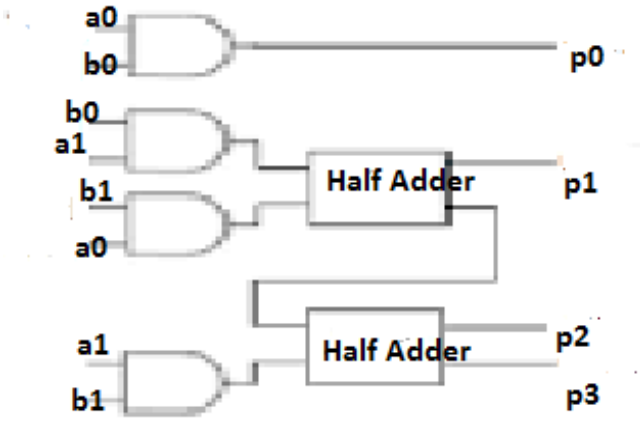

Figure 11. Block diagram of 2*2 Array Multiplier

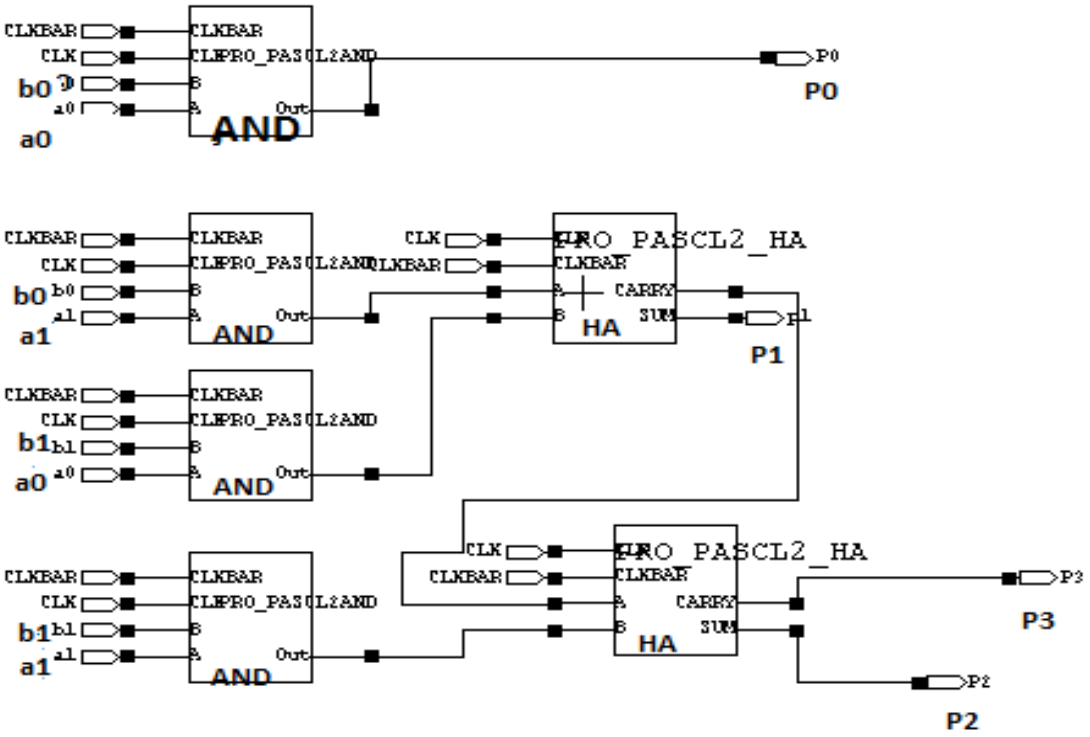

Figure 12. Design of 2*2 Array Multiplier using Proposed 2PASCL

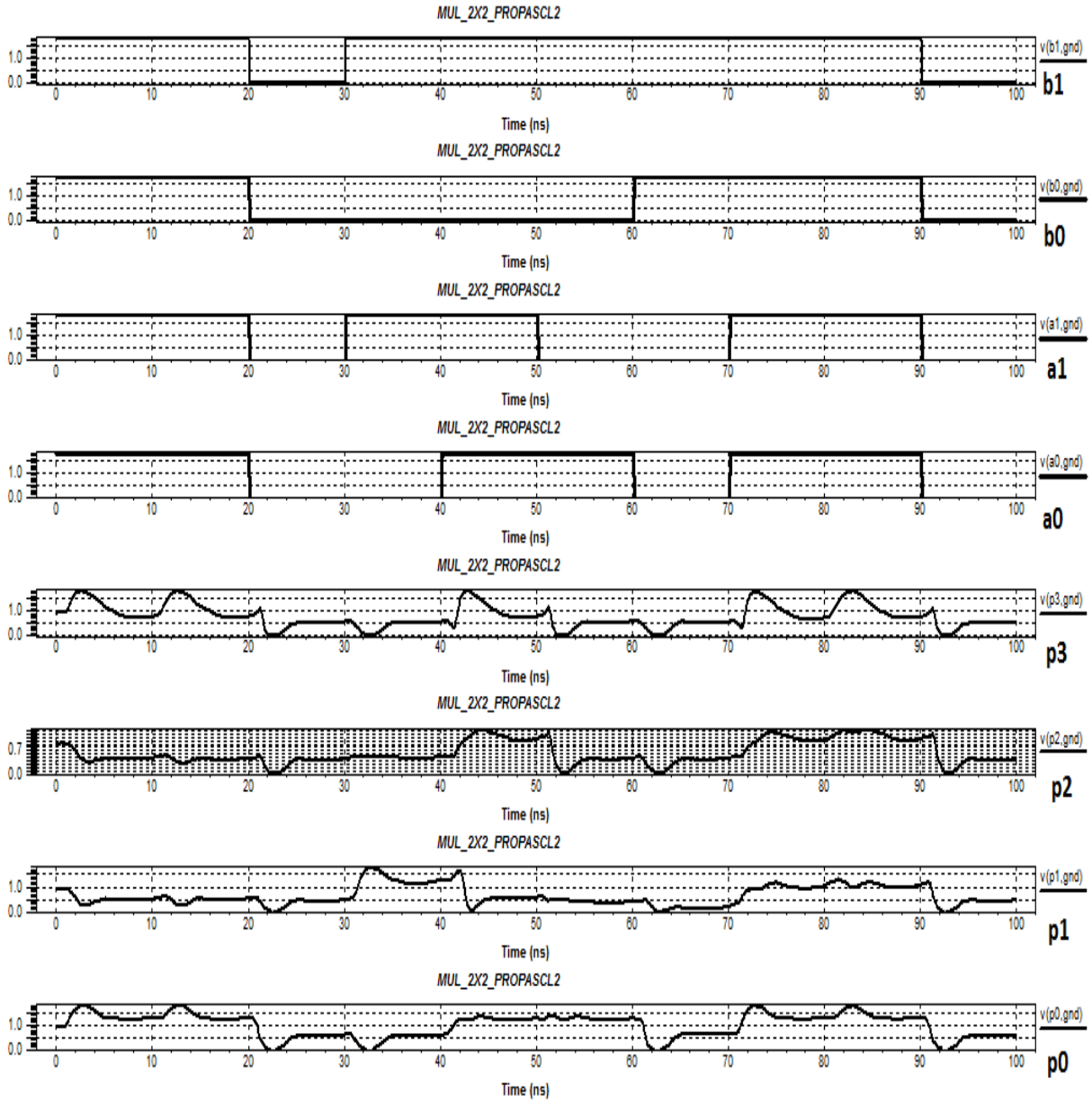

Figure 13. Simulation Waveform for proposed 2PASCL 2*2 Array Multiplier

3.4. 4*4 Array Proposed 2PASCL Multiplier

As shown in Figure 14, the 4_4-bit array 2PASCL multiplier consists of 16 ANDs, six full adder logic circuits, and four half adder logic circuits. This 4*4 bit array multiplier [18] is designed using three logic style i.e. CMOS logic, 2PASCL logic and Proposed 2PASCL logic. The proposed circuit implementation is shown in Figure 15 and Figure 16 demonstrates the simulation result of array multiplier. At the output load capacitance varying from 0.01pF to 0.1pF is set for p0 to p7. The proper working of the circuit can be demonstrated from simulation result shown in Figure 16, however signal glitches will ocuur at p4. The circuit consists of same transistor size and W/L ratio 180nm/180nm i.e. 1.the supply voltage is 1.8v. and two sinusoidal clock signals are used which are 180^0 phase shifted with each other.

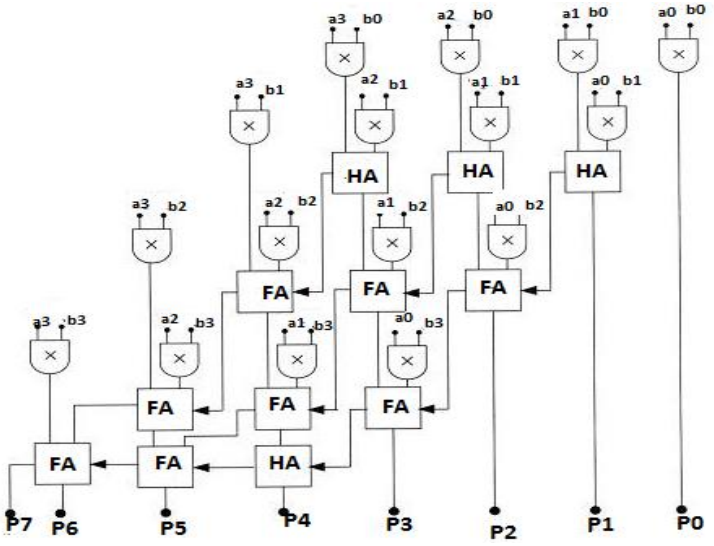

Figure 14. Block diagram of 4*4 Array Multiplier

Figure 15. Design of 4*4 Array Multiplier using Proposed 2PASCL

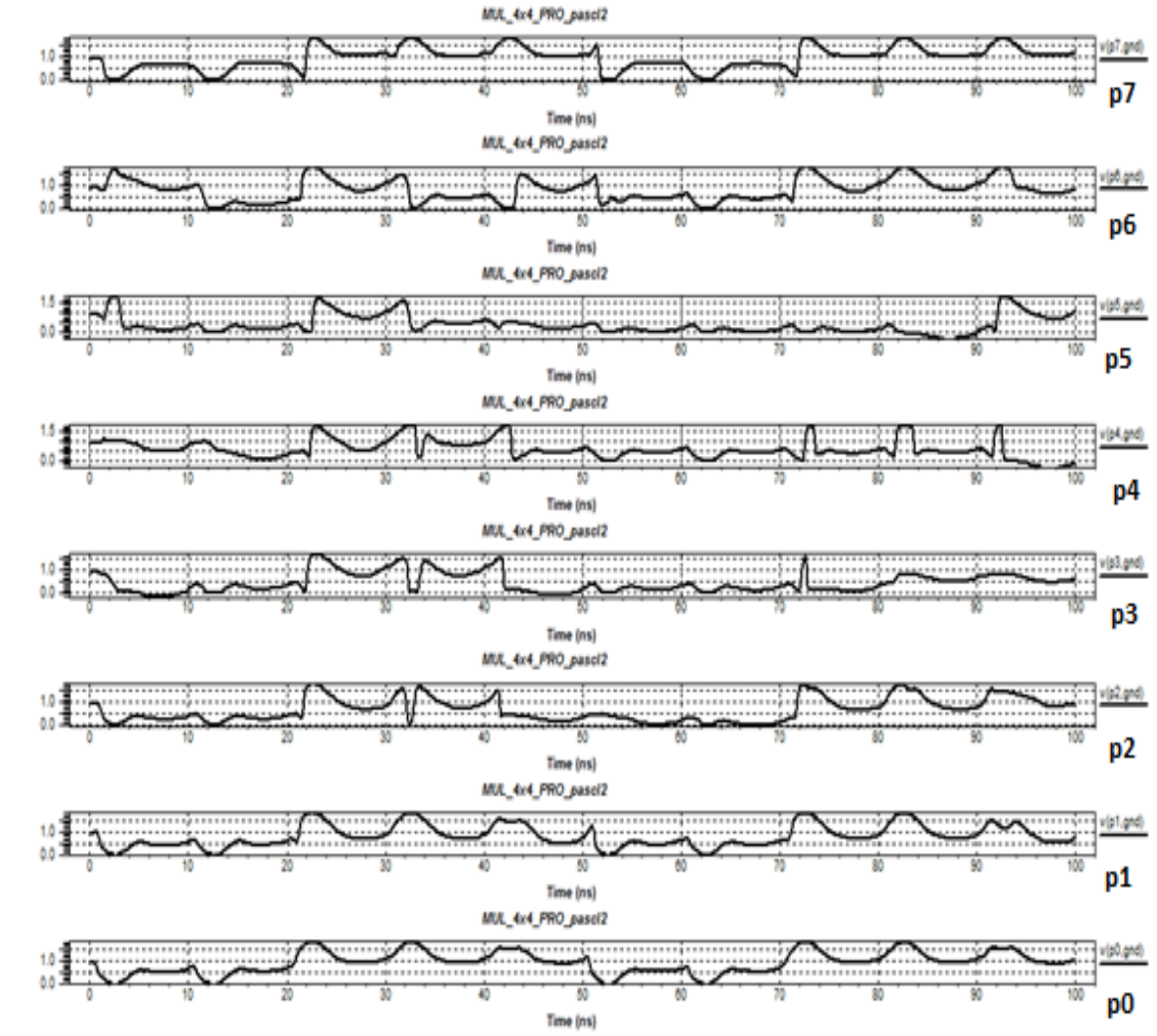

Figure 16. Simulation Waveform for proposed 2PASCL 4*4 Array Multiplier

The proposed 2PASCL 4*4 bit array multiplier gives 32.88% power reduction compared to report 2PASCL multiplier and 82.02% reduction compared to conventional CMOS logic at clock frequency of 100MHz and input signal frequency of 50 MHz. Thus proposed multiplier shows improvement of 8.81% over conventional CMOS logic compared with reported 2PASCL.

The proposed 4×4-bit array 2PASCL multiplier only shows a good logic functionality of up to 200 MHz transition frequency. We observe that for transition frequency of more than 200 MHz some signal degradations will occur. This is due to the charging time T which is much slower than conventional CMOS. T is also proportional to RC_L i.e. the longer the path, the larger T is needed. These input frequencies are adequate for the applications such as low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.

4. RESULT AND ANALYSIS

The comparative power analysis has been done for the half adder, full adder, 2*2 bit array multiplier and 4*4 bit array multiplier for the input frequency of 50MHz and clock signal frequency of 100MHz for the signal transition from 1ns to 100ns. The Table 1 shows comparative power analysis of the circuits implemented using the three logic style i.e. CMOS logic, 2PASCL logic and proposed 2PASCL logic and its graphical analysis is shown in Figure 17.

Table 1. Comparative Power Analysis

Device	Power dissipation(uW)		
	CMOS	*2PASCL[14]*	*Proposed 2PASCL*
AND Gate	0.849	0.409	0.134
HALF ADDER	63.5	12.12	4.13
FULL ADDER	72.59	38.12	8.25
2*2 MULTIPLIER	45.32	5.416	1.054
4*4 MULTIPLIER	381.66	102.22	68.60

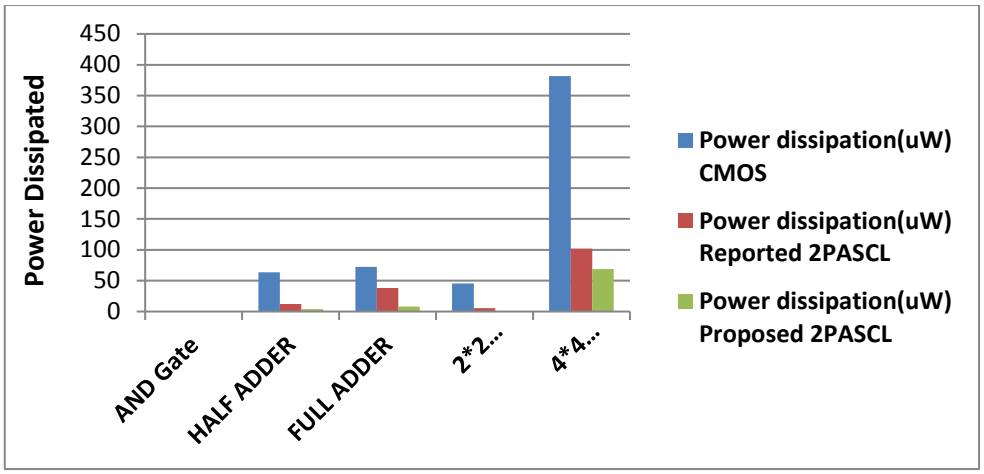

Figure 17. Comparative power analysis at clock frequency of 100MHz

5. CONCLUSION

Thus we designed and simulated a 4×4-bit array multiplier using three logic styles. The proposed logic designs are compared with the reported one and conventional CMOS logic style. The proposed 2PASCL 2*2 bit multiplier is 80.53% and 97.67% power efficient over reported 2PASCL multiplier and CMOS multiplier. The reported 2*2 PASCL multiplier is 88.04% power efficient compared to CMOS multiplier. Thus the proposed structure has achieved efficiency of 9.63%. The proposed 2PASCL 4*4 bit multiplier is 32.88% and 82.02% power efficient over reported 2PASCL multiplier and CMOS multiplier. The reported 4*4 PASCL multiplier is 73.21% power efficient compared to CMOS logic multiplier. Thus the proposed structure has achieved efficiency of 8.99%. Thus power consumption in the 2PASCL multiplier is considerably less than that in a CMOS. We believe that the proposed adiabatic logic circuit is advantageous for ultra low energy computing applications. As for our future work, we will further evaluate the cause of the signal glitches in 2PASCL.

REFERENCES

[1] A. Bellaouar and M. Elmasry, "Low-Power Digital VLSI Design: Circuit and Systems," Norwell, MA, Kluwer, 1995.
[2] Chandrakasan and R. Brodersen, "Minimizing power consumption in digital CMOS circuits," *Proc. IEEE*, vol. 83, pp. 498-523, 1995.
[3] J. S. Denker, "A review of adiabatic computing," *Proc. 1994 Symp. Low Power Electronics/Digest of Technical Papers, San Jose, CA*, pp. 94-97, 1994.
[4] J. Rabey and M. Pedram, "Low Power Design Methodologies," Norwell, MA, Kluwer, 1996.
[5] S. Thakral, *et al.*, "Implementation and Analysis of Reversible logic Based Arithmetic Logic Unit," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol/issue: 14(4), pp. 1292-1298, 2016.
[6] B. H. Nagpara, "A 45 nm 6 Bit Low Power Current Steering Digital to Analog Converter Using GDI Logic," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 16(1), pp. 46-51, 2015.
[7] J. Muralidharan and P. Manimegalai, "Current Comparison Domino based CHSK Domino Logic Technique for Rapid Progression and Low Power Alleviation," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 7(5), pp. 2468-2473, 2017.
[8] W. C. Athas, *et al.*, "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. Very Large Scale Integration Syst.*, vol/issue: 2(4), pp. 398-407, 1994.

[9] L. Svensson, "Adiabatic switching," in A. Chrakasan and R. Brodersen, "Low Power Digital CMOS Design," Norwell, MA, Kluwer Academic, 1995.
[10] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," *IEEE Journal o Solid-State Circuits*, vol/issue: 30(3), pp. 311-315, 1995.
[11] N. Anuar, *et al.*, "Two phase clocked adiabatic static CMOS logic," *Proc. IEEE SOC 2009*, pp. 83-86, 2009.
[12] N. Anuar, *et al.*, "Two phase clocked adiabatic static CMOS logic and its logic family," *J. Semiconductor Technology and Science*, vol/issue: 10(1), pp. 1-10, 2010.
[13] N. Anuar, *et al.*, "4-bit ripple carry adder of two-phase clocked adiabatic static CMOS logic," *Proc. IEEE TENCON 2009, THU4.P.16*, 2009.
[14] N. Anuar, *et al.*, "Fundamental logics based on two phase clocked adiabatic static logic," *Proc. IEEE ICECS 2009*, pp. 503-506, 2009.
[15] M. L. Keote and P. T. Karule, "Improved Two Phase Clocked Adiabatic Static CMOS Logic Circuit," in *European Journal of Advances in Engineering and Technology*, vol/issue: 4(5), pp. 319-325, 2017.
[16] C. S. Wallace, "A suggestion for a fast multiplier," in *IEEE Trans. On Electronic Computers*, vol. EC-13, pp. 14-17, 1964.
[17] N. A. Nayan, *et al.*, "LSI implementation of a low-power 4*4-bit array two-phase clocked adiabatic static CMOS logic multiplier," *Microelectronics Journal*, vol. 43, pp. 244-249, 2012.
[18] C. S. Wallace, "A suggestion for a fast multiplier," *IEEE Trans. On Electronic Computers*, vol. EC-13, pp. 14-17, 1964.

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Dr. P.T. Karule was born in India and persued his B. E. (Electronics and Power) from Govt. College of Engineering, Amravati. in 1986, M.Tech. (Electronics Engineering) from VNIT, Nagpur in 1992 and Ph.D. in the area of Medical Image Processing & Neural Network from Amravati University in 2010. He has 25 years of teaching experience. His area of expertise is microprocessors and embedded system At present he is Professor in Department of Electronics Engineering of YCCE and also looking after administrative work of autonomous YCCE as Registrar. Earlier he was Head of Department of ECE, YCCE; during his tenure he started the popular activity of workshop series for students on current technologies with hands-on practice in summer & winter vacation to enhance the employability. He had also worked as Dean Industry Institute Interaction; YCCE He had Published 51 research papers in various international journals & international and national conferences. He received Best Paper Award at PSG college of Engineering.