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An Investigation towards Effectiveness in Image Enhancement Process in MPSoC

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ABSTRACT

Image enhancement has a primitive role in the vision-based applications. It involves the processing of the input image by boosting its visualization for various applications. The primary objective is to filter the unwanted noises, clutters, sharpening or blur. The characteristics such as resolution and contrast are constructively altered to obtain an outcome of an enhanced image in the bio-medical field. The paper highlights the different techniques proposed for the digital enhancement of images. After surveying these methods that utilize Multiprocessor System-on-Chip (MPSoC), it is concluded that these methodologies have little accuracy and hence none of them are efficiently capable of enhancing the digital biomedical images.

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1. INTRODUCTION

Image enhancement is a method for digital image processing having a large range of application in medical and non-medical areas. The principle objective of image enhancement is manipulating image attributes to make it more appropriate for an observer to see. This can be implemented adapting algorithms developed on FPGA in Very Large Scale Integrated (VLSI) Circuits [1]. As an important class of vast scale integration, MPSoC is specifically a system on the chip integrated with multiple programmable processors as its system components. Widely having its applications in the digital signal processing field, communication, networking, and multimedia MPSoC incorporates all the required components for their operation. MPSoC is a distinct and an essential branch of multiprocessors. The complexity of the application to be designed would demand high-performance computing, and hence it fulfills the desire of being application specific, as it is divided into homogeneous and heterogeneous multiprocessors. The advantage of real-time application performance ability, functioning at low power and handling multiple tasks at the same instant of time, when combined with the reconfigurable hardware technologies MPSoC possess the capacity of building a custom hardware system [2]. A homogenous MPSoC system is easier to design a system because of the presence of the same type of nodes in the processor having lower power and performance throughput. In case of heterogeneous MPSoC systems, inbuilt with different processing nodes and hardware components, provides a higher speed of computing in order with programming flexibility. To maintain a balance in between both flexible programs and performance parameter the system, Application Specific Instruction-set Processor is introduced which works on MPSoC being its primary necessity. ASIP is capable of performing many image processing algorithms using one data path. When compared to conventional RISC processor, ASIP works at 16 times higher rate and performs several ID filtering processing in 8cycle/pixel along with the advantage of achieving Full HD (1920x1080) application [3]. Interconnections in MPSoC are established by Network-on-

Chip (NOC) to ensure high efficiency and scalability. The system design of low-cost NoC- based MPSoC and its applications are implemented using an algorithm to enhance a video based on Super-Resolution (SR) [4]. A technique to synthesize a heterogeneous architecture, having many processors, to speed up a particular application is dealt with the presented heterogeneous system synthesis to accomplish a design flow commercially built on the platform of XtensaTM from Tensilica Inc. This is the first tool integrating extensible processors for the synthesis of customized MPSoC [5]. Design space exploration is a method required to assess the different design alternatives for utilizing the immense hardware resources available in MPSoC efficiently. A solution is developed for the faster result simulation and calculation of the performance characteristic of MPSoC which reduces the time, and within the procedure of Transaction-level modeling, a unique way of defining the Programmer's View level is introduced by two complementary modeling sub levels [6]. The technique of adopting a framework based on high-level power calculation of MPSoC architectures working upon FPGA is called as event signatures, and it operates on the principle of abstract execution profiles. To perform a quick validation of the high-level power models when compared to the of the MPSoC implementations on FPGA, Daedalus is an entirely integrated tool-flow in which system-level synthesis and FPGA prototyping are carried out [7]. A high-performance FPGA implementation of an operator is introduced. It is performed by mapping technique of polynomials which are pixel value adaptable. The Drago operator is suitable for the operation of high-frame-rate and the proposed resource-efficient FPGA execution [8]. Section 1.1 discusses the background of the existing work reviewed followed by foregrounding the research problems identified in Section 1.2 and proposed solution in 1.3 Section 2 deals with current research methodologies most often adopted which have been presented to increase the output efficiency of the image enhancement system. Section 3 discusses the research gap. Existing research trends highlighting the models proposed are mentioned in section 3.1. Section 4 highlights the future scope of the evolving trends in image processing. Finally, Section 6 has the conclusion briefed on it.

1.1. Background

This section discusses the background of image enhancement. The surveillance systems using ***Electro-Optical (EO)*** have the capability of searching, detecting, tracking and monitoring the potential target designation. Since an issue is posed due to the difficulty in target detecting and detection of it, the proposed solution would reduce the clutter from the background and atmospheric degradation [9]. The enhancement of bio-medical images that detect the presence of liver cancer that happens to be world's sixth most common tumor, malignant is carried out by comparing the value of PSNR, MSE, algorithms based on contrast stretching, image histogram, shock filter and contrast limited adaptive histogram equalization [10].

1.2. Research Problem

Due to the growth and demand of cost, efficient image system operating with a minimal amount of power like video cam recorder, PC camera, and digital camera algorithm implied by it is a necessity. Algorithms applied for enhancement are critical regarding constraints and hence to maintain the image appeared in signal processing, these methodologies are utilized. Serial processors being deployed in the treatment of real-time multimedia image manipulation is problematic with the size of a picture having a higher resolution. To make the image processing system work efficiently providing the high-performance parameter in a short span of time is a demanding task. Implying the algorithms for image processing by hardware architecture is inconvenient in real time situation. Factors namely chip area, computational speed constraints; design maintained at low power should be adequately optimized. The design modeling should be carried out by hardware-based languages VHDL, Verilog or Xilinx system generator supporting Digital Signal Processing (DSP).

1.3. Proposed Solution

An electronic generated digital image can be improved regarding its superiority by enhancing it. Numerous mechanisms have been presented in the field of image enhancement with Field Programmable Gate Array (FPGA). Incorporation of Advanced Microcontroller Bus Architecture (AMBA)/Advanced high-performance bus (AHP) /Advanced Peripheral Bus (APB) /Advanced Extensible Bus (AXI) in the mechanism would provide a better interface for communication between the memory and medical image given as an input for enhancement reducing the effect of heterogeneity of MPSoC.

2. EXISTING RESEARCH TECHNIQUES

This section describes a brief overview of the existent methods that have been conducted to address the issues in image enhancement technologies. CMOS image sensor can be incorporated to provide lower power consuming enhanced images at a lesser cost but are majorly affected by the disadvantage of the low-quality factor [11].Image edges are the most attribute that gives the useful data for image interpretability. The operation of detecting the image edges is the work of Sobel operator. Software does not operate to meet the particular requirement of the real-time application as it posse's property of being less sensitive towards noise and results in lesser accuracy extent for complex edges [12]. Processing a data stream which has different image size bits is inconvenient. A single serial processor makes it incredibly difficult to handle several operations on a picture pixel for enhancing it [13]. Mapping of an image enhancement technique from software to hardware requirement is a demanding task.

The study of Alareqi et al. [14] focused on the use of spatial domain in FPGA and implemented the digital enhancement technique for real-time hardware in biomedical applications. Regular methods of image enhancement cannot satisfy the requirement in real-time. The technology was incorporated into hand image with veins utilizing Open Access Biomedical Image Search Engine. By the use of the DSP tool, an efficient architecture is built by involving the system generator blocks from it. Performance parameters are evaluated on FPGA Virtex (XUPV5- LX110T).The various techniques applied to a medical image showed that brightness control provided the best result and hence it was helpful in determining the data for the vein pattern. In the study of Salcic and SIvaswamy [15] suggested a way to attain a better speed of computation for the contrast of an image via low-cost FPGA that focuses on X-ray images. Filtering followed by histogram modification is the main principle of operation here. Global Histogram Equalization (GHE) was the idea behind the change of histogram whereas that for the functioning of a filter is High Boost Filter (HBF). A coprocessor was made to work on FPGA prototype ISA-bus board is the image coprocessor for enhancement, IMECO that enabled high-efficiency implementation of improvement methodologies and acquired high-performance, low-cost solutions provided by hardware/software co-design. Operations such as downloading and uploading an image with the configuration process of equipment. Practical enhancement of images is possible verifying the low-cost of a RAPROS prototype board. The study of Arici et al. [16] discussed a general frame work based on the equalization of a histogram for image enhancing purpose. The challenge of optimization that decreases the effect of the cost was given a solution by constructing a framework here. It is based on Histogram Equalization (HE) that resulted in contrast enhancement excessively which created visual artifacts and produced a processed image with an unnatural look. An algorithm was developed for serving contrast enhancement property that avoided the memory-bandwidth consuming operation and cumbersome calculations.

The study of Ma et al. [17] presented the design of an Intellectual Property of the APB Bridge that converted the translation input of AXI4.0- lite into APB 4.0 transactions input levels. The originally developed standard SoC bus was an initiative made by ARM named as AMBA 4.0.As a result, the characteristics of AXI4-Lite to APB bridge attained 32-bit AXI and APB interfaces, slave, and master respectively along with the support of sixteen APB peripherals and response of AXI read/write providing a result of error transfer results. The study of Paunikar et al. [18] discussed the design of an APB employing Universal Asynchronous Reception Transmission (UART) as its slave. To ensure data security, Linear Feedback Shift Register (LFSR) module was involved. Consumption of power with this design adoption was saved up to 6% and 10% of area optimization for the one interfaced with AMBA2 APM. The study of Zhiwei et al. [19] proposed a CMOS image sensor architecture, which used APB bus to incorporate image processing. The issue of color image processing and deals with the changes in the conventional and proposed architecture employed in the pipeline of digital still cameras. The study involves two efficient auto white balance techniques together which is a system on the chip. The image quality of raw data can immensely be improved as FPGA is applied. Results prove that VLSI architecture can be performed on an identical chip. The study of Li et al. [20] emphasized on the sequence of video for eliminating the unnecessary vibrations in it. A feature-based technique to stabilize the video in its full frame and an entirely FPGA based architectural system design pipelined feature was enabled. The presented methodology had the process of initial extraction from feature points with an algorithm named oriented fast and rotated brief, and later similarity check was done for frames which are consecutive. Further, the pairs of the points are operated with affine transformation with the help of random sample consensus-based estimation to determine the robust inter-frame movement. The evaluated results were integrated to find the parameters of cumulative motion among reference and present frames, smoothening the translational components via a Kalman filter. Image mosaicking technique was implied in constructing the mosaicked image, and respectively the display window was developed. Experimental observations indicated that presented system could deal with PAL input video

standard involving translation of arbitrating and enhanced viewing experience is seen at 22.37 milliseconds per frame, attaining real-time performance in processing. The study of Long et al. [21] presented an algorithm for edge enhancement in an image along with an algorithm implied in the reduction of noise functioning at 5*5 block on Y channel. The structure of parallel and pipelining was used for processing a single pixel which resulted in image reduction. The system design was created and validated at a frequency of 90MHz in Xilinx Virtex2 FPGA. Observations showed that a frame rate of 290 frames per second for VGA images was obtained. This technique efficiently minimized the effect of two kinds of noise in the system. The study of Yen et al. [22] dealt with the histogram equalization modified technique to enhance the property of contrast in the monochrome frame of an image. A lookup was created by the image which was alternatively sampled and quantized and later the table was applied to acquire the enhanced image. When comparing the original scheme, the differences found were minute to a viewer's eye. In cases of real-time processing, the adopted method of sampling and quantization was more appropriate for a hardware pipelining design. The technique was found suitable for surveillance systems also when the size of the frame was larger in comparison to the HDTV.

Author Smriti et al. [23] performed the comparative analysis of different image enhancement mechanisms by considering ultrasound liver image and suggested that shock filter can offer significant performance than other mechanisms.The pre-processing mechanism for enhancement of wireless capsule endoscopy image was illustrated in Shahril et al. [24], and it achieves improvement of 20.3% in PSNR and 31.5% in gradient value of the image. Ali et al. [25] used the Gaussian estimation parameter to remove the noise (i.e., salt & pepper) from the image and found quality enhancement in the image.

In the study of Chiuchisan [26], an implementation methodology to improvise the configurable system for image enhancement incorporating VHDL and architecture which is reconfigurable was initiated. For a medical specialist to have an enhanced version of images, a new set of filters were created at the hardware level. From Xilinx, ISIM simulator and the ISE design program component was implied for simulation and verification of the Verilog based system complex algorithms that could be rapidly prototyped with the employment of Verilog Hardware Description Language (HDL) with FPGA implementation. It shows that an additional processor was not mandatory to dedicate processing of an image.

The algorithms implied in the image enhancement for MPSoC on reconfigurable FPGA hardware are:

a. Brightness Control Algorithm: The image captured by a digital camera will generate an image having low brightness and the objects from it would not become visible prominently. By adding/subtracting the constant value to gray level of each pixel individually, this technique is effectively implied in increasing the brightness of an image or vice-versa.
b. Contrast Stretching: The intensity range value is expanded to improvise the quality by evolving the possible existing values. Low-light conditions are affected as a result of low image contrast value. The stretching is used for linear mapping for input to output values of the image.
c. Image Histogram: This algorithm is used to enhance the image contrast. The equalization would stretch the uniformly distributed histogram from gray levels at darker ends. It works on two principles namely, probability mass function and cumulative distribution function.
d. Edge Detection techniques: these are incorporated in the processing an image and vision of a computer to enable detection of the edges using operators namely Sobel and Prewitt. They calculate the approximate image function gradient.
a. Sobel operator: the principle of operation here is convolution performed on the image with filter values in vertical and horizontal directions through the pixels which are original
b. Prewitt operator and other techniques: mostly used for higher frequency changes in the image produced by gradient approximation, performs the same function as that of the Sobel operator.
e. Mean Filtering: This filtering technique replaces the centre pixel value from the window along the mean value possessed by all the pixels present in the window. Allows the reduction of the noise in the images and is held responsible for decreasing the variation in the intensity from one pixel to the next pixel that smoothens the fed image. In evaluating the mean, shape, and size of the neighbourhood, the convolutional kernel is initiated.
f. Image Thresholding: It is categorized as an image segmentation technique, which allows the creation of binary images in gray level. If the input given is lesser than the threshold value, the image pixel is replaced with the white pixel else black pixel.

Table 1 shows the summary of Existing Approaches.

Table 1. Summary of Existing Approaches

Authors	Problems	Technique	Outcome	Performance Parameters
Sree and Rao [1]	Enhancement of Retinal Fundus Image	FPGA based algorithm implementation	Comparison of hardware system with the software version for complex video inputs	Slice flip-flops, LUTs and block memory has reduced utilization of 1%, 1%, and 6% respectively.
Wolf et al. [2]	CAD problems in MPSoC	Survey paper	MPSoC is found as a distinct category of computer architecture	Improvised computational speed
Liao et al. [3]	Real-time processing of images	Application-Specific Instruction-set Processor*(*ASIP*)*	FullHD(1920x1080) application is achieved	Technology, normalized area, area, cache size, frequency
Singla et al. [4]	Interconnection in MPSoC	Network on Chip	Characterization of performance	SR Execution time, Number of processing elements and type of application
Sun et al. [5]	Heterogeneity in MPSoC	Algorithm based on expected execution time	First tool for synthesis of custom MPSoC	Custom area instruction
Atiallah et al. [6]	Resource utilization of MPSoC	Timed programmers view	Speedup factor is 18	Simulation Speedups, Number of processors, time of execution and number of contentions
Piscitelli et al. [7]	Complexity of MPSoC	Event signatures	Fairly accurate power estimates are obtained	Power consumption
Popovic et al.[8]	Execution of FPGA	Drago operator	Resource efficient FPGA execution	SSIM, PSNR
Singh et al.[9]	Long range detection of the target	EO Surveillance systems	High system speed performance observed	Utilization of sliced flip-flops, occupied slices, slices containing only one logic and DSP48s is 11%, 24%,100% and 1% respectively.
Sahu et al.[10]	Detection of Liver Cancer	Shock filter, CLAHE, Contrast stretching and Image histogram	Improvised version of the visual perception is observed	MSE and PSNR value
Jung et al. [11]	Requirement of real-time image enhancement	CMOS image sensor	Low-cost, one chip PC camera having higher performance was estimated	Logic gates optimization
Gou et al. [12]	Real-time parallel processing of videos	Sobel edge detection algorithm	Edge of gray image is located	Utilization of slices, flip-flops, LUTs, IOBs, BRAMs, GClk is 11%, 7%, 9%, 10%,16% , 12% respectively
Al Ali et al. [13]	Real-time processing of image using serial processors	Windowing operator	Image of any size can be traversed for its pixels	Device usage, time delay, frequency of clock and total power
Alareqi et al. [14]	Real-time image processing for biomedical applications	Inverting image operation, brightness control, segmentation, contrast stretching	Vein image detected is clear	MSE,MD,NAE,NCC, SC,PSNR, AD

Authors	Problems	Technique	Outcome	Performance Parameters
Salcic and Swamy, [15]	Computational speed of image contrast	IMECO	Target applications have real-time image enhancement	Speed of computation
Arici et al. [16]	Optimization reducing cost function	Histogram equalization	Contrast enhancement is presented	Enhancement measure, absolute mean brightness error, discrete entropy
Ma et al. [17]	Communication in bus	Intellectual property design	High-performance AXI bus is attained with APB domain	Read/ write operations, peripheral support
Paunikar et al. [18]	Interfacing challenges in APB	UART with LFSR	APB saves 6% power and 10% area	Power and area optimization with/without LFSR
Zhiwei et al. [19]	Color image processing	CMOS image +sensor APB bus	Possible to implement VLSI architecture on a single chip	Efficiency of transmission, process timing, minimized power consumption
Li et al.[20]	Vibrations in video sequences	Oriented fast and rotate brief algorithm	Viewing experience of 22.37 millisecond per frame was obtained	PSNR, Usage of device components
Long et al.[21]	Edge enhancement of an image	Noise reduction algorithm on Y-channel is proposed	Two kinds of noises are effectively reduced	Usage of multipliers, SRAM and LUT.
Yen et al.[22]	Contrast enhancement	Sample and quantized image	Frame size larger than HDTV can be accommodated	Standard deviation, efficiency of area performance, cost of hardware, throughput
Chiuchisan [23]	Configurability of real-time processing system	Employing new series of filters	Rapid prototyping of complex algorithms is possible	Brightness adjustment, contrast enhancement, sharpening operation

3. RESEARCH GAP

The following are the categories to be focused on the research gap in image enhancement:

a. Artefacts: For enhancement of bio-medical images, it is essential to remove artifacts like hair, air bubbles affecting the segmentation accuracy. This gives the need to develop the special aid to control the illuminated artifact.
b. Pixel lost: In the process of converting the original bio-medical image to the transformed form, the pixel values may tend to get altered or even get lost and hence to avoid this, a countermeasure should be adapted to retain the useful data in the pixels.
c. Illuminate misbalancing: The illuminance property of the image might face imbalance as there are predefined rules for the image transformation and the region of interest may not be particularly concentrated.
d. Edge degradation: Degraded edges can lead to variation in the enhancement of the image than the expected output, and since it has a crucial role in the process, it should be maintained at its initial value.

3.1. Research Trends

The existing research works towards enhancing an image in the field of spatial domain involving the techniques of histogram equalization, intensity transformation, and spatial filtering are found to have 71 journals, 180 conference publication and one early access article published. Systems implying frequency domain method for image enhancement include filtering process of low pass, high pass, linear; root and homomorphic methods had 216 conference publication, 83 journals and magazines, one early access article and one book and eBook published.

Figure 1 shows the existing Research Trends.

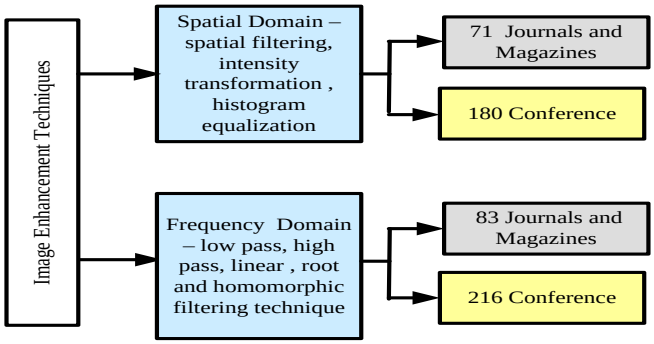

Figure 1. Existing Research Trends

4. CONCLUSION AND FUTURE WORK

Image enhancement can be applied in different domains, designed using multiple approaches to obtain images as per the requirement of the user. This paper presents the number of ways in which the attributes of an image can be enhanced with the FPGA hardware and MPSoC computing. Implementing an interfacing module consisting of AMBA AHB/APB/AXI, combination of advanced microcontroller bus architecture would control the operation of creating a communication channel in between the memory and algorithms developed in the system. Advanced high-performance bus initiates the performance; advanced peripheral bus provides the input-output peripheral device function. It supports 256 beats of length regarding burst, need of updated write and read operations and data on component operability. It has sixteen masters and sixteen slaves interfacing ability. Introducing hybrid algorithms in the future will be successfully able to overcome the drawbacks observed in the image processing technique. Capacity to boost the factor of contrast by using the edge filter hypothesis would immensely bring a change in the digital image fields.

In this paper, we have come across the problems of heterogeneity in MPSoC on FPGA that makes it crucial in designing a model that assures the overall high throughput and will act in increasing the behavior of an image. Unifying the image enhancement algorithms namely brightness control, contrast stretching, negative image transformation, gamma correction or power-law transformation, image histogram, mean filter, Median Filtering, histogram equalization, Sobel operator, Prewitt operator and image thresholding will initiate a method to rectify the drawbacks in the previous research works introduced in the approval of image enhancement. AMBA AXI-4 can behave as a bus giving suitable solution for the interfacing non-convenience between the inputs from the user to the output gained after processing.

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