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Variable Body Biasing (VBB) based VLSI Design Approach to Reduce Static Power

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ABSTRACT

The static power consumption is an important parameter concern in IC design due to t for a higher integration numbers of transistor to achieve greater performance in a single chip. Leakage current is the main issues for static power dissipation in standby mode as the size of transistor been scale. Therefore, the subthreshold leakage current rises due to threshold voltage scaling and gate leakage current increases due to scale down of oxide thickness. In this paper, a Variable Body Biasing (VBB) technique was applied to reduce static power consumption in VLSI design. The VBB technique used a DC bias at body terminal to control the threshold voltage efficiently. The Synopsys Custom Designer EDA tools in 90nm MOSFET technology was used to design a 1-bit full adder with VBB technique in full custom methodology. The simulation of 1-bit full adder was carried out with operation voltage $V_{DD} = 0.2V$ supply was compared in conventional technique and VBB technique. The results achieved the reduction in term of peak power, $P_{peak} = 33\%$ and average power, $P_{avg} = 13\%$ in static CMOS 1-bit full adder compared with conventional bias and VBB technique.

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1. INTRODUCTION

In nowadays technology, the size of transistors was scaling down to sub-nanometer (nm) to achieve higher density number of transistor to design a complex, high performance circuit in a smaller size of area. The scaling down in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) channel size is a big challenge for the Integrated Circuit (IC) designers as it doubles every two years according to Moore's law [1].

As the MOSFET technology channel size downscaling, the subthreshold leakage current exponentially increases as threshold voltage (V_{th}) reduces [2]. In a sub-nanometer of transistor, the shorter channel length of transistor will be resulting sub-threshold leakage current through at transistor when in standby mode. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned OFF completely. Therefore, the static power consumption will occur due to the leakage current when the transistor in standby mode. As a result, it will consume leakage current dissipation, in which has become a significant portion of total power consumption for future IC design technologies in a smaller MOSFET channel length.

In a shorter channel length between Source and Drain of a MOSFET, it will down scaled the transistor threshold voltage (V_{TH}) to maintain a reasonable gate over drive [2]. The MOSFET V_{TH} reduction,

result in an exponential increases in the subthreshold current. Moreover, to control the short channel effects (SCEs) and to maintain the transistor drive strength at low supply voltage, the oxide thickness needs to be also scaled down. The aggressive scaling of oxide thickness results in a high tunneling current through the transistor gate insulator.

In MOSFET, the subthreshold conduction takes place when the applied gate voltage is under the threshold voltage (V_{th}). In long channel devices the V_{TH} is independent of the Drain bias, but in sub-nm channel length devices the scenario is different and causes Drain Induced Barrier Lowering (DIBL). The general equation for subthreshold leakage is [2]:

$$I_{sub} = I_0 e^{(V_{GS}-V_T)/nV_{TH}} \quad (1)$$

where $I_0 = \mu_0 c_{ox} \frac{W}{L}(n-1)V_{TH}^2$, V_{GS} is the gate-source voltage, V_T is the thermal voltage (KT/q), n is the subthreshold swing coefficient, V_{th} is the threshold voltage, μ_0 is the carrier mobility at zero bias, c_{ox} is the gate oxide capacitance, W and L are the effective transistor width and length.

To minimize the subthreshold leakage current dissipation, this paper proposed a Variable Body Bias (VBB) technique to reduce static power consumption in VLSI design. However, there are several VLSI design techniques to reduce leakage power nowadays. Each technique provides an efficient way to reduce leakage power, but the drawback of each technique limit the application of each technique.

2. RESEARCH METHOD ON VBB TECHNIQUE

Typically, the body terminal from a MOSFET is used to control the threshold voltage, V_{th}. This benefit made convenient to the IC designers in controlling the V_{th} by biasing the body of MOSFET independently. This independent body bias dynamically varies the threshold voltage of the MOSFET and the effect of V_{TH} variation due to body bias is known as body effect. The basic equation which shows how body bias impacts on threshold voltage V_{th} is [3]:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\emptyset_B - V_{SB}} - \sqrt{2\emptyset_B}\right) \quad (2)$$

where V_{th} is the threshold voltage, the $\emptyset_B$ is the flatband voltage, γ is the body effect coefficient, V_{th0} is the threshold voltage with zero substrate bias and V_{SB} is the source to body bias voltage.

According to Equation (2), V_{TH0}, γ and $\emptyset$ are the constant element at which setting by the technology's parameter. Therefore, based on Equation (2) the threshold voltage, V_{th} is directly proportional with the source to body bias voltage, V_{SB}, ($V_{th} \propto V_{SB}$). Therefore, the body terminal of a MOSFET able to control the threshold voltage, V_{th}.

Conventionally, in order to maintain the minimum threshold voltage (V_{th}) in static CMOS configuration, the body terminals of pMOS is connected to V_{DD} and the nMOS body terminals connected to ground. In the proposed VBB technique, the logic the body of the pMOS connected to a positive body biased ($+V_{BB}$) to increase their V_{th} in standby mode. Meanwhile, the nMOS body was connected in negative body biased ($-V_{BB}$) to increase the V_{th} because of the body-bias effect in static mode. Figure 1 illustrates the conventional static CMOS connection and VBB technique connection logic design [4].

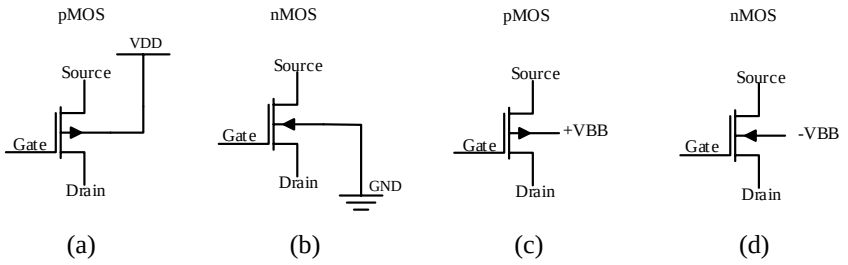

Figure 1. Body connection of logic design (a), (b) in conventional, (c) and (d) in VBB technique.

The proposed circuit design using VBB technique dynamically control the threshold voltage of transistors through body biasing in standby mode. The body biasing in pMOS biases the body of the transistor to a voltage higher than V_{DD}, while in nMOS to a voltage lower than V_{SS} thereby reducing leakage

current. To be more understanding of VBB technique, a schematics of CMOS inverter with VBB technique circuit was carried out. Figure 2 illustrates an inverter design with VBB technique.

Based on Figure 2, there was an external supply connected to the body of each MOSFET. Since raising threshold voltage will affects performance and the VBB technique control the body to be applied different input voltage supply, so during an active mode of operation the reverse bias is small, while in standby the reverse bias is stronger. Therefore, it can be reducing the sub-threshold leakage current and reduction of static power dissipation [5].

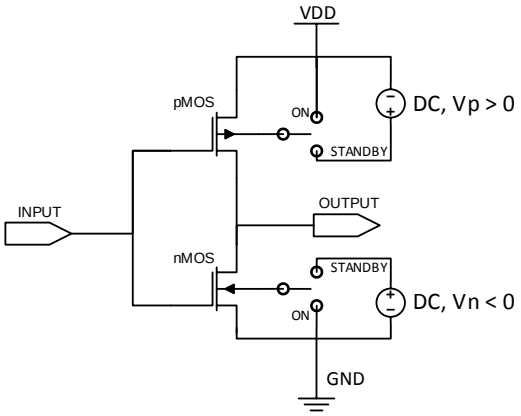

Figure 2. An inverter with VBB technique

3. VBB TECHNIQUE IN 1-BIT FULL ADDER

In this paper, the 1-bit full adder was designed in conventional bias and VBB technique. The results obtained were compared and analyze in term of power consumption, propagation delay and number of transistor designed in 1-bit full adder. A 1-bit full adder is a combinational circuit which results in arithmetic sum of two bits. Typically, a full adder has three input terminals and two output terminal. The three inputs are denoted by A, B and a carry input, C_{in} and produce two output namely as summation, SUM and carry out, C_{out}. The truth table of a full adder is shown in Table 1.

Table 1. Truth table of a 1-bit full adder

INPUT			OUTPUT	
A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table of full adder, the Boolean equation for SUM and C_{out} can be obtain by solving with Karnaugh map. The equation for full adder is shown as below:

$$\begin{aligned} SUM &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \\ &= (A \oplus B) \oplus C \end{aligned} \quad (4)$$

$$\begin{aligned} C_{out} &= AB + AC + BC \\ &= \overline{\overline{AB + C(A+B)}} \\ &= \overline{(\overline{A+B})(\bar{C} + \overline{AB})} \\ &= \overline{\bar{A}\bar{B}} + \bar{C}(\bar{A} + \bar{B}) \end{aligned} \quad (5)$$

Nowadays, the number of transistors had been reduced to achieve low power consumption in a system. Conventionally, the static CMOS full adder design at which the number of pMOS pull-up network (PUN) and nMOS pull-down network (PDN) must be equivalent. Based on Equation (4) and Equation (5), the static CMOS 1-bit full adder can be design in 28T (Transistor) based on the following equation which is obtained by rearranging the SUM equation and factoring SUM in order to reuse the C_{out} term as below:

$$SUM = ABC + (A + B + C)C_{out} \quad (6)$$

Rather than following the conduct complements rule, the pMOS PUN in the adder circuit is identical to the nMOS network according Equation (6). The area efficiency can be obtained in layouts due to this simplification which provides uniformity CMOS design by reducing the number of transistors connected in series. Thus, the static CMOS 28T 1-bit full adder was become the most common full adder in IC design. The schematics of the static CMOS 1- bit full adder using 28T [7] shown in Figure 3.

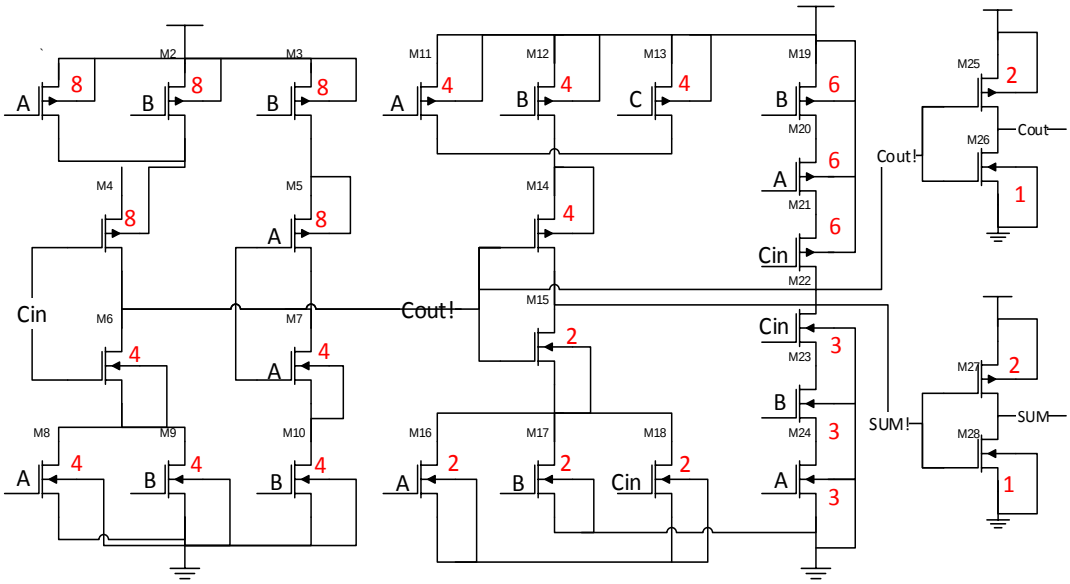

Figure 3. A static CMOS 1-bit full adder with 28T

The MOSFET in designed the 1-bit full adder size was in term of $\left(\frac{W}{L}\right)$ ratio were carried out based on the logical effort calculation in order to optimize the propagation delay. The logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current. Equivalently logical effort indicates how much worse a gate is at producing output current as compared to an inverter. Table 2 shows the logical effort of basic common gate that will be used for design 1-bit full adder [6].

Table 2. Logical effort of basic common gate

Gate type	Number of inputs					
	1	2	3	4	5	n
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n + 2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3

Conventionally, the full adder of 28T, the pMOS is connected to V_{DD} and nMOS connected to ground used to prevent latch-up in CMOS where the body-source and body-drain diodes should not be forward biased. In the static 28T 1-bit full adder design shown in Figure 3, the logical effort was being calculate in achieve a minimum propagation delay. The sizing in $\left(\frac{W}{L}\right)$ ratio of transistors were illustrated in red color number.

This paper proposed a VBB technique in a conventional static CMOS 28T full adder design, the body of pMOS and nMOS will be connected to an external source supply in order to provide a reverse bias in standby mode to reduce the sub-threshold leakage current. Figure 4 illustrates the schematic of CMOS 28T full adder with VBB technique.

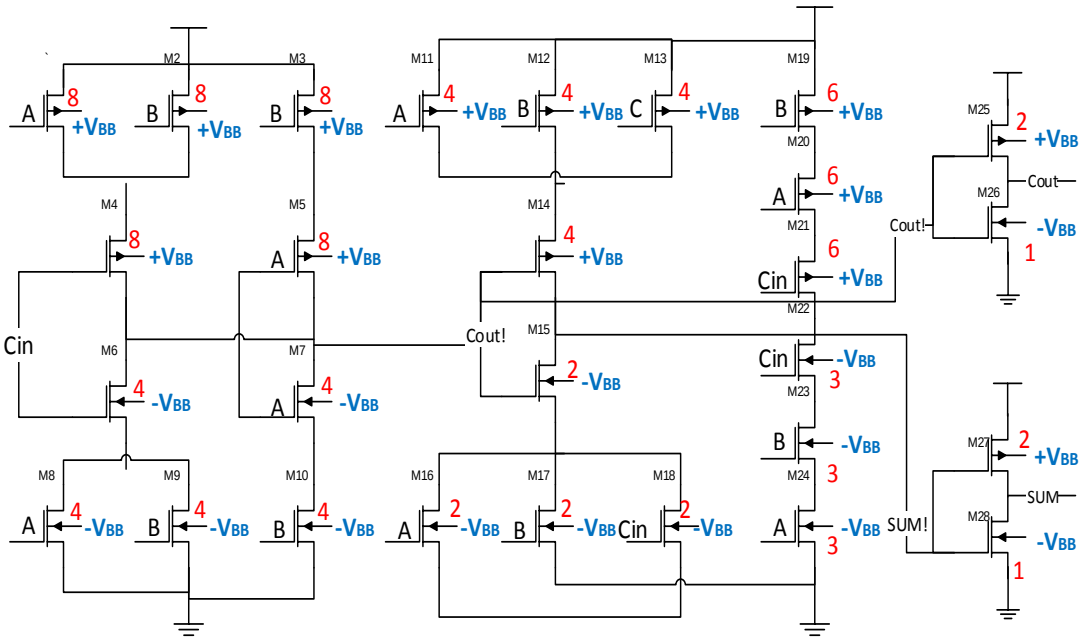

Figure 4. A 28T static CMOS 1-bit full adder with VBB technique

The comparison had been carrier out to analyze performance parameter of power consumption, delay and Power Delay Product (PDP). In order to further reduce the static power consumption, the reduction number of transistor must be done. By resolving and manipulated the Boolean equation of full adder, the number of transistor to design a 1-bit full adder can be reducing by implementation using Complementary Pass Logic transistor (CPL) and Transmission gate design.

The 1-bit full adder circuit with minimize numbers of transistor was being design in 20T [8], 16T [9], 14T [10], 11T [11] and 10T [11] in conventional bias mode and VBB technique to analyze the power consumption. Figure 5 illustrates the 20T 1-bit full adder in transmission gate. Figure 6 illustrates full adder with 16T design in minimize the XOR logic with transmission gate. Figure 7 14T 1-bit full adder was design in CPL with transmission gate. Circuit in Figure 8 and Figure 9 used 11T and 10T 1-bit full adder design with CPL transistor in low power terminology design. The each 1-bit full adder logic style can be used depending upon specific design requirements and constraints imposed by applications. In each of the design the high threshold transistor was been used to reduce the power consumption with high doping concentration of pMOS and nMOS. However, the used of high threshold transistor will increase the propagation delay performance compare with standard MOSFET.

Since this paper focussed on sub-threshold leakage current in which concern on static power dissipation. The design terminology minimizes the used of number transistors designed for 1-bit full adder will not be discussing. The body biasing in conventional and VBB technique of 1-bit full adder was simulating with Synopsis EDA tools of Simulation and Analysis Environment (SAE) in 90nm CMOS technology. The SAE is a comprehensive transistor-level simulation and analysis environment that is tightly integrated and included with Synopsys HSPICE circuit simulators. The netlist-based flow of SAE provides intuitive and comprehensive capabilities to efficiently set up and launch simulations, and analyze and explore simulation results to improve the productivity of analog verification. In order to ensure all the 1-bit full adder running at a similar timing analysis in SAE, the input supply setting was been standardized pulse applied for input A, B and C_{in} as shown in Table 3.

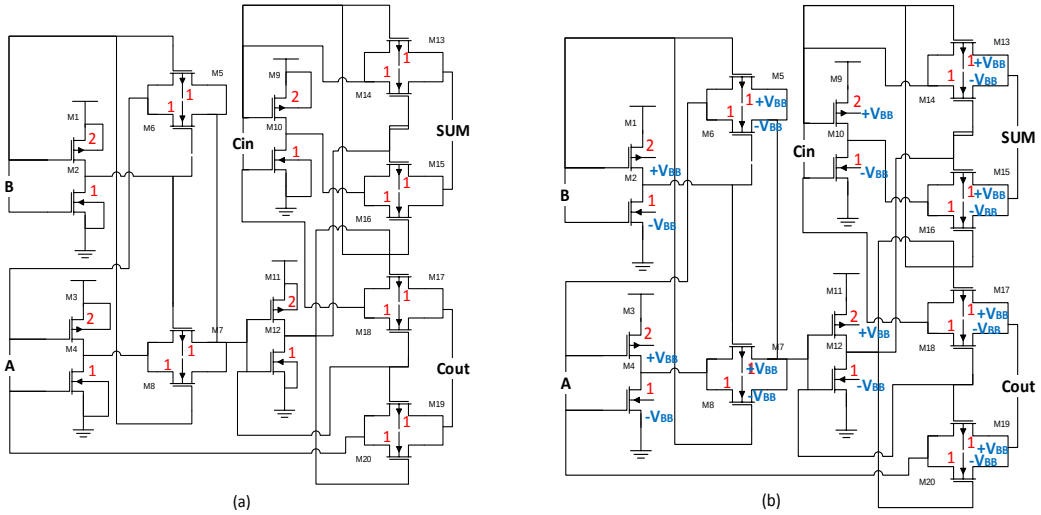

Figure 5. 20T 1-bit full adder design in (a) conventional bias and (b) VBB technique

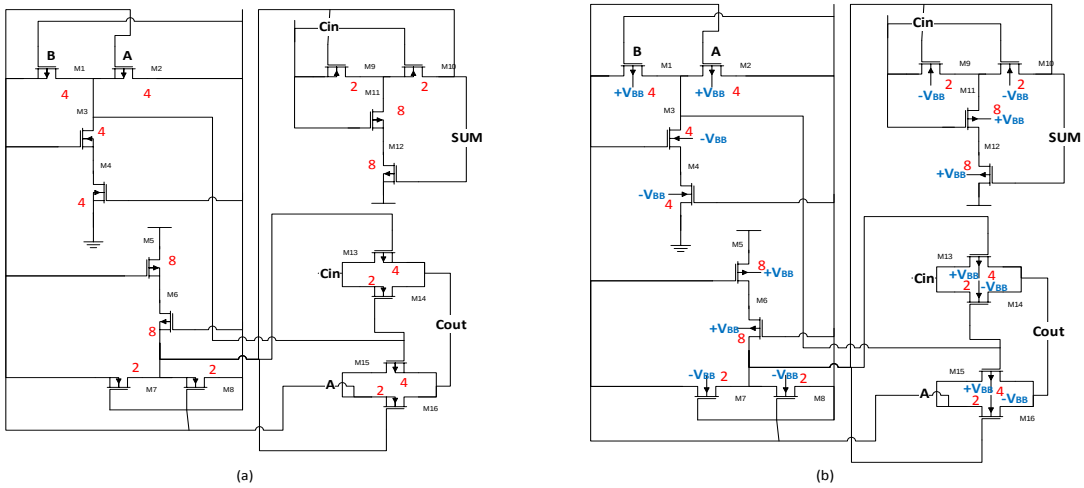

Figure 6. 16T 1-bit full adder design in (a) conventional bias and (b) VBB technique

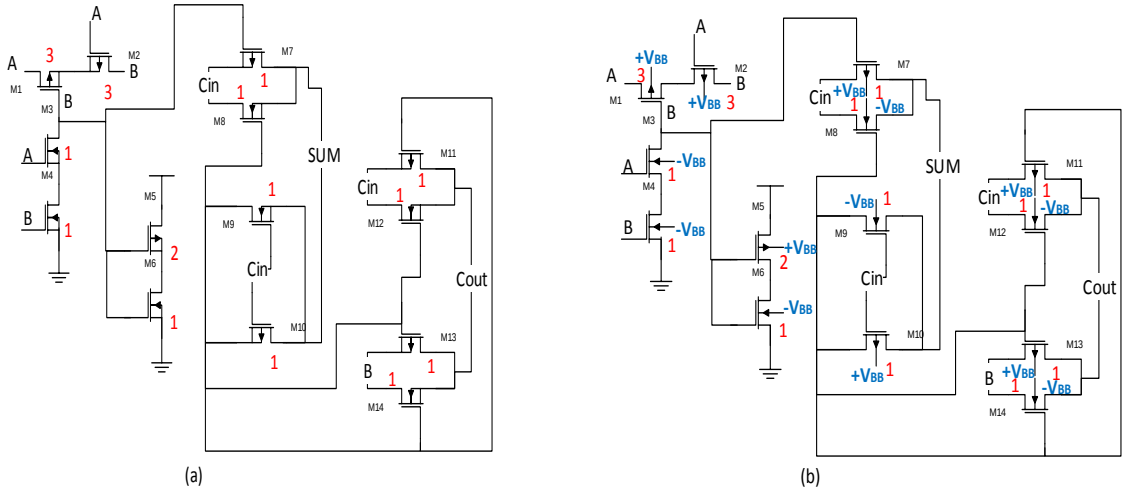

Figure 7. 14T 1-bit full adder design in (a) conventional bias and (b) VBB technique

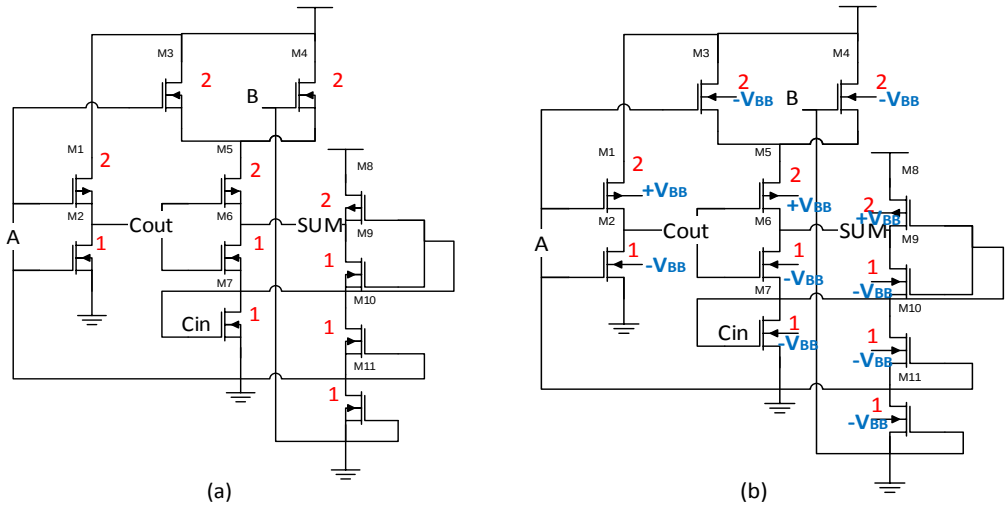

Figure 8. 11T 1-bit full adder design in (a) conventional bias and (b) VBB technique

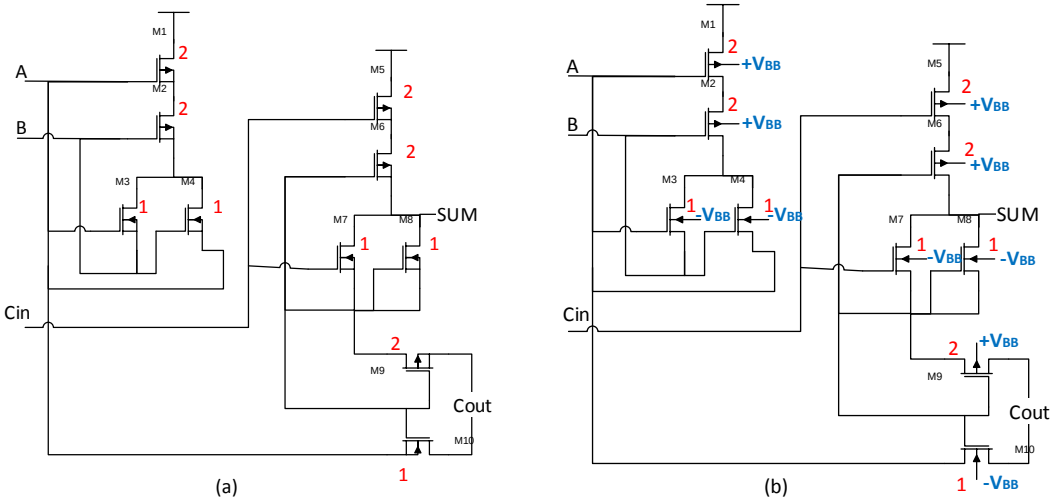

Figure 9. 10T 1-bit design in (a) conventional bias and (b) VBB technique

Table 3: Standardized input for 1-bit fill adder

INPUT	V_{DD}	Rise time	Fall time	Pulse width	Period
B	0.2V	10ns	10ns	2us	4us
A	0.2V	10ns	10ns	4us	8us
C_{in}	0.2V	10ns	10ns	6us	12us

From the inputs pulse setup on Table 3, the most significant bit (MSB) was input C_{in} and the least significant bit (LSB) was input B. The pulse width was set with the 50% of a period. The period of the simulation perform was began at 4us for input B, 8us for input A and 12us for input C_{in}. Moreover, the rise time and fall time of the pulse width was set at 10ns to observe the glitch intersect occurs on the output.

4. RESULT AND ANALYSIS

The 1-bit full adder will be design simulated in Synopsys CMOS 90nm technology tools with the standardize operating voltage of $V_{DD} = 0.2V$. The functionality of designed 1-bit full adder was verified by comparing with the truth table.

Furthermore, the comparison of 1-bit full adder continue in term of power performance, propagation delay and power delay product (PDP) were been carried out. Table 4 shown the simulation result of different types of 1-bit full adder with standardize operating voltage of $V_{DD} = 0.2V$.

Table 4: Simulation result of 1-bit full adder design

Number of Transistor	Body Bias Technique	Peak Power (nW)	Average Power (nW)	RMS Power (nW)	Delay (ns)	PDP (aJ)
28T	Conventional	123.40	1.067	2.009	25.61	27.33
	VBB	82.72	0.9275	1.447	27.43	25.44
20T	Conventional	34.25	0.6687	1.114	43.78	29.28
	VBB	30.05	0.5913	0.8993	47.32	27.98
16T	Conventional	18.04	0.5574	0.9152	56.76	31.64
	VBB	16.67	0.4638	0.6787	58.92	27.33
14T	Conventional	25.23	0.3761	0.8724	57.43	21.60
	VBB	15.38	0.2828	0.6211	59.75	16.89
11T	Conventional	13.89	0.2043	0.5478	62.71	12.81
	VBB	13.72	0.1321	0.4522	64.89	8.57
10T	Conventional	6.935	0.2889	0.5486	67.34	19.45
	VBB	4.058	0.1932	0.3004	69.28	13.38

For the conventional static CMOS 1-bit full adder using 28T, it achieved the reduction power performance in term of $P_{peak} = 33\%$, $P_{avg} = 13\%$, $P_{RMS} = 28\%$ and PDP reduction of 7% compared between conventional bias and VBB technique. Therefore, the VBB technique successfully reduce the sub-threshold leakage current gradually reduce static power dissipation.

Based on Figure 10 and Figure 11, the reduction of power consumption was gradually reduced as the number transistor in designing 1-bit full adder decreased. Moreover, the proposed VBB technique showed the reduction of static power consumption across the number transistor used. Thus, the minimize usage of transistor was successfully reducing the static power consumption.

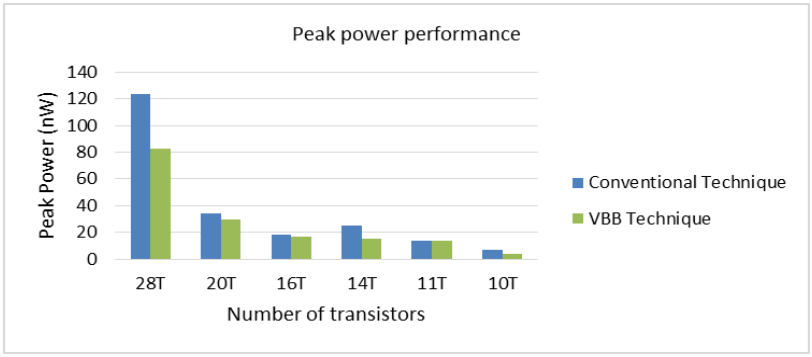

Figure 10. Comparison of peak power performance with number of transistor

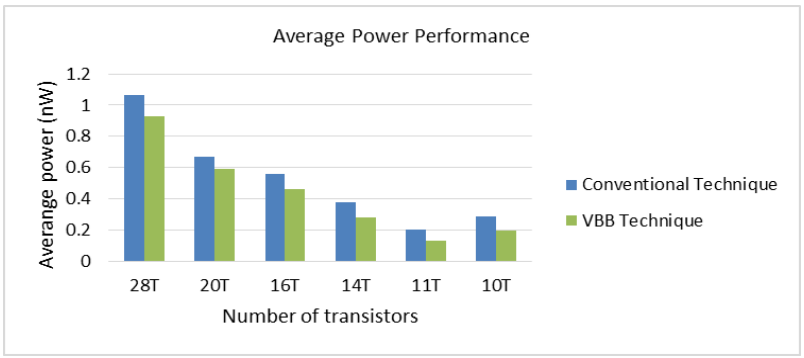

Figure 11. Comparison of average power performance with number of transistor

Furthermore, the VBB technique have a drawback in the propagation delay at the carry out from the adder summation. Based on Figure 12, there was an increased in delay because of less output driving capability due to the increase in threshold voltage of the device by using VBB technique during standby mode. Moreover, the delay increase because the used of CPL and transmission gate of 1- bit full adder designed. Since the nMOS will pass strong LOW (0) logic while pMOS pass strong HIGH (1) logic, thus in the CPL or transmission gate 1-bit adder designed will be used of an nMOS or pMOS acts as switch to control the flow of input voltage. However, in term of PDP obtained shown that the reducing the numbers of transistor will efficiency reduce the static power consumption.

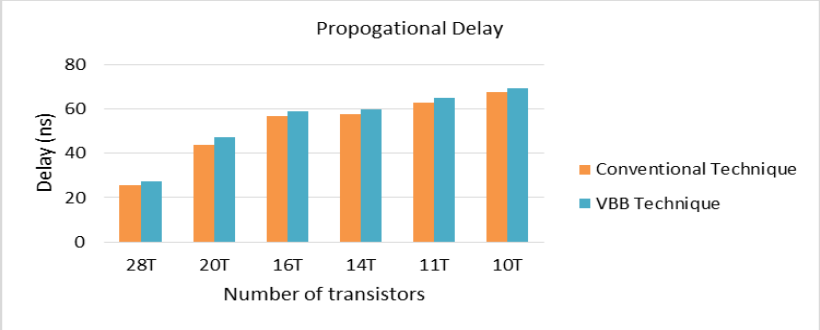

Figure 12. Comparison of propagation delay with no. of transistor

5. CONCLUSION

The proposed of Variable Body Bias (VBB) technique in different number of transistors designed in 1- bit full adder was presented and compared in term of power performance, propagation delay and power delay product (PDP). By comparing in term of static 28T CMOS 1-bit full adder with approached VBB technique was achieved reduction more than 32% in peak power saving and 13% in average power but slightly increasing in delay of 7%. Hence from the comparisons, the proposed VBB technique is one of the best alternatives method to achieve low power consumption with accepted performance in VLSI design.

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Woo Wei Kai currently an undergraduate student in Electronic Engineering specialized in Microelectonic Engineering from Universiti Tun Hussein Onn Malaysia (UTHM) and received a Diploma in Electrical Enginnering on 2015 in UTHM. Currently he was involving in Integrated Circuit (IC) designed project in term of low power, high performance and smaller in area on 90nm technology design. He has done a project such as arithmetric logic unit system, SRAM memory system, variable body bias designed system in full custom methodology. He was familiar in designing circuitry with Synopsys EDA tools at schematics and physical design level of a system.

Nabihah @ Nornabihah bt Ahmad received her Ph.D in Electronic Engineering from Massey University, New Zealand in 2014. She is a senior lecturer at the Department of Electronic Engineering, Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia (UTHM). She received a Bachelor of Electrical, Electronic and Systems with Honours from Universiti Kebangsaan Malaysia and Master of Electronic Engineering (Microelectronic) from Kolej Universiti Tun Hussein Onn Malaysia in 2002 and 2005, respectively. She has published a number of research papers in international journals and conferences in the area of Digital, Analog Integrated Circuir Design and VLSI Design. Her research interests include IC design, low power VLSI circuit design, cryptography co-processor, SoC, low power digital system and ASIC/FPGA design. She is currently a member of Board of Engineers Malaysia (BEM), IEEE, IEEE Young Profesionals and IEEE Circuit and System.

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