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Low-Power D-Band CMOS Amplifier for Ultrahigh-Speed Wireless Communications

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ABSTRACT

This paper presents a low-power D-Band amplifier suitable for ultrahigh-speed wireless communications. The three-stage fully differential amplifier with capacitive neutralization is fabricated in 40 nm CMOS provided by TSMC. Measurement results show that the D-band amplifier obtains a peak gain of 9.6 dB over a -3 dB bandwidth from 138 GHz to 164.5 GHz. It exhibits an output 1 dB compression point (OP1dB) of 1.5 dBm at the center frequency of 150 GHz. The amplifier consumes a low power of 27.3 mW from a 0.7 V supply voltage while its core occupies a chip area of 0.06 mm^2.

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1. INTRODUCTION

According to the current trend, the frequency used for wireless communication will reach the terahertz band in 2020. The unallocated frequency region beyond 275 GHz with vast bandwidth can be potentially utilized for ultrahigh-speed wireless communication. In particular, the 300 GHz band is attractive since propagation decay in air around 300 GHz is relatively low. However, since studies on terahertz wireless communication including the 300 GHz band are still in early stage when only a few transceivers operating above 275 GHz were reported [1] [2]. Since the maximum operating frequency or the unity-power-gain frequency, $f_{\max}$, of the n-type MOSFET even with advanced CMOS process is below 300 GHz, realization of 300 GHz RF front-end is challenging. One solution is to use frequency multipliers. A 300 GHz CMOS RF front-end was reported using a tripler [4]. However, the tripler generates not only the desired RF signal but also the higher-order spurious. As a result, the RF signal may be distorted by a higher-order spurious. On the other hand, since quadratic nonlinearity of a MOSFET is stronger than its cubic counterpart, a doubler can generate higher output power than a tripler does. When the doubler is employed, the 300 GHz output signal can be generated from the 150 GHz input one. In this paper, we are going to present a low-power D-band amplifier whose center frequency is 150 GHz. This amplifier will be used as the preceding stage of the 300 GHz doubler.

2. DESIGN OF D-BAND AMPLIFIER

The D-band amplifier is designed using TSMC 40 nm 1P10M CMOS GP process. Its back end consists of 10 copper layers and a top aluminum redistribution layer (RDL). The cross-view of a grounded coplanar wave-guide transmission line (GCPW-TL) is depicted in Fig. 1 [5]. The GCPW-TL with the characteristic impedance of 50 Ω (the 50 Ω GCPW-TL) is used for connecting to the input and output pads of the D-band amplifier. Its signal line consists of the RDL layer with a width of 9 μm. Ground (GND) walls composed of the 6th to 10th metal layers with a width of 2.7 μm are placed on the both side of the signal line at the distance of 7.2 μm. The GCPW-TL with the characteristic impedance of 71 Ω (the 71 Ω GCPW-TL) is used for the shunt stubs of the amplifier's matching

networks and the series stubs of the rat-race balun. The width of the top-layer signal line is 2.9 µm, and the GND wall placed at a distance of 7.6 µm from the signal line has the width of 1.8 µm. The 3nd to 5th metal layers are meshed and stitched together with vias to form the GND plane.

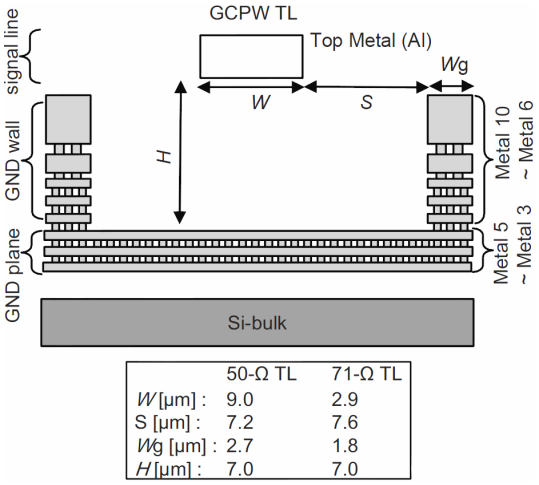

Figure 1. The cross-view of the 71 Ω GCPW-TL.

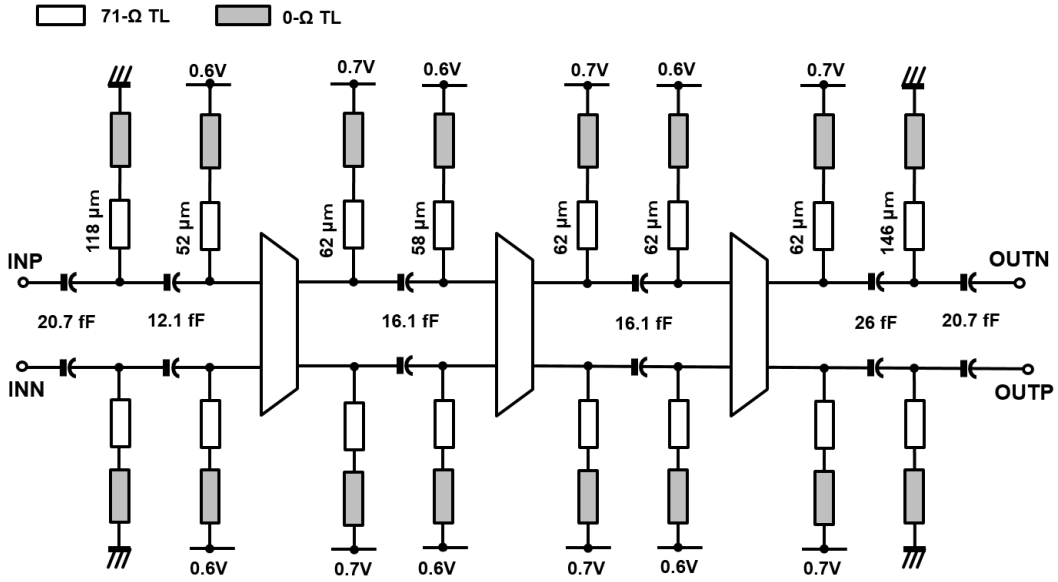

Figure 2. The proposed D-band amplifier.

The complete circuit of the proposed amplifier with all component values are given in Fig. 2. It includes input matching networks, output matching networks, three fully differential amplifying stages and inter-stage matching networks. For bandwidth enhancement, multi-stage matchings using capacitors and GCPW-TLs are adopted. The series capacitors and shunt GCPW-TLs form 4th-order high-pass filters at the inputs and outputs of the amplifier. Both the inputs and outputs are matched to 50 Ω for measurement purpose. The inter-stage matching networks are based on PI networks for wideband performance. All of the capacitors also act as coupling capacitors while the DC bias voltages are applied through the GCPW-TLs. The bias voltages are common to all amplifying stages. The shunt stubs composed of the 71 Ω GCPW-TLs are arranged regularly with sharing GND walls, and the space between the GCPW-TLs is 17 µm. The near-end and far-end crosstalk simulated by EM simulation are below -30 dB and -34 dB at 100 GHz and 250 GHz, respectively. It indicates that the cross-coupling between stubs is negligible.. The connection between the MOSFETs, MOM capacitors and GCPW-TLs are made by the 8th to 10th metal layers. The lengths of the GCPW-TLs and the number of fingers of MOM capacitors are determined by a nonmetric optimization process taking into account the models of MOSFETs, MOM capacitors and GCPW-TLs. The far end of each shunt

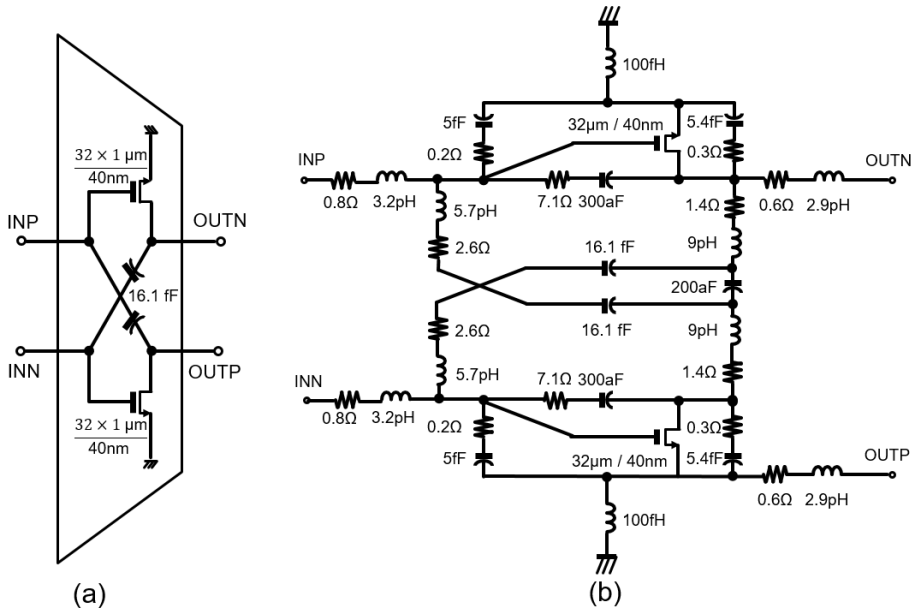

Figure 3. Amplifier core (a) and its equivalent circuit with extracted parasitics (b).

stub is terminated by a wideband decoupling power line with very low characteristic impedance (the 0 Ω TL) [6].

The internal negative feedback path caused by the parasitic gate-drain capacitor, C_{GD} limits the power gain and reverse isolation, and potentially causes instability. In order to improve the stability without compromising the gain of the MOSFET, the internal feedback in the transistor has to be reduced. An elegant technique to accomplish this is to neutralize C_{GD} in a differential pair by using cross coupling capacitors [7]. Fig. 3a shows the core of the amplifier that is a fully differential pair with capacitive neutralization. The cross coupling capacitor whose value is 16.1 fF is determined to obtain high gain. Fig. 3b reveals the parasitics associated at each node of the amplifier core. The parasitic components are extracted using bond-based design which is a measurement-based design approach to avoiding the difficulty associated with layout parasitics when ordinary layout parasitic extraction (LPE) tools used for chip design do not extract inductances [8]. Multistage amplifiers for terahertz frequencies tend to occupy a large area since inter-stage matching networks consist typically of several passive devices that are much large than MOSFETs. To realize cost-effective chips, area reduction is important. In order to reduce the area of the amplifier, we proposed the "fishbone layout" [9]. In this technique, GCPW-TL stubs used in matching networks are arranged regularly at narrow spacings, and the GCPW-TLs themselves are designed to be narrow, thereby reducing the footprint.

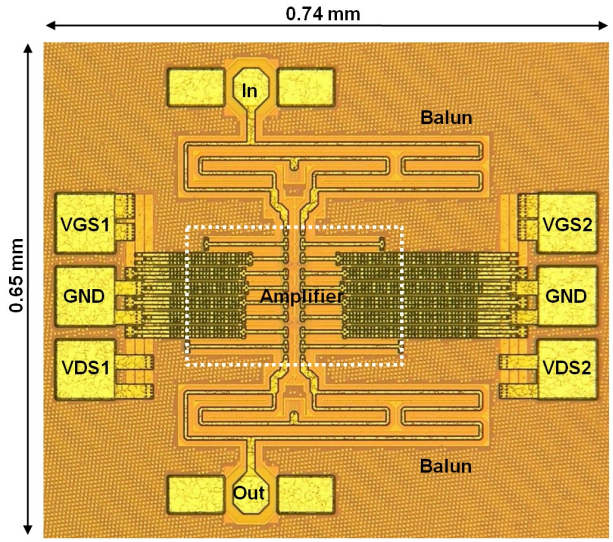

Figure 4. The die microphotograph of the D-band amplifier.

Table 1. Comparison with previous published amplifiers operating in the similar frequency band

Parameter	MWCL'11 [10]	Elec. Let'11 [11]	APMC'13 [12]	RFIT'15 [5]	**This work**
CMOS Technology	65 nm	65 nm	65 nm	40 nm	**40 nm**
No. of Stages	3/Differential	5/Differential	4/Differential	5/Differential	**3/Differential**
Gain (dB)	20.6	8.1	7.1	19.7	**9.6**
Center Freq. (GHz)	144	200	147	138	**150**
-3 dB BW(GHz)	3*	5*	13*	22	**26.5**
Die Area (mm^2)	0.05	0.06	0.12	0.06	**0.06**
Supply Voltage (V)	1.4	2.0	2.0	0.94	**0.7**
Power Cons. (mW)	54.6	108	104	75	**27.3**
GBWP/P_{DC}	0.59	0.12	0.28	2.83	**2.93**

* Estimated graphically

3. MEASUREMENT RESULTS

In order to verify the performance of the D-band amplifier, a chip prototype was fabricated in TSMC 40 nm CMOS. Fig. 4 shows the die microphotograph of the amplifier. The amplifier occupies an area of 0.65×0.74 mm^2 including probe pads, input and output balun while its core is only 0.06 mm^2. The rat-race balun composed of the 71 Ω GCPW-TLs is designed for conversion between the single-ended and differential signals at the inputs and outputs of the amplifier. The length of the GCPW-TL unit of the rat-race balun is 300 µm which is equivalent to $\lambda/4$ at 150 GHz (λ is the wave length). The compact design is realized by folding the GCPW-TLs and sharing the GND wall. The amplifier was measured by means of on-chip probings using a probe station. The RF probe pads were designed for ground-signal-ground (GSG) probes with 750 µm pitch. The Anritsu 37397D VNA and D-band frequency extenders were used for measuring small-signal S-parameters.

Fig. 5 shows the measured and simulated S-parameters of the D-band amplifier. As can be seen in this figure, the measured results show good agreements with the simulated ones. Both input and output return loss indicate wideband performance when S_{11} and S_{22} remain below -10 dB over the -3 dB bandwidth from 138 GHz to 164.5 GHz. The D-band amplifier achieves a peak gain of 9.6 dB at 150 GHz (after compensating for the rat-race balun's loss). The reverse isolation is lower than -40 dB. A high reverse isolation guarantees high stability for the amplifier. Fig. 6 plots the output power versus the input power. A Keysight E8244A signal generator and a VivaTech VTXFA-06-12 signal module were used for generating input signal at 150 GHz while a VDI PM5-305V power sensor was used to measure the output power. At 150 GHz, the designed amplifier obtains a OP1dB of approximately 1.5 dBm. The amplifier consumes a low power of 27.3 mW from a 0.7 V supply voltage. Table 1 summarizes the performance of the proposed amplifier and compares it to other published ones operating in the similar frequency range.

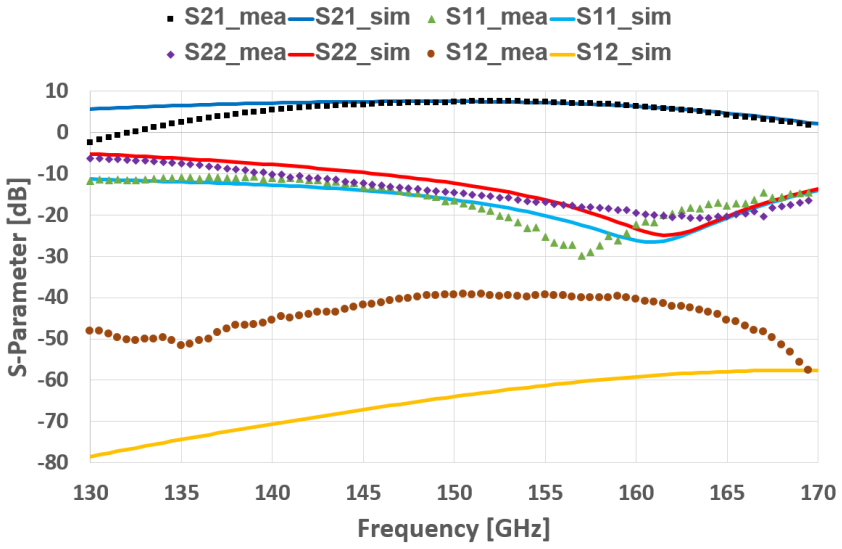

Figure 5. The measured and simulated S-parameter of the D-band amplifier.

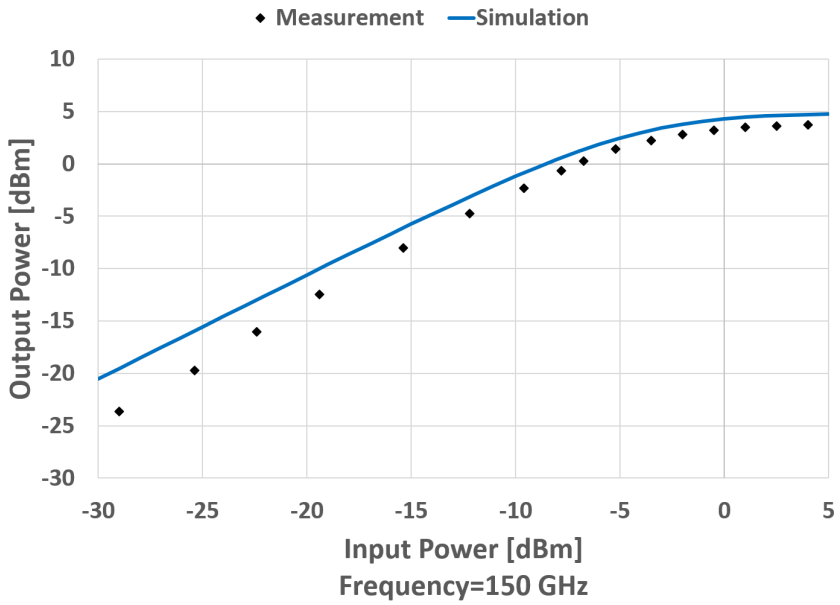

Figure 6. The measured and simulated output power versus the input power of the D-band amplifier.

4. CONCLUSIONS

In this paper, we have presented the designs and measurement results of the D-band amplifier targeted for ultrahigh-speed wireless communications. The proposed amplifier obtains the peak gain of 9.6 dB over the -3 dB bandwidth from 138 GHz to 164.5 GHz. Supplied by the 0.7 V supply voltage, the amplifier consumes the low power of 27.3 mW while its core occupies the chip area of 0.06 mm^2.

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