

1.5-V CMOS Current Multiplier/Divider

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Article Info

Article history:

Received Jan 10, 2018

Revised Mar 14, 2018

Accepted Mar 28, 2018

Keyword:

Analog multiplier
Current-mode circuit
Low voltage
MOS analog circuits
Squarer

ABSTRACT

A circuit technique for designing a compact low-voltage current-mode multiplier/divider circuit in CMOS technology is presented. It is based on the use of a compact current quadratic cell able to operate at low supply voltage. The proposed circuit is designed and simulated for implementing in TSMC 0.25- μm CMOS technology with a single supply voltage of 1.5 V. Simulation results using PSPICE, accurately agreement with theoretical ones, have been provided, and also demonstrate a maximum linearity error of 1.5%, a THD less than 2% at 100 MHz, a total power consumption of 508 μW , and -3dB small-signal frequency of about 245 MHz.

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1. INTRODUCTION

Analog multipliers and dividers are very useful sub-circuits in a wide range of signal processing and conditioning applications, such as, analog computation circuits, fuzzy logic controllers and instrumentation systems [1]. They can also be used in communication systems as a programming circuit element, such as, peak detectors and amplitude modulators [2]. Based on the well known current-mode approach, the current multiplier/divider circuit can achieve low supply voltage, low power consumption, large dynamic range, and wide bandwidth. Accordingly, several recent works on analog CMOS current-mode multiplier/divider circuits have been proposed in the literature [3]-[12]. The design approach takes either the exponential I-V relationship of MOS transistors in weak inversion [3]-[6] or their square-law behavior in strong inversion [7]-[12]. In [3]-[5], the translinear loops with MOS transistors operating in the weak inversion mode are used to implementing multiplication and division. The realized circuits are therefore suitable for low-voltage operation and low-power consumption. However, the main limitation of these circuits is that the input dynamic range is very small. The circuits presented in [6]-[10] are not well-suited for low-voltage and low-power applications. A 1.5-V CMOS current multiplier/divider circuit has been reported in [11]. The circuit is based on the use of four compact voltage-to-current converter cells, and also requires additional circuit components to realize the sum and difference of the two input signals i_x and i_y ($i_x + i_y$ and $i_x - i_y$), which means that the resulting circuit is relatively complex. Additionally, in order to increase an upper -3dB small-signal bandwidth, many analog function circuits can be achieved by utilizing the square-law characteristic of MOS transistors operated in saturation mode [12].

To this aim, we present a compact CMOS current-mode four-quadrant multiplier and two-quadrant divider circuit based on the current quadratic cell. The circuit relies on the square-law characteristic of the MOS transistor operating in the saturation region. The proposed circuit achieves simultaneous multiplication and division operations with no additional circuitry. Simulated results in TSMC 0.25- μm CMOS technology demonstrated that the typical power consumption is only 508 μW from a single 1.5 V supply voltage, and the linearity error is approximately 1.5% for input range up to $\pm 40 \mu\text{A}$. Also, the total harmonic distortion is less than 2% at 100 MHz. Moreover, its -3dB bandwidth of 245 MHz is achievable.

2. CIRCUIT PRINCIPLE AND DESCRIPTION

2.1. Current quadratic cell

Figure 1 shows a current quadratic cell (M_1 - M_4), which is a modified version of the well-known current squaring circuit introduced in [13]. The circuit directly exploits the square-law model of an MOS transistor operated in saturation, described by the following relation:

$$I_D = K(V_{GS} - V_T)^2 \tag{1}$$

where I_D is the drain-to-source current, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, $K = \frac{\mu C_{ox} W}{2 L}$ is the transconductance parameter, μ is the carrier mobility, C_{ox} is the gate capacitance per unit area of the gate oxide, W and L are the channel width and length, respectively. Assumed that all transistors are well matched and biased in the saturation region, the bias voltage V_B is assumed as:

$$V_B = 2V_{GS3} = 2 \left[\sqrt{\frac{I_B}{K}} + V_T \right] \tag{2}$$

where V_{GSi} is the V_{GS} of the transistor M_i (for $i = 1, 2, 3, 4$). Since the drain current I_{D1} of M_1 is equal to $i_{i1} + i_{o1}$, the gate-to-source voltage V_{GS1} can be derived as:

$$V_{GS1} = \sqrt{\frac{i_{i1} + i_{o1}}{K}} + V_T \tag{3}$$

Using Equations (1) to (3), the output current i_{o1} of the squarer of Figure 1 is obtained as:

$$i_{o1} = \frac{(i_{i1} - 4I_B)^2}{16I_B} \tag{4}$$

As apparent, the output current i_{o1} of the cell results in quadratic relation with the input current i_{i1} divided by the bias current I_B .

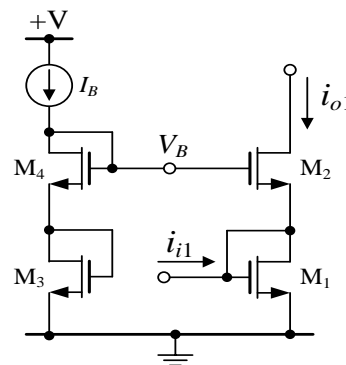


Figure 1. Current squarer cell

2.2. Current follower circuit

Figure 2 shows the basic current follower circuit, which is constructed by n-type current mirror (M_5 - M_6) and p-type current mirror (M_7 - M_8). Assuming M_5 - M_8 to be operating in the saturation region, the drain currents I_{D5} and I_{D7} of the transistors M_5 and M_7 according to Equation (1) can be expressed as, respectively,

$$I_{D5} = K(V_{i2} - V_{TN})^2 \quad (5)$$

and

$$I_{D7} = -K(+V - V_{i2} - V_{TP})^2 \quad (6)$$

where V_{TN} and V_{TP} are the threshold voltage (V_T) of the NMOS and PMOS, respectively. Assume that V_{TN} be identical to V_{TP} , i.e. $V_T \cong V_{TN} \cong V_{TP}$, then the input current i_{i2} is simply given by

$$i_{i2} = I_{D5} + I_{D7} = K[(V_{i2} - V_T)^2 - (+V - V_{i2} - V_T)^2] \quad (7)$$

By the same way as that used to derive i_{i2} , the output current i_{o2} of Figure 2 can be found to be:

$$i_{o2} = I_{D6} + I_{D8} = K[(V_{i2} - V_T)^2 - (+V - V_{i2} - V_T)^2] \quad (8)$$

Thus, Equations (7) and (8) yields

$$i_{o2} = i_{i2}. \quad (9)$$

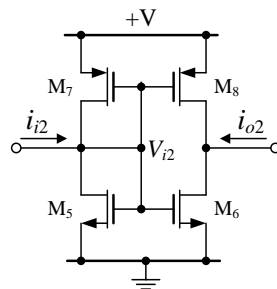


Figure 2. Basic current follower circuit

2.3. Proposed current multiplier/divider circuit

The circuit configuration capable of performing both current multiplication and division is shown in Figure 3. The core elements are the current biquadratic cells M_{1A} - M_{2A} , M_{1B} - M_{2B} and M_{1C} - M_{2C} corresponding to those shown in Figure 1, in which the sharing bias voltage V_B is provided by transistors M_3 - M_4 . The x -input and y -input current signals ($i_{iA} = i_x$ and $i_{iB} = i_y$) and the sum of i_x and i_y ($i_{iC} = i_x + i_y$) for the three squarer cells are generated by the current follower circuits M_{5A} - M_{10A} and M_{5B} - M_{10B} of Figure 2. From the squarer shown in Figure 1, we see that the bias current I_B in Equation (4) is in the denominator. Thus, for the proposed circuit shown in Figure 3, if I_B is considered as the third input i_z , then it can be shown that this circuit may be performed as a current divider. According to Equation (4), the output currents i_{oA} , i_{oB} and i_{oC} of the three squarers in Figure 3 are given by, respectively:

$$i_{oA} = \frac{(i_x - 4i_z)^2}{16i_z} \quad (10)$$

$$i_{oB} = \frac{(i_y - 4i_z)^2}{16i_z} \quad (11)$$

and

$$i_{oC} = \frac{[(i_x + i_y) - 4i_z]^2}{16i_z} \tag{12}$$

The current mirror circuit M_{14} - M_{15} performs signal current summation at an output node. The output current (i_{out}) of this multiplier is therefore:

$$i_{out} = i_z + i_{oC} - i_{oA} - i_{oB} \tag{13}$$

Substituting Equations (10) into (13), we have:

$$i_{out} = \frac{i_x i_y}{8i_z} \tag{14}$$

The equation clearly shows that the circuit of Figure 2 operates as the four-quadrant current multiplication between i_x and i_y , or the two-quadrant current division between i_x (or i_y) and i_z , with the conversion gain of 1/8.

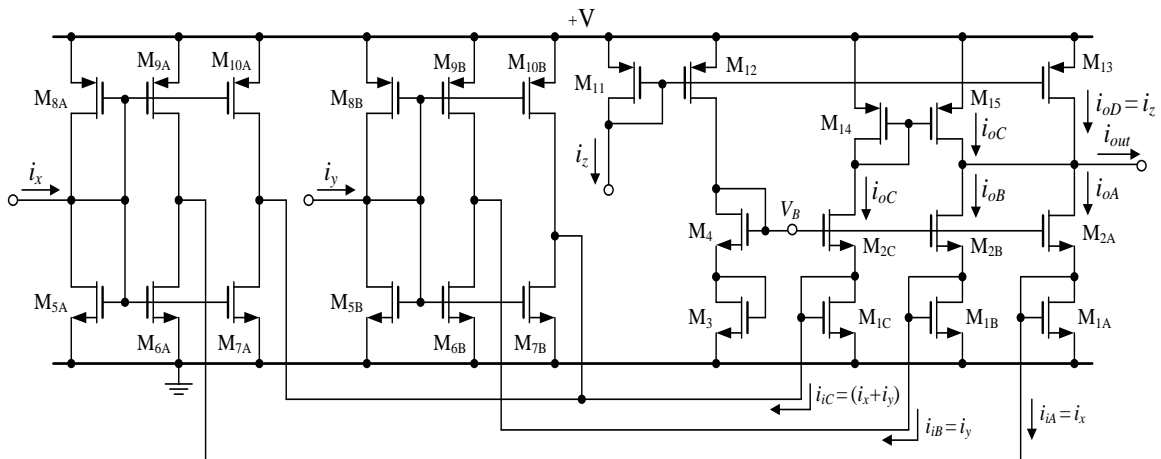


Figure 3. Proposed current-mode multiplier/divider circuit

3. MISMATCH ANALYSIS

This section discusses in detail the important effects of various mismatches introduced in the proposed circuit operation. These effects mainly include channel length modulation, input current mismatch and transistor mismatch. However, practically, the channel effect modulation can be reduced by using long-channel devices. Therefore, the important errors due to the input current mismatch and transistor mismatch are considered in this section.

3.1. Input current mismatch

If the current mirrors consisting of M_{5A} - M_{10A} , M_{5B} - M_{10B} and M_{11} - M_{13} do not work properly, the output currents of these mirrors can be modeled as:

$$i_{iA} = i_x + \Delta_x \tag{15}$$

$$i_{iB} = i_y + \Delta_y \tag{16}$$

$$i_{iC} = (i_x + i_y) + \Delta_{xy} \tag{17}$$

and

$$i_{oD} = i_z + \Delta_z \quad (18)$$

where Δ_x , Δ_y , Δ_{xy} and Δ_z are the mismatch percentages of i_x , i_y , $(i_x + i_y)$ and i_z , respectively. Substituting Equations (15) to (18) into (10)-(13) yields the output current i'_{out} due to input-current mismatching effect as follows:

$$i'_{out} = (1 - \varepsilon)i_{out} + I_{OS}, \quad (19)$$

where

$$\varepsilon = \frac{\Delta_z}{i_z + \Delta_z}, \quad (20)$$

and

$$I_{OS} = \frac{\Delta_x + \Delta_y - \Delta_{xy}}{2}. \quad (21)$$

This result obviously shows that the mismatching effect seems to produce an error (ε) and the output offset current (I_{OS}). From Equation (20), the error ε decreases with increasing the input current i_z . Furthermore, for nominal values of all parameters with $|\Delta_x| \leq 1\%$, $|\Delta_y| \leq 1\%$ and $|\Delta_{xy}| \leq 1\%$, the worst-case estimate of I_{OS} introduced by the input current mismatch is therefore less than 0.5%.

3.2. Transconductance parameter mismatch

In the matched case, transistors M_{1i} and M_{2i} ($i = A, B, C$) of the current squarer circuit in Figure 3 are assumed to be well matched. However, to consider the mismatching effect situation, it is assumed that the transconductance parameters of M_{1i} and M_{2i} are respectively equal to K and $K + \Delta_k$, where Δ_k is the mismatch percentage of the transconductance parameter. With considering this mismatching effect, the output current i'_{out} can be given by:

$$i'_{out} = \delta i_{out} + I_{OS}, \quad (22)$$

where

$$\delta = \frac{\left(1 + \frac{\Delta_k}{K}\right)}{\left(1 + \frac{\Delta_k}{2K}\right)}, \quad (23)$$

and

$$I_{OS} = \left(\frac{\Delta_k}{2K + \Delta_k}\right) i_z. \quad (24)$$

Above relations indicate that the mismatch of K seems to generate the output current deviation (δ) and the offset current (I_{OS}). To evaluate this mismatching effect, considering the typical set of device parameters is, for example, if $|\Delta_k| \leq 1\%$ and $i_z = 40 \mu\text{A}$. The maximum δ and I_{OS} are equivalent to $< 1.1\%$ and $< 0.5\%$, respectively.

3.3. Threshold voltage mismatch

Considering a worst case scenario in which the threshold voltage (V_T) of M_{1i} and M_{2i} are mismatched, for example, $V_{T1} = V_{TN}$ and $V_{T2} = V_{TN} + \Delta_T$ where Δ_T is the percentage variation of V_{TN} . Therefore, including this effect, the output current deviation from that given in Equation (14) will be obtained as:

$$\Delta i_{out} \cong \Delta_T \sqrt{\frac{K}{i_z}} \tag{25}$$

It is evident that the threshold voltage mismatch will contribute leads to the output offset current, which is proportional to i_z .

4. COMPUTER SIMULATION AND PERFORMANCE VERIFICATION

The performances of the proposed current multiplier/divider circuit of Figure 3 were verified by PSPICE simulation with TSMC 0.25- μm CMOS technology. The aspect ratios of all transistors in Figure 3 are provided in Table 1. The supply voltage (+V) used in simulations was 1.5 V.

Figure 4 shows the simulated DC current transfer characteristic of the proposed multiplying circuit of Figure 3, when the input currents i_x and i_y are continuously scanned from $-40 \mu\text{A}$ to $40 \mu\text{A}$ with $10\text{-}\mu\text{A}$ step size. According to the simulation results, the maximum error is around 1.5% for input signal swings up to $\pm 40 \mu\text{A}$, and the maximum power consumption is found to be around $508 \mu\text{W}$, at $i_x = i_y = i_z = 40 \mu\text{A}$. The total harmonic distortions (THDs) of the output current against the input current amplitude at 1 MHz, 10 MHz and 100 MHz are simulated and given in Figure 5. The simulations have been performed by varying the amplitude of i_x from $5 \mu\text{A}$ to $60 \mu\text{A}$, while keeping i_y and i_z constant at $40 \mu\text{A}$ (peak). It can be observed that all the simulated THDs are found to be less than 2% for i_x having peak amplitude as large as $40 \mu\text{A}$ (peak).

Table 1. Transistor Aspect Ratios of the Proposed CMOS Current Multiplier/Divider of Figure 3

Transistors	W/L ($\mu\text{m}/\mu\text{m}$)
$M_{1A} - M_{2A}, M_{1B} - M_{2B}, M_{1C} - M_{2C}$	7/0.25
$M_3 - M_4$	8.5/0.25
$M_{5A} - M_{7A}, M_{5B} - M_{7B}$	17/0.25
$M_{11} - M_{12}, M_{14} - M_{15}$	17/0.25
$M_{8A} - M_{10A}, M_{8B} - M_{10B}$	0.75/0.25
M_{13}	13/0.25

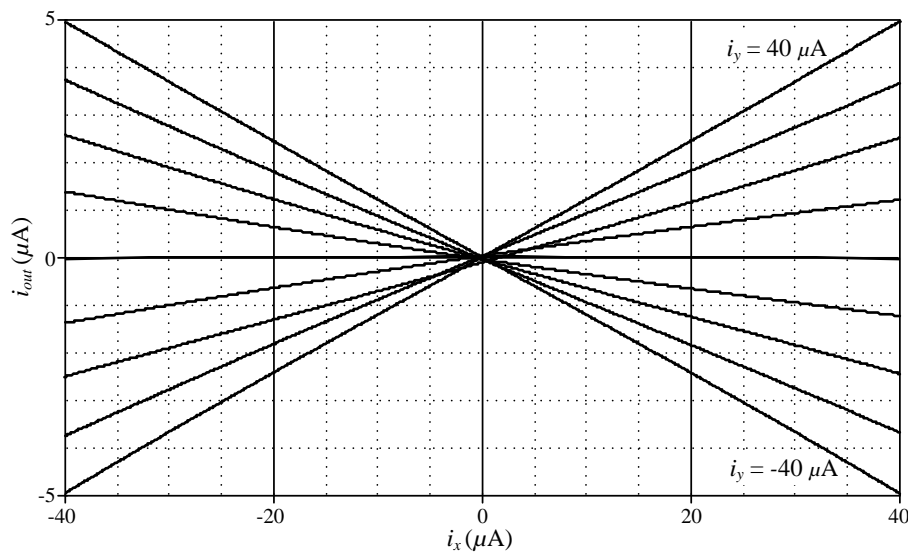


Figure 4. DC current transfer characteristics of the proposed multiplier in Figure 3

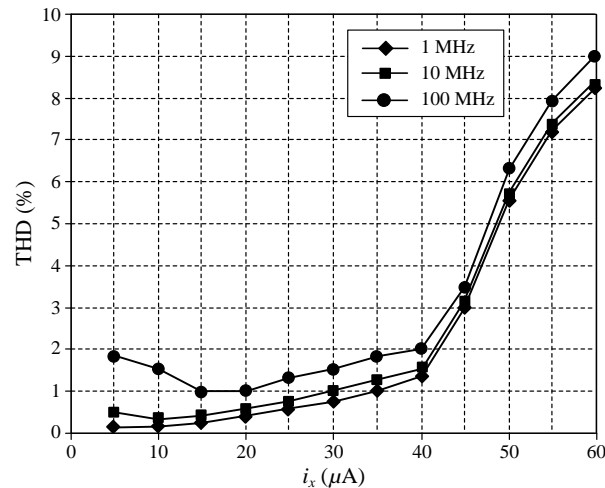


Figure 5. Proposed current-mode multiplier/divider circuit

Figure 6 illustrates the DC transfer function of the proposed current divider circuit under $i_y = 40 \mu\text{A}$, i_z swept from $30 \mu\text{A}$ to $60 \mu\text{A}$, and i_x ranging from $-40 \mu\text{A}$ to $40 \mu\text{A}$ in $10\text{-}\mu\text{A}$ steps. To obtain simulated transient responses of the proposed divider circuit, the input currents i_x and i_y are applied as constant DC currents with amplitude of $40 \mu\text{A}$ (peak), while the input current i_z is a 1-MHz triangle wave with amplitude of $30 \mu\text{A}$ (initial value of i_z is $30 \mu\text{A}$). The resulting output current i_{out} obtained from the simulations is shown in Figure 7. It is seen that the characteristic of i_{out} of the circuit performs approximately the divider operation as expected.

Figure 8 shows the simulated input and output waveforms of the proposed multiplier, when a 1-MHz sinusoidal current signal with an amplitude $40 \mu\text{A}$ was applied to input i_x ($= i_y$) while a $40\text{-}\mu\text{A}$ constant DC current was applied to input i_z . Its output error between calculated and simulated values is also plotted in the lowest trace of Figure 8. The worst-case output error is lower than 0.2%. The proposed current multiplier circuit of Figure 3 was also used to implement as an amplitude modulating operation. From simulations, the input and output waveforms are demonstrated in Figure 9, where a 1-MHz sinusoidal carrier (i_y) is multiplied by a 100-kHz sinusoidal modulating signal (i_x). As seen, the performance of the circuit achieves the multiplication of two current signals properly.

Figure 10 shows the simulation of the circuit's frequency characteristic, when i_x was a sinusoidal current with an amplitude of $20 \mu\text{A}$, while i_y and i_z were constant currents equal to $20 \mu\text{A}$. The result indicates the circuit has a -3dB small-signal bandwidth of approximately 245 MHz.

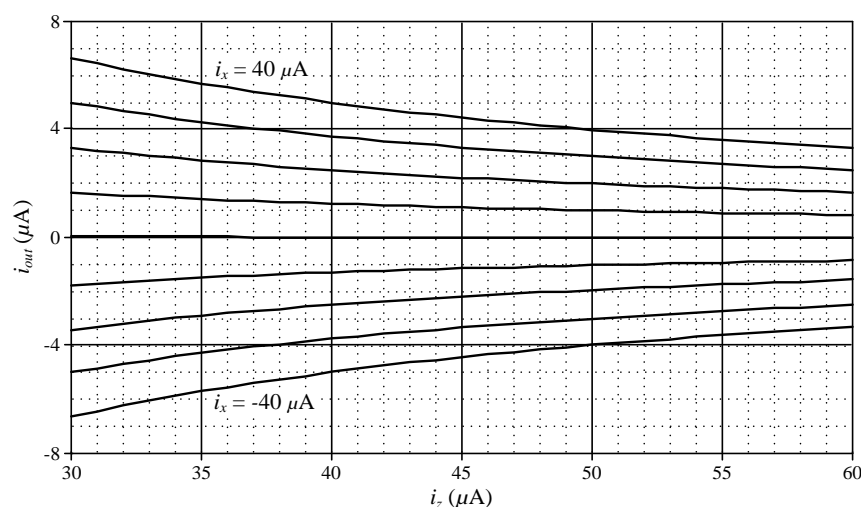


Figure 6. DC current transfer characteristics of the proposed divider in Figure 3

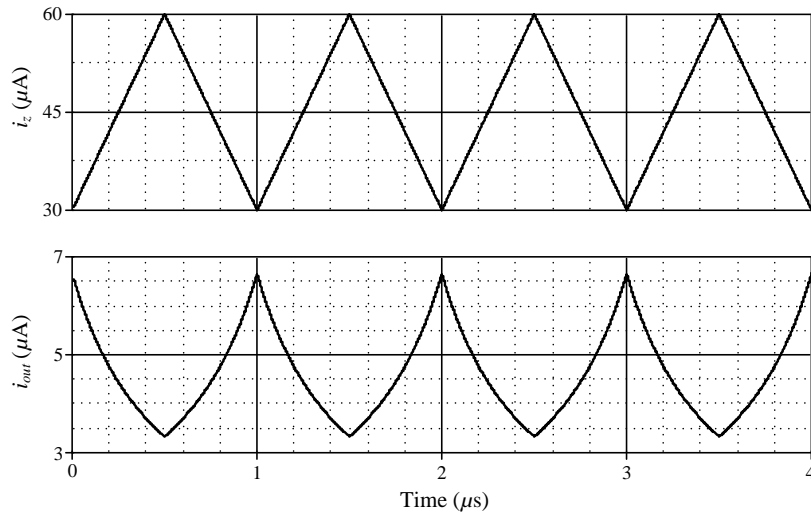


Figure 7. Transient responses of the proposed current divider

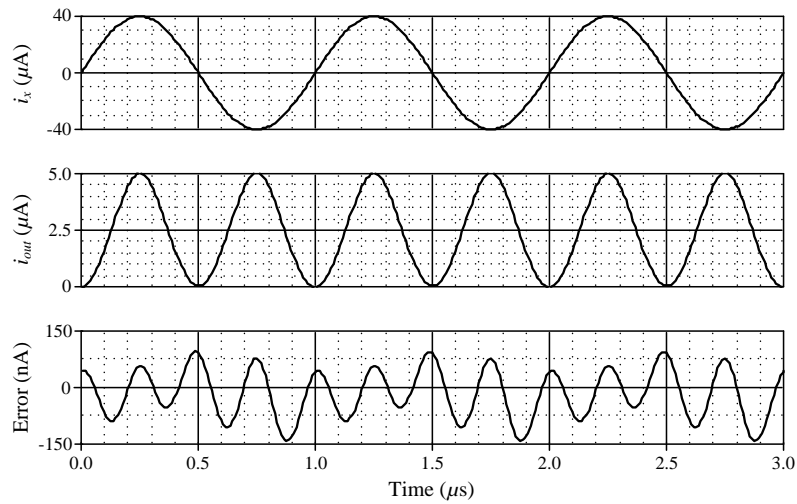


Figure 8. Simulated results of the proposed current multiplier, when performing as a frequency doubler

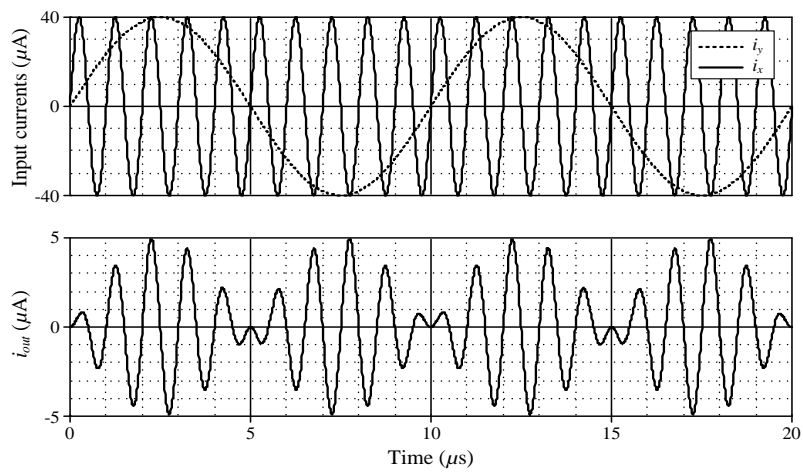


Figure 9. Simulated results of the proposed current multiplier, when performing as an amplitude modulator

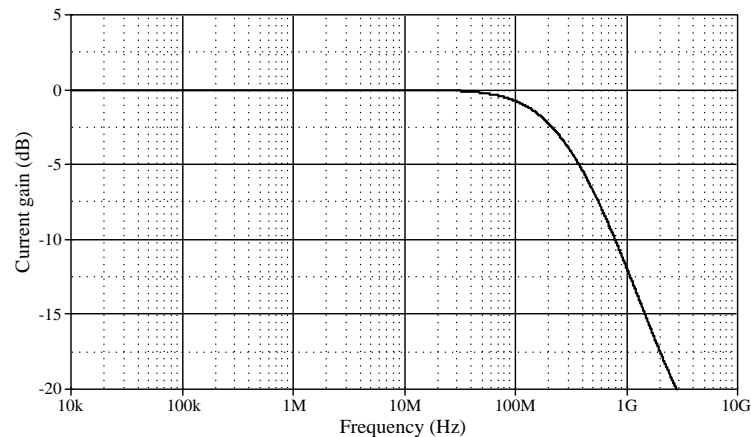


Figure 10. Frequency response of the proposed circuit

5. SUMMARY

In conclusion, a four-quadrant current multiplier and a two-quadrant current divider are presented. It is designed by using a very compact current quadratic cell together with simple current mirrors, allowing low-power, low-voltage and high-frequency requirements. All simulations were performed by PSPICE assuming TSMC 0.25- μm CMOS technology. Simulation results demonstrate that the total power dissipation $< 508 \mu\text{W}$ from a single 1.5 V supply, THD of $< 2\%$ for 40 μA peak, linearity error of $< 1.5\%$, and a small-signal bandwidth of 245 MHz.

ACKNOWLEDGEMENT

This work was supported by King Mongkut's Institute of Technology Ladkrabang Research Fund [grant number KREF116001].

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