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Low Noise Amplifier using Darlington Pair At 90nm Technology

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ABSTRACT

The demand of low noise amplifier (LNA) has been rising in today's communication system. LNA is the basic building circuit of the receiver section satellite. The design concept demonstrates the design trade off with NF, gain, power consumption. This paper reports on with analysis of wideband LNA. This paper shows the schematic of LNA by using Darlington pair amplifier. This LNA has been fabricated on 90nm CMOS process. This paper is focused on to make comparison of three stage and single stage LNA. Here, the phase mismatch between these patameters is quantitavely analyzed to study the effect on gain and noise figure (NF). In this paper, single stage LNA has shown the 23 dB measured gain, while the three stages LNA has demonstrated 29 dB measured gain. Here, LNA designed using darlington pair shows low NF of 3.3-4.8 dB, which comparable to other reported single stage LNA designs and appreciably low compared to the three stages LNA. Hence, findings from this paper suggest the use of single stage LNA designed using Darlington pair in transceiver satellite applications.

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1. INTRODUCTION

Currently, expanding use of high data rate wireless communication systems, high resolution radars, millimeter-wave (mm-wave) trans-receivers, medical devices and other radio communication systems have highlighted the applications of low noise amplifier (LNA) to achieve better sensitivity and low noise figure [1]-[10]. In recent, based on the demand for requirement to amplify very week signal, low noise amplifier (LNA) has been used like signal coming from a satellite [1]-[10]. Power of satellite is very limited and designers want to pick up a 20 watt signal from miles to miles away. The signal is very week because it is coming from long distance, so, designers have to amplify that signal [2], [3]. Designers can't use normal amplifier because normal amplifier itself has noise that can mask the real signal. So Designers have shown to choose LNA which have been suggested to possess less inductors, capacitors and also low noise transistors. A LNA amplifies a very week signal without degrading its signal to noise ratio (SNR) [4]-[6]. Normally LNA generates power gain of 100 (20dB) while decreasing the SNR by a factor of 2. Normal amplifier increases the power of both the signal and noise in signal. LNA minimizes the extra noise [5], [6].

The LNA, which uses complex matching networks is suggested to possess a large number of inductors or transmission lines that may consumes a large chip area and need of large amount of DC power [8]-[17]. In earlier reported topology of LNA, there are discernible problems of requiring a high voltage supply and high power consumption. Further, for a better high data rate, there is need of a maximization of the relative bandwidth at high carrier frequencies. Appreciably in case of mobile

applications, a significant reduction of DC power consumption is favourable. In some instances, maximum gain can be achieved in highest gain mode, but these success compromise the linearity and noise figure [10]-[20]. This paper proposes a three stage LNA using cascode connection. In three stage LNA, two stages are cascode and one is Darlington pair amplifier. This circuit required less power consumption and low voltage supply as compared to the conventional one.

2. RESEARCH METHOD

2.1. Basic staructure of LNA

The low noise amplifier (LNA) is referred as the first participating block in a receiver and LNA has ben suggested to contribute in bringing better performance specifically the sensitivity of wireless communications systems. The cascode architecture has been suggested to bring a significant amount of isolation of input – output. In the next, the transistor M2 separates another component Miller capacitance [1]-[10]. Here, Input Impedance has been shown to be derived from utilizing the source degeneration inductor Ls. Another component Gate inductor Lg initiates the frequency resonance. Further, in the same schematic model, the tuning granularity is shown to be obtained by the network with matching output [8]-[10]. The matching network in the output is the combination of varactor and satellite. The impedance in the load is converted into one parameter of subsequent stage as input impedance by using a LC network [11]. If matching network is properly designed then it transfer the maximum power up to load. If input voltage to the varactor (DC) is varied, then frequency of the output is shown to be matched with a different frequency [12], [13]. Figure 1 shows the basic architecture of LNA.

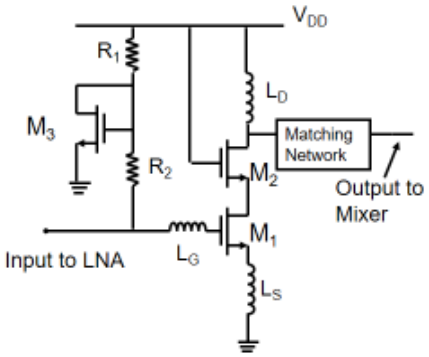

Figure 1. Basic architecture of low noise amplifier

2.2. Noise figure

The variation in the signal to noise ratio (SNR) variation has been suggested to be created due to radio frequency (RF) signal chain component and that variation is measured by NF and noise factor (F) [14], [15]. In case of NF and F, the minimum value is indicated to better performance because such specifications specify the amplifier or radio receiver presentation and capability [16]-[20]. The of noise power in output of any device to the portion of there of attributable to thermal noise in input terminalis called noise factor and at that point the standard value of noise temperature is 290k. Further, the NF has been described as the ratio of original output noise to the remaining noise in a setting, where device is not able to introduce any noise. Further, the signal over noise ratio of input to signal to noise ratio of output may also be described as the NF. Here, the NF or F is denoted by unit decibels (dB) [16]-[20].

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \quad (1)$$

Noise factor as a function of a device

$$NF = \frac{N_{device} + G \cdot N_{source}}{G \cdot N_{source}} \quad (2)$$

G=Power gain of the device.

2.3. CMOS LNA

To confine the decay of the signal-to-ratio (SNR), several reports suggest that high gain and a minimum low NF should be attributed to first stage of an RF receiver for ultra-wideband (UWB) systems [21]. Further, high gain and a low NF LNA have also been indicated to be one of characteristics of LNA [22], [23]. Since the noise specific of the front end of an RF receiver is calculated with the help of LNA.

It has been observed that basic requirements for designing wideband LNAs could be such as flat and wideband gain, high gain and low NF in comparison to complete UWB frequency band at low power consumption. In connection with attachment of an antenna port, it is suggested for wideband 50 Ω input matching [24], [25]. Essentially, three main different methods of wideband matching are available. But, these described topologies have been faced with some difficulties like high NF (the resistive termination, the common gate) and large chip area (the band pass LC filter). In present context, for achieving wideband input matching sparing the above mentioned problems in LNA, there is a preference for calculation of the two frequency matching method. In recent times, researchers have also been reported to be engaged in appreciable with reference to the circuit topologies of wideband LNAs like resistive shunt feedback topologies and distributed topologies. Further, these studies have shown relevance based on their greater wideband characteristics. It is also suggested that resistive shunt feedback amplifiers can demonstrate appreciable wideband input matching and gain [21]-[25].

Here, reported novel method of designing of input matching suggests a spontaneous matching method. Where Darlington-pair is considered to show maximum gain compared to the whole operating band evincing low power consumption. In the current era of technology advancement in wireless communication systems and wireless sensors utilized for Internet of Things (IOT) supported the overwhelming responses for the applications of wideband low noise blocks and thse low noise blocks are shown to deonstarte less chip area and reduced requierement of power [24]-[27].

To suffice the requirements of in wireless communication systems and wireless sensors, RF circuits without inductor are significantly suggested by focusing on the indystry and acamedia need. In a clear comparison to traditional RF circuits, the inductor less RF circuits is suggested to need smaller chip area. Nevertheless, inductor less RF faces some drwbacks as the relatively high NF and low linearity. In consequence, available devices including MOSFETs, resistors, etc., which are suggested to work as an alternate toinductive devices may show high noise power and additionally it may cause supply-voltage headroom issue [26], [27].

2.4. Cascode amplifier

When common emitter stage is coupled with common base stage, the whole configuration is called two stage cascode amplifiers. Above configuration has more input –output isolation, high input impedance. In such configuration, there is suggestion about the output impedance, and higher gain or high bandwidth when compared to single stage amplifier. In current applications cascode can be designed by two transistors (BJT or FET), where common emitter or common source work as the first block and common base or common gate used as the second block. The cascode amplifier enhances the isolation between input and output (reduces reverse transmission). Such observation has been linked to the fact about the absence of coupling between output and input terminal. Hence, such amplifier excludes the chance of Miller effect. Therefore, it may contribute to a significantly enhanced bandwidth [28]. Figure 2 shows the basic circuit of cascode amplifier.

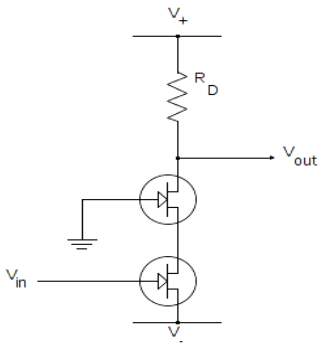

Figure 2. Basic circuit of cascode amplifier

2.5. Circuit diagram

Two frequency matching process is used which is beneficial to get wideband input matching. The design process includes impedance matching at two frequencies simultaneously which is used for wideband input matching. A schematic diagram of the single stage LNA which has wideband is given in Figure 3. The cutoff frequency should be increased to improve the gain at higher frequency and relatively parasitic capacitances should be decreased [12] M1 (160μΩ) and M2 (160μΩ) and W1 (160μm) and W2 (240μm) [12]. In this paper, W1 (150μm) and W2 (300μm) so that W2/W1=2 and we can increase the gain of amplifier with low power consumption. A symbolic representation of single stage LNA used for simulation is presented in Figure 4.

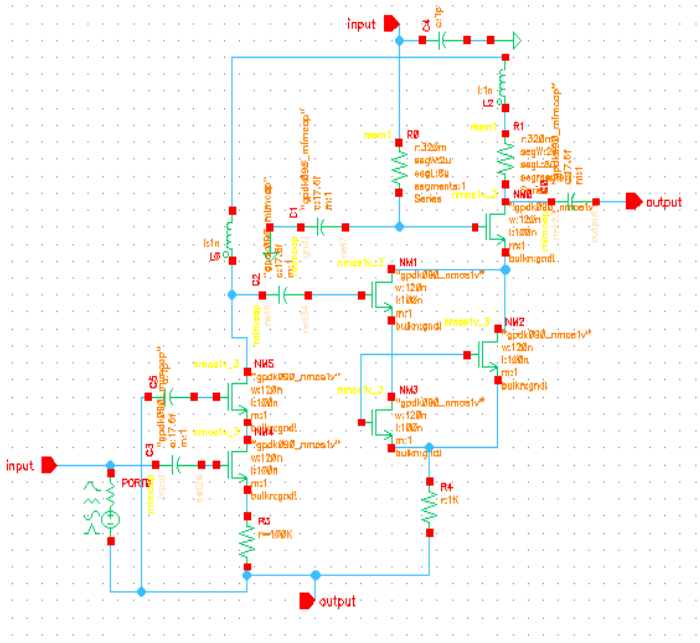

Figure 3. Schematic diagram of the conventional pair amplifier

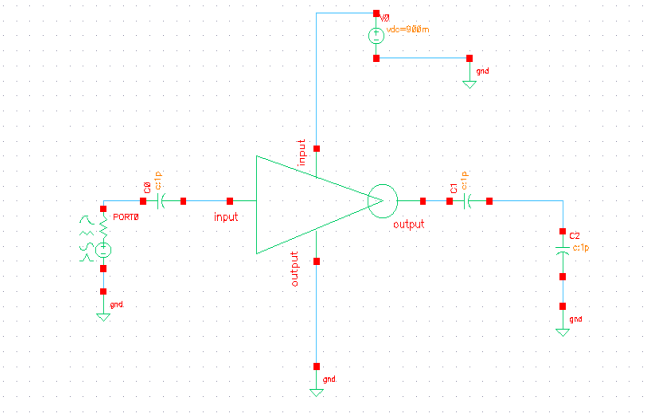

Figure 4. Symbolic representation of single stage LNA used for simulation

In Figure 5, the front end receiver has been shown to have basic block, which is called as LNA. To enhance the receiver chain sensitivity, the LNA should have minimum noise factor (NF). The cascade amplifier that provides better isolation and noise matching with source generation that is inductive and is used LNA. Figure 5 presents the circuit model of the proposed 3 stage LNA. Here, first stage is used for better noise factor i.e. cascade amplifier. The Darlington cascade amplifier is used to obtain high ft and gain in case of subsequent stages.

Further, this schematic model explains that the output matching network of each stage is evenly supplied with a short stub. This short-tub is in next comprehended by micro strip-line inductors to resonance the dependent of transistor to amplify the gain up to 60 GHz. In the above schematic diagram in Figure 6, an input matching network (IMN) is used to do noise matching with capacitor (C1) in series with transmission line inductor (LT1). ACCORDING TO paper 21 M1, LT1, LT2 are set so that to minimize input return loss (S11) and also decrease the NF at frequency 60 GHZ. In this paper return loss is minimized but NF is increased in case of three stage LNA.

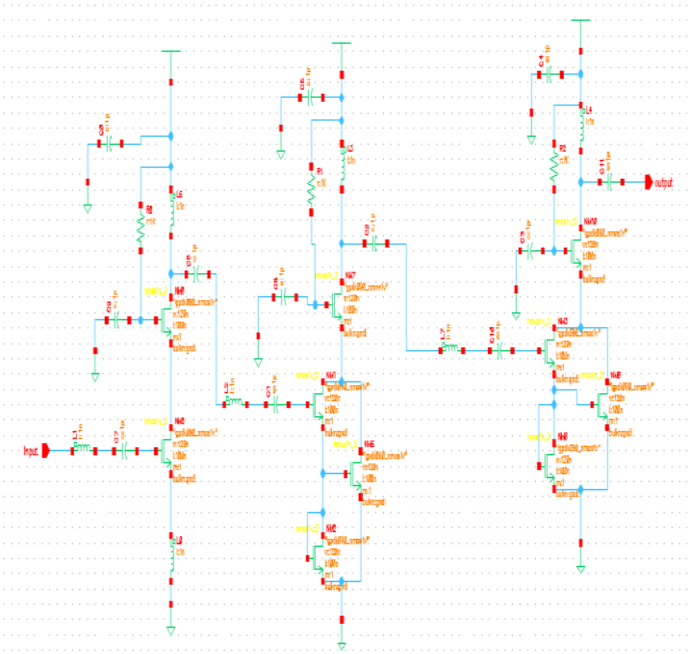

Figure 5. This diagram depicts the representative model of three stage low noise amplifier

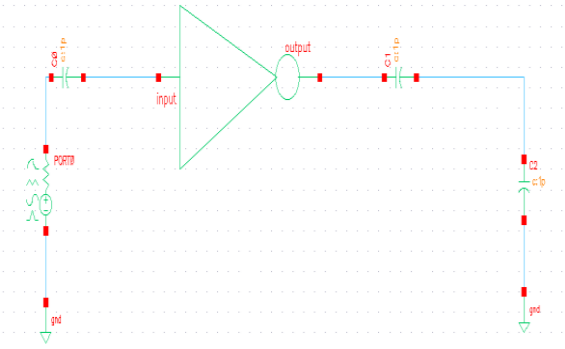

Figure 6. Symbolic representation of 3 stage LNA used for simulation

3. RESULTS AND DISCUSSION

The S parameters of the LNA from 50 GHz are shown to be analyzed by an Agilent N5247A vector network analyser. Further, the S parameters from 67-90 GHz recorded with an R&S ZVA67 vector network analyser plus R&S ZVA-Z90E E-band extension module [30]. In the present paper, S parameter (S11) is calculated at 90nm using cadence virtuoso analog design environment which is shown in Figure 7(a). The maximum gain is 17.7 dB at 67 GHz [30]. In this paper, maximum gain in case of single stage is 23 dB and in case of three stage it is 29 dB. Hence, in our case, we find 32 percent improvement in gain as compared to the previous work reported for single stage LNA [30]. The measured bandwidth of the LNA increases and S parameters (S11 and S22) shift to low frequencies at some extent. This is seen as disadvantages to the single

stage LNA as reported in [30]. At the same time, we report that S parameter (S11) remains constant with respect to frequency level. The measured NF 5.4-7.4 dB and simulated NF is 4.7-5.3 dB. In the present paper, the NF in case of single stage is 3.3-4.8 dB and in case of three stage it is 8.1-8.9 dB. As compared to previous work [30], we report that in case of single stage LNA, there is an improvement of simulated NF by a decrease up to 25%. It is concluded that by increasing the number of stages, NF increases.

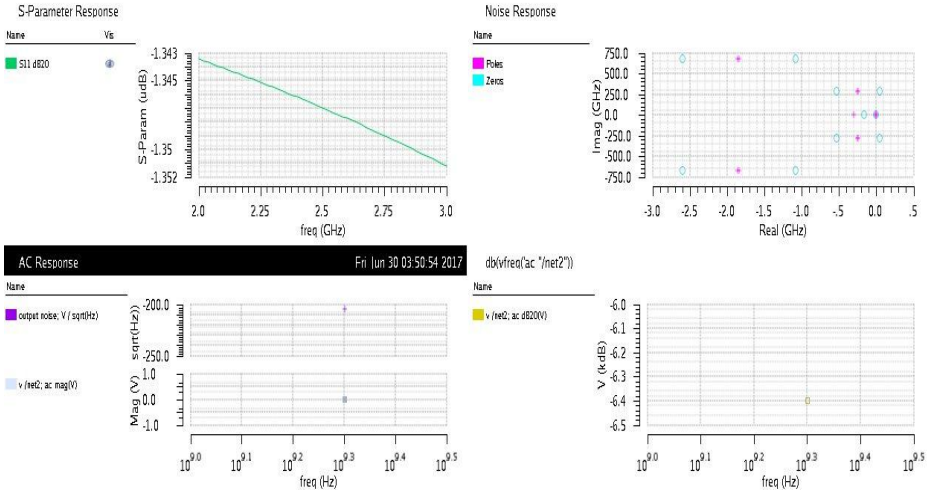

Figure 7. The figure shows the sub window of responses of single stage low noise amplifier. (a) s-parameter (b) pole zero response (c) AC response (d) noise response.

In the present paper, noise responses are also given in Figure 7(b), which shows the number of poles and zeroes in single stage LNA. A reported LNA demonstrates a measured small signal gain higher than 12 dB and measured NF is 6 dB [31]. In a paper, authors report the NF is high and low gain modes are about 5 and 13.5 dB respectively. In the low gain mode, the NF of proposed LNA can become worse [32]. In the present paper, we noticed that in the low gain mode the NF remained constant that shows that single stage LNA is in good condition. The high conversion gain and gain tuning capability are shown to record a large BB signals change compared to a large RF input power range [32]. The present circuit has the highest conversion gain of 47 dB. In case of a circuit consuming 120 mW DC power, a paper reported on the value of the measured minimum NF is 10.7 dB (double side band) is among the lowest reported values when circuit consumes 120 mW DC power. In our case, we found the NF of single stage LNA of 3.3-4.8 dB, which makes it relevant and useful. A circuit of 190 GHz receiver is designed using LNA and integrated in a 130 nm SiGe BiCMOS technology [33].

The high gain of LNA lowers the NF of an overall receiver [2]. The chosen gate widths of the Darlington pair amplifier are 160 µm (M1), 160 µm (M2), 80 µm (M3) [2]. In this paper the chosen gate widths of the Darlington pair amplifier are 180 µm (M1), 180 µm (M2), 90 µm (M3). The NF of the LNA is 2.85-4.5 dB and gain is 21DB [2]. In this paper the NF in case of single stage is 3.3-4.8 dB and gain is 23dB.

A LNA is suggested to include a minimum NF for heightened sensitivity of the receiver chain. As suggested earlier, the cascade amplifier can obtain a better NF than the Darlington cell. Because, the Darlington cell enhances fT and current gain which is equivalent to the bias current, the Darlington cell cascade amplifier displays better gain in comparison to the cascade amplifier [1]. In this paper Darlington amplifier is used to design LNA to increase the gain and lower down the NF and observed NF is 7.1-8.2dB [1]. In the present paper, we obtained NF of value 8.1-8.9 dB which is supported by other reported three stage LNA [1]. From Table 1, it is concluded that the NF is increased in amplifier if we increase the number of stages and gain flatness is also tough but gain and bandwidth is improved and SNR is also decreased. So, single stage LNA is preferred if we need low NF especially in case of satellite communication.

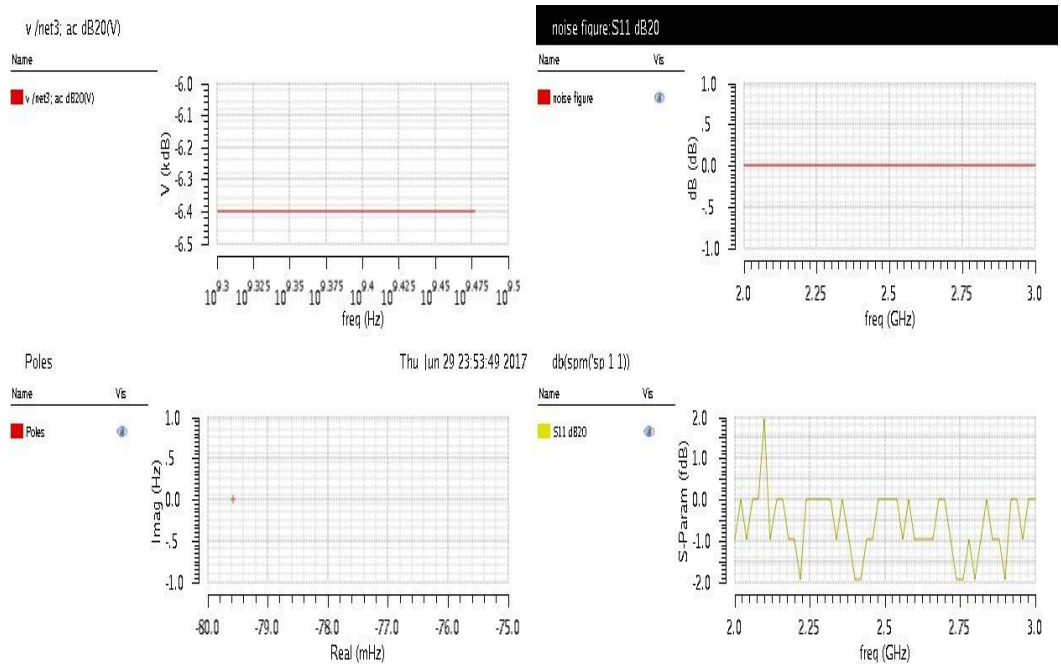

Figure 8. The figure shows the sub window of responses of three stage low noise amplifier, (a) s-parameter (b) pole zero response (c) AC response (d) noise response.

Table 1. This Table Compares and Relates the Reported Data with Newly Measured Data. These Values are Calculated by Expending Calculator on Cadence Analog Tools of GPDK 90nm Technology

Parameter	Single stage paper [1]	Three stage paper [2]	Proposed work single stage	Proposed work three stage
POWER GAIN (db)	21	28	23	29
BANDWIDTH (ghz)	8	14	7	15
NOISE FIGURE (db)	2.85-4.5	7.1-8.2	3.3-4.8	8.1-8.9
Process	180nm Cmos	90nm Cmos	90nm gpdk	90nm gpdk

4. CONCLUSION

Compares the three stages LNA and single stage LNA. Numerous significant constraints of respective amplifiers are calculated based on simulation outcomes and the consequences are presented in this paper for a fast qualitative comparison. Power gain of single stage LNA is 23dB and of three stages is 29db. Noise figure of single stage LNA is 3.3-4.8dB and that of three stages LNA is 8.1-8.9dB. Bandwidth of single stage LNA is 7GHz and that of three stages is 15GHz. This finding supports several existing attempts to design LNA with low noise figure and high bandwidth and showing potential applications in transceiver design. This paper proposes a three stage LNA using cascode connection. In three stage LNA, two stages are cascode and one is Darlington pair amplifier. This circuit required less power consumption and low voltage supply as compared to the conventional one.

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