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Current Comparison Domino based CHSK Domino Logic Technique for Rapid Progression and Low Power Alleviation

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ABSTRACT

The proposed domino logic is developed with the combination of Current Comparison Domino (CCD) logic and Conditional High Speed Keeper (CHSK) domino logic. In order to improve the performance metrics like power, delay and noise immunity, the redesign of CHSK is proposed with the CCD. The performance improvement is based on the parasitic capacitance, which reduces on the dynamic node for robust and rapid process of the circuit. The proposed domino logic is designed with keeper and without keeper to measure the performance metrics of the circuit. The outcomes of the proposed domino logic are better when compared to the existing domino logic circuits. The simulation of the proposed CHSK based on the CCD logic circuit is carried out in Cadence Virtuoso tool.

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1. INTRODUCTION

The Complementary Metal Oxide Semiconductor (CMOS) technology becomes a major part in advanced process of Very Large Scale Integration (VLSI) applications. It increases the leakage current, shows improvement in scaling and enhances the sensitivity which makes the factor fluctuations as barriers of scaling technology in CMOS. As per the improvement of wireless portable systems with the speed of microprocessors and less budget on power the VLSI circuit is rapidly integrated. In the transistor technology, the supply of power simultaneously scaled down and achieves less consumption of power and faster. As well as the threshold voltage is lesser in the similar proportionate. The threshold voltage scaling in exponential provides less immune of noise and improves the sub threshold leakage current in the transistor. In the dynamic node, the dynamic capacitance and supply voltage of domino logic reduces the storage of charges. As per the synchronized factor, the technology scaling is deceased by the substantially of domino gate immunity noise. The high leakage makes the system as difficult due to parallel process of the path evaluation.

The wide fan-in domino has become difficult if there is high immunity of noise and leakage. It happens due to the parallel process and the charge leakage from the node of pre-charge. In the dynamic node, the keeper transistor is prevented by employing the undesired discharging because of charge sharing and leakage current of pull down network. It processes during the phase of evaluation and progresses the robustness by upsizing between the network evaluation and transistor. Also it enhances the delay of the circuit, shows improvement in power consumption and performance. Therefore, the delay and power are considered by compromising the leakage current, upsizing the keeper and noise improvement. The keeper ratio (K) is defined as the ratio of the product of electron mobility and aspect ratio of the keeper transistor to the product of hole mobility and aspect ratio of the evaluation network.

$$K = \frac{p * \left(\frac{W}{L}\right) Keeper\ Transistor}{n * \left(\frac{W}{L}\right) Evaluation\ Transistor} \quad (1)$$

Where, the transistor size is represented as L and W, the mobility of hole and the mobility of electron is denoted as p and n respectively.

The technology of ultra-deep sub-micrometer is developed for the application of wide fan-in and implemented using CCD logic. The CCD logic concept is shown in Figure 1. Due to the replacement of full adder instead of half adder is considered for the reduction of multiplier of power leakage. So, there will not be any separate unit of final summing. The multiplexer is implemented instead of OR gate. The issues in the existing are the noise immunity, leakage current, power consumption, robustness degradation due to contention current and delay. Hence, the power total leakage is reduced by the implementation of CCD. In this paper, the CHSK domino logic is implementing with the CCD for the improvement of noise immunity, power consumption, and speed process. The CCD is combined with the CHSK circuit for the control process of the circuit and improvement of noise immunity and leakage.

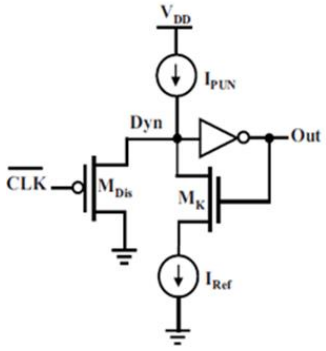

Figure 1 Current Comparison Domino Concept

A new technique of comparison mirror current was proposed for wide fan-in gates with low leakage and better noise immunity. In this technique, the parasitic capacitance was diminished on the dynamic node resulting in smaller keeper to execute speedy and robustness in circuits. So the contention current and power consumption is reduced with degradation in delay. Because of the footer transistor in diode configuration the leakage current is decreased leading to high noise immunity [1]. The mixed high speed domino logic was designed to enhance the performance metrics. The CHSK domino logic is a combination of high speed and conditional keeper domino logic techniques designed with multiplex, which yields better results compared to existing domino logic [2].

A domino logic technique is designed to meet the critical concern of the VLSI era with convenience and high microelectronic devices, power consumption of the digital circuit. The Filtered Switch Domino and Multi Dynamic Node Domino are designed to measure the parameters like power, area and delay. For further improvement both the techniques were combined and results have been deliberate. Multi dynamic nodes are introduced for reducing switching activity in the circuit and power dissipation. The Multi Dynamic Filtered Switch Domino result shows high performance in the trade-off parameters when compared to the existing domino logic systems [3]. The domino logic circuit design techniques are suitable for highly performing circuits for its higher speed and uniqueness of area in comparison with Static CMOS Circuits. Stacked transistor dual threshold voltage technique abates the sub threshold leakage current which in result power consumption also reduced significantly. The sleep switch dual threshold voltage technique shows better reduction in power, improvement in delay and reduction in area in contrast with standard dual-Vth domino logic. The high speed domino logic circuit shows excellent reduction in power, enhancement in propagation delay and power delay product was improved significantly. The conditional keeper domino logic circuit improves speed and also maintains the noise immunity. The diode footed domino logic improves the robustness when compared to standard footless domino and conditional keeper domino under the same delay [4], [18].

The domino logic circuits are applied in modern digital VLSI circuits because of its design cost is low, implementation is simple and outcome affords better performance. Generally domino logic gates consume high dynamic switching activity and leakage power but exhibits low noise immunity in comparison with static CMOS [5]. The domino logic circuits are widely used in digital design applications for its power

efficiency. The idea of the newly designed technique is to consume less power and to overcome conflict problem, which results in reduced power dissipation and offers high noise immunity. The outcomes of the proposed design shows low power consumption and circuit speed is increased significantly [6].

The dynamic gates have the drawback of low noise margin in comparison with standard static logic gates. The problem can be resolved by introducing PMOS keeper transistor in the pull up network which balances the sub threshold current of pull down NMOS network. A current comparison based domino logic circuit was designed to track the threshold voltage variation using single current mirror in the dynamic node. The parasitic capacitance also reduced significantly on the dynamic node [7]. In energy efficiency and high speed operation circuit design dynamic logic styles have been utilized because of its usage of transistors count is less and speedy comparing to CMOS logic circuits. Due to its less noise tolerant domino logic styles are not extensively used in all kind of circuit design [8]. The dynamic power and abstaining reliability problems will be reduced when the power supply voltage was trimmed down. The consumption of power in highly performing circuits has climbed to the level where it enforces the most important limitation to the rising performance and functionality. The foremost factor in CMOS technology based design is dynamic switching power which can be reduced by reducing the supply voltage [13 - 14]. If the supply voltage is reduced then it automatically reduced the transistor current which affects the speed of the circuit. The threshold voltages are scaled down so that it will compensate the speed of the circuit which was affected because of lowering the supply voltage. It also helps to maintain the dynamic power consumption with sufficient level without affecting the performance of the circuit. As a result of threshold voltage reduction the sub threshold leakage current starts increasing exponentially [15]–[17].

A new design technique is proposed for low leakage and noise immune for wide fan-in domino circuits. The proposed design technique utilizes the pull down network's comparison and difference between the switching current of the ON transistor and leakage current of OFF transistor to have a control over the PMOS keeper transistor. The results reduce the conflict between pull down network and keeper transistor. The performance of the current mirror is enhanced due to the usage of stacking effect which reduces the leakage current [20 - 21]. The CMOS domino circuit is designed with a single clock edge to turn on all the gates in the circuits at once which involve the dynamic gates in it. Because of this complex clocking scheme is avoided and complete inherent speed of the dynamic gate is utilized. So this makes the proposed design is significant in which gates are complex and have high fan-out [22]–[23].

2. RESEARCH METHOD

In this section, the design and implementation of proposed logic with and without keeper are explained with its process. Here, the design of the logic is carried out with the combination of CCD logic and CHSK domino logic. The proposed circuit is designed and implemented to exhibit the better improvement in terms of power consumption, faster and less immunity of noise. In order to overcome the existing issues, the proposed circuit is designed by combining the CHSK in company with CCD and more transistors are connected in series. The flow of input terminal to the output terminal is considered in evaluation phase.

The CHSK domino logic and CCD logic are combined and the process is considered as per the logic, in which the CHSK is based on the CCD logic. The control flow of the circuit and the reduction of noise immunity reduction are improved by implementing the CCD in the CHSK. According to the large size of dynamic node capacitance the speed is decreased dramatically. The high speed domino logic and conditional keeper domino logic has been combine together to obtain the logic circuit of CHSK. In CHSK, the MUX function is used as a replacement for of OR logic gate. The results produce better noise immunity and the rapid process was achieved. Figure 2 shows the proposed circuit schematic diagram.

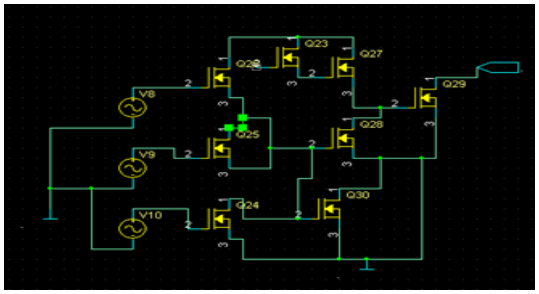

Figure 2 Schematic Diagram of CCD based CHSK with Keeper

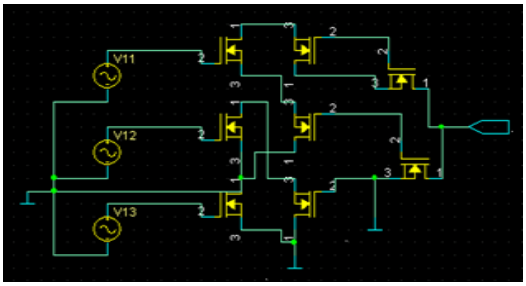

Figure 3 Schematic Diagram of CCD based CHSK without Keeper

Figure 2 shows the schematic diagram of the CCD based CHSK with Keeper and Figure 3 shows the schematic diagram of the CCD based CHSK without Keeper. In the evaluation phase, the assumption of clock signal is considered if the node is low, then it is said to be in standby mode. During the precharge mode, the PMOS transistor will turn off due to swapping of clock signal from low to high. By turning off the PMOS transistor the source voltage will get decreased. Also, the sub threshold of current leakage will decrease by means of the stacking effects and the source voltage of gate will decrease if the direct current voltage is increased. In CCD logic, the transistor of keeper is upsized and improves the robustness of noise, delay and power consumption due to large conflict. In order to overcome this issue, the function of logic is implemented and the transistor separated the functions, then it compares with the leakage of current in worst case. In order to decrease the consumption of power the reference current is added with the transistor in series during the voltage fall to ground.

Then the reference voltage generating is another issue which varies the current reference as per the flow of circuit in order to preserve the circuit robustness. The effects on threshold voltage will affect the gate speed, noise immunity and the power consumption accordingly. In the pre discharge phase of the proposed circuit, the clock voltage and the input signal is in the level of low and high respectively. The dynamic node and voltage fallen to the level of low by the discharge mode of transistor and rise to high by the pre-charge mode. Therefore, the transistor will be on and off according to the flow of the circuit to provide output. Here, the inverter output will raised the output voltage to the level of high.

In the evaluation phase of proposed circuit, the voltage clock will be high and the input will be low. Here, the discharge and the pre-charge will be in off mode and remaining will be in on mode. Also, the transistor keeper can be off and on according to the voltage of input. So the states occurred are as state that remains the input signal at high level and another is at least one input will be in the level of low. During the high level, the voltage is recognized across transistor because of current leakage and also it is mirrored by the next transistor. If the keeper is in another stage then it remunerated the current leakage emulated. So that, the mirror ratio is increases the speed because of the current copied higher at the degradation expense of noise immunity.

3. RESULTS AND ANALYSIS

In this section, the proposed domino logic technique simulation results and analysis of performance metrics are carried out with the comparison of existing domino logic techniques. The proposed domino logic technique circuit analysis is simulated at operating voltage of 0.7 Volts. The proposed circuit's garbage input/output is consummate using the virtuoso tool of the cadence and the outputs are simulated. The analysis of proposed domino logic shows the improvement in the reduction of power consumption and noise immunity. Also, the operation mode and logic circuit comparison with existing system is defined to prove the efficiency and better performance. The performance metrics comparison was carried out with proposed domino logic and different types of existing domino logic and the values were illustrated. Table 1 shows the comparison of various domino logic circuits with the proposed domino logic.

Table 1 Comparison of Various Domino Logic Circuits with the proposed domino logic

Domino Circuit	No of Transistors	Power (μw)	Delay (ns)	UNG (v)	PDP (μw*ns)*10^{-3}
Standard footless	36	286.41	27.8	0.2625	7.96
FSD	42	48.25	78.03	0.5293	3.53
MDND	46	52	77.54	0.4625	4.497
MDFSD	46	89	79.02	0.4259	7.032
HS Domino	42	518.89	27.59	0.2619	14.318
Conditional keeper	47	540.67	31.72	0.2773	17.153
Proposed HS Domino	10	335.42	5	0.3911	1.677
Proposed CK Domino	16	217.71	12	0.5293	2.612
CHSK with Keeper	23	511.43	19.63	0.2526	10.039
CHSK without Keeper	19	510.1	19.93	0.2719	10.166
CHSK – CCD with Keeper	17	234.86	13.85	0.2135	8.34
CHSK – CCD without Keeper	17	228.54	12.05	0.2015	8.56

The results obtained from the proposed circuits have been tabulated and compared with the existing circuits and its graphical representation has been plotted. The performance metrics like Transistor Count, ower, Delay and Unity Noise Gain are included for the performance measurement. Fig. 5 shows the graphical representation of the domino logic styles and transistor count.

Figure 5. Domino Logic Style Vs Transistor Count

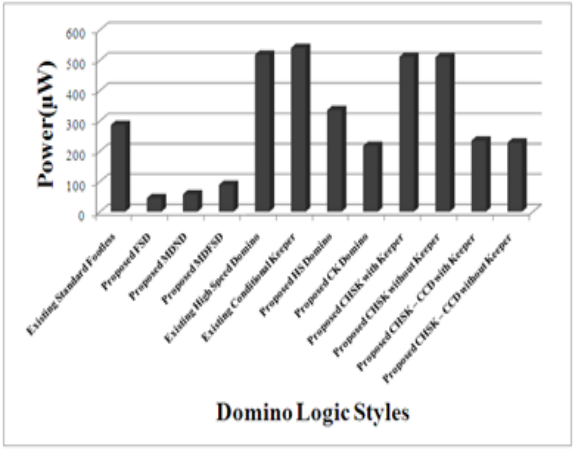

Figure 6. Domino Logic Style Vs Power

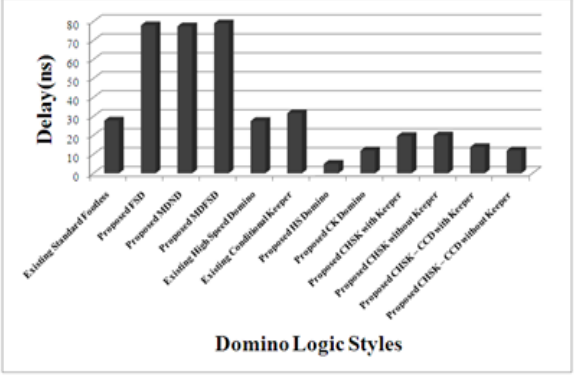

Figure 7. Domino Logic Style Vs Delay

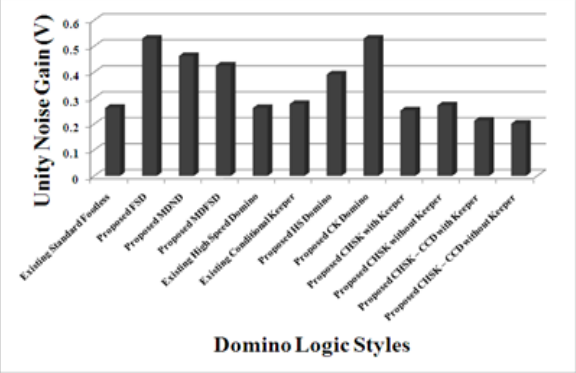

Figure 8. Domino Logic Style Vs Unity Noise Gain

4. CONCLUSION

In this paper, a new circuit technique of CHSK – CCD logic is proposed to provide better robust, reduced delay, enhanced power consumption and unity noise gain. The intent of the circuit is to attain a less leakage current and less power consumption. The reduction in delay and power consumption is carried out by combining CHSK and CCD logic. The simulation results of the proposed domino logic circuit shows the analysis of performance metrics like Power, Delay, Transistor Count, Power Delay Product and Unity Noise Gain. From the analysis of the proposed circuit raises the circuit efficiency with the reduction in noise immunity and power consumption comparing with existing techniques.

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