

A CORDIC based QR Decomposition Technique for MIMO Detection

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Article Info

Article history:

Received Aug 2, 2017

Revised Jan 3, 2018

Accepted July 27, 2018

Keyword:

CORDIC

FPGA

Givens rotation

MIMO

QR decomposition

ABSTRACT

CORDIC based improved real and complex QR Decomposition (QRD) for channel pre-processing operations in (Multiple-Input Multiple-Output) MIMO detectors are presented in this paper. The proposed design utilizes pipelining and parallel processing techniques and reduces the latency and hardware complexity of the module respectively. Computational complexity analysis report shows the superiority of our module by 16% compared to literature. The implementation results reveal that the proposed QRD takes shorter latency compared to literature. The power consumption of 2x2 real channel matrix and 2x2 complex channel matrix was found to be 12mW and 44mW respectively on the state-of-the-art Xilinx Virtex 5 FPGA.

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1. INTRODUCTION

Multiple-Input Multiple-Output (MIMO) technique plays a vital role in current day wireless communication systems to reach higher data rates, improved reliability, high throughput and capacity [1]. In [2], different channel models for MIMO were simulated. Although there is a quite a lot of performance improvement, the complexity of the receiver increases significantly. In order to reduce the complexity of algorithms for MIMO detection, QR decomposition is of critical importance. It decomposes the channel matrix H into orthogonal matrix Q and an upper triangular matrix R . The QR decomposition is performed every time the channel impulse response changes significantly. Noise enhancement problem is greatly reduced in QR decomposition due to the property of unitary transformations, thus minimizing the chance of erroneous detection arising from noise. Successive Interference Cancellation (SIC), V-BLAST and tree search based detection algorithms utilize these matrices to detect the received complex-valued signal vector.

QR decomposition technique can be computed using several methods. They are Householder transformations, Givens rotations and Gram-Schmidt orthogonalization. These transformations can be made easier with CORDIC algorithm [3] leading to low-complexity solution for hardware realization. In small scale MIMO detector, the channel matrix size is small and requires a lower processing speed for QR decomposition. So, in these systems parallel systolic array processors with reduced dimensions are not justified to be used. In [4], Lin discussed QR decomposition based on Givens Rotation with CORDIC algorithm. Hwang in [5] implemented complex QR factorization based on Givens rotation for real-time detection of MIMO signal and also several hardware reduction techniques like constant multiplier sharing and look-up table elimination for CORDIC modules were devised. High speed hardware multipliers were evaluated in [6]. Nazar in [7] discussed low complexity hardware architecture for QR decomposition.

Therefore, the objective of this paper is to propose a QR Decomposition (QRD) module for square channel matrices based on Givens rotation method which allows low complexity decomposition of the

channel matrices, by reducing the number of computations. The Givens rotation of the channel matrix was performed using CORDIC module designed with Xilinx System Generator Block set to reduce the hardware complexity and power consumption. The proposed QRD module can be used as a pre-processing unit in MIMO detection unit.

In Section 2, the block diagram of MIMO system is explained. Section 3 briefs the basic CORDIC algorithm, its different operating modes and the pipelined and scaled implementation using Xilinx System Generator. Section 4 describes the proposed QRD module and its implementation. VLSI architecture implementation results are discussed in Section 5. Section 6 concludes the paper.

2. RESEARCH METHOD

Consider a MIMO system, with M transmit antennas and N receive antennas, with the assumption that $N \geq M$. The complex baseband equivalent model for the considered flat fading MIMO wireless channel yields an N -dimensional received vector $y = [y_1, \dots, y_N]^T$ given by the equation

$$y = Hs + n \quad (1)$$

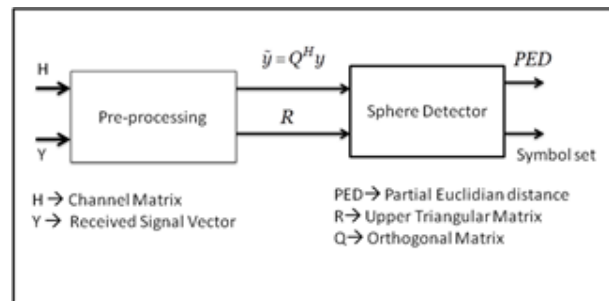


Figure 1. MIMO Detection unit

where H is the $N \times M$ complex valued channel matrix, $s = [s_1, \dots, s_M]^T$ is the transmitted signal vector and n is the additive noise vector. Figure 1 shows the MIMO detection unit containing the pre-processing unit and the sphere detector unit. Most of the detection algorithms for MIMO systems start by decomposing the channel matrix H into unitary matrix Q and an upper triangular matrix R . The pre-processing unit performs the QR Decomposition in the detector and then the received signal vector is rotated by Q matrix as $y' = Q^H y$ and fed to the detector unit.

3. CORDIC ALGORITHM

CORDIC (COordinate Rotation Digital Computer) algorithm can perform several computations like trigonometric, logarithmic and hyperbolic functions, real and complex multiplications, square-root, division, Eigenvalue estimation, QR decomposition and many other functions using simple shift and add operations [8]. CORDIC may not be fastest but it is drawing attention due to its simple hardware implementation and once designed it can be used in all the previously mentioned applications. In this section, the basic principles of CORDIC algorithm and its different modes are discussed. The main concept used in CORDIC algorithm is (i) to decompose the rotations into a sequence of elementary rotations by predefined angles that could be implemented with minimum hardware resource utilization and (ii) to avoid arithmetic operation for scaling such as square-root and division and also by considering the fact that the scale-factor contains only the magnitude information but no information about the rotation angle. There are basically two operating modes namely vectoring mode and rotation mode.

3.1. Vectoring Mode

The CORDIC unit rotates the input vector with the required angle in the vectoring mode, in order to align the result vector with the x -axis. The rotation angle and the scaled magnitude of the input vector i.e., the x -component are the output of the vectoring mode. The y -component of the input vector is minimized at each

micro-rotation and the sign of the y-component is used to determine the direction of the next rotation. In vectoring mode, the equations are written as [9], [3]:

$$x_{i+1} = x_i - y_i d_i 2^{-i} \quad (2)$$

$$y_{i+1} = y_i + x_i d_i 2^{-i} \quad (3)$$

$$z_{i+1} = z_i - d_i \tan^{-1}(2^{-i}) \quad (4)$$

where $d_i = +1$, if $y_i < 0$, -1 otherwise.

3.2. Rotation Mode

In rotation mode, the CORDIC unit is useful for performing vector rotations of the given input vector. First, the desired rotation angle is initialized with input. After each iterative rotation, the magnitude of the angle is made to diminish and the decision is based on the sign of the angle after each step. In rotation mode, the equations are given by

$$x_{i+1} = x_i - y_i d_i 2^{-i} \quad (5)$$

$$y_{i+1} = y_i + x_i d_i 2^{-i} \quad (6)$$

$$z_{i+1} = z_i - d_i \tan^{-1}(2^{-i}) \quad (7)$$

where $d_i = +1$, if $y_i < 0$, -1 otherwise.

3.3. Pipelined CORDIC unit

The vectoring CORDIC unit is connected in pipeline to attain rotation close to the nulling axis. The number of iterations or pipeline stages for sufficient accuracy was found by manual calculations and by Zahid Khan in [10] as 13. The x component i.e. the output of vectoring mode is scaled by constant $K=0.6057$ [11]. Similarly, the rotation CORDIC unit is connected in pipeline to obtain accurate rotation of the x- component and the y-component and both are scaled by scaling constant K.

4. PROPOSED QR DECOMPOSITION MODULE

The Givens rotation of a 2x2 real-valued channel matrix is given by Huang in [12] as

$$\begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \sqrt{h_{11}^2 + h_{21}^2} & h_{12}' \\ 0 & h_{22}' \end{bmatrix} \quad (8)$$

Equation 8 can be implemented using a pipelined and scaled vectoring CORDIC unit followed by pipelined and scaled rotation CORDIC unit. The CORDIC vectoring unit normalizes the first column of the real 2x2 channel matrix and calculates the rotation angle θ which is used to rotate the second column of the matrix. The resultant first and second column elements form the upper triangular matrix R. The rotation angle θ is used to rotate the identity matrix to generate the Q matrix. Figure 2 shows the block diagram of the proposed QRD module.

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \xrightarrow{\text{vectoring}} \begin{bmatrix} \sqrt{h_{11}^2 + h_{21}^2} & h_{12} \\ 0 & h_{22} \end{bmatrix} \xrightarrow{\theta(\text{rotation})} \begin{bmatrix} \sqrt{h_{11}^2 + h_{21}^2} & h_{12}' \\ 0 & h_{22}' \end{bmatrix} \quad (9)$$

The second column of the channel matrix and the two columns of the identity matrix are fed consequently using buffer and reshaping units. Similarly, the output of the second column and the two columns of Q matrix are obtained by buffer unit. The proposed QRD module eliminates division, squaring

and square root operations which lead to area optimization and less power consumption in hardware implementation.

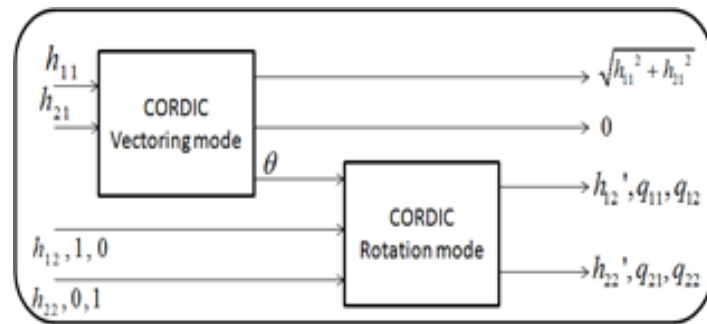


Figure 2. Proposed QRD module for real 2x2 matrix

5. IMPLEMENTATION AND RESULTS

The proposed QRD module for MIMO detection is implemented using Xilinx System Generator. System Generator is a DSP design tool that makes use of Simulink-The Mathworks based design environment [13] for FPGA design. Xilinx blocksets are IP cores and used to design the modules required. The blocks are polymorphic and the FPGA implementation steps such as synthesis and place and route are automatically performed to generate the programming file. Figure 3 shows the implementation of CORDIC vectoring unit using Xilinx System Generator.

The vectoring unit implements the equations 2, 3 and 4 and the angle increment in (4) are stored using Block RAM in Xilinx Block set. For each iteration, the angle increment is retrieved from the Block RAM by giving the address. The vectoring unit takes one clock cycle(cc) to generate the output. Therefore, the latency for the unit is 1cc. Figure 4 shows the CORDIC rotation unit. This unit implements the equations 5, 6 and 7 and has a latency of 1cc. Figure 5 depicts the pipelined and scaled rotation CORDIC unit for 13 iterations and Figure 6 shows the scale correction unit for K=0.6057 using simple shift and addition operation.

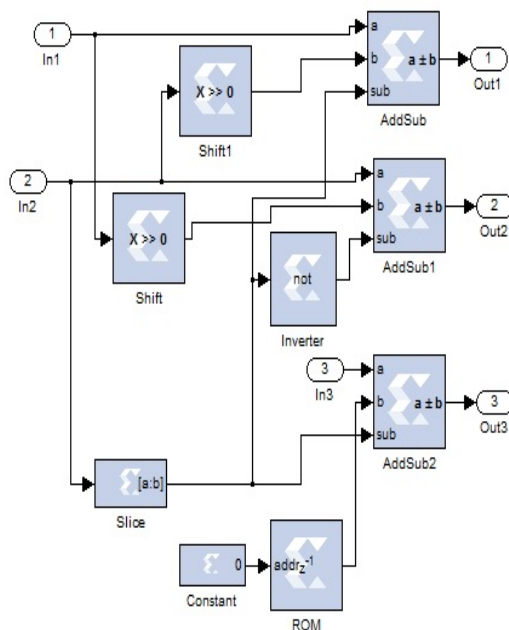


Figure 3. Implementation of Vectoring mode

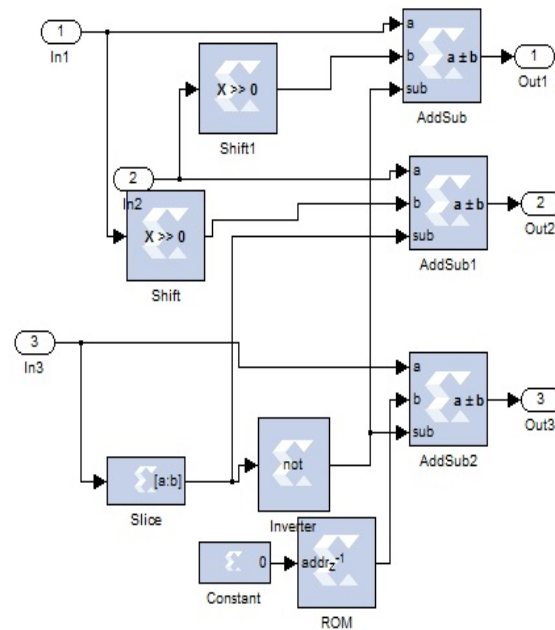


Figure 4. Implementation of Rotation mode

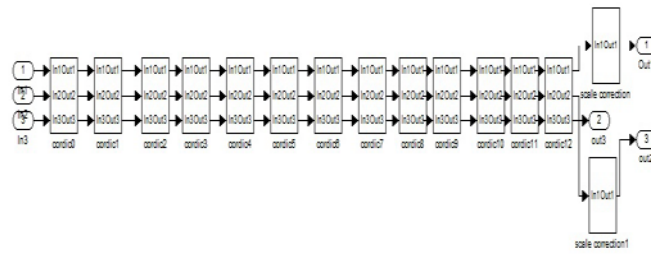


Figure 5. Implementation of Pipelined and scaled rotation CORDIC

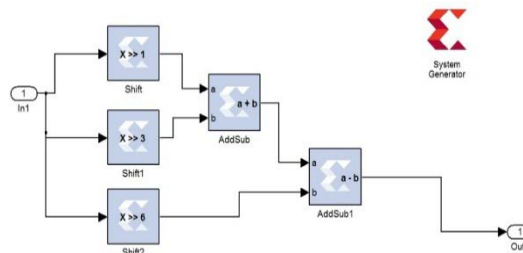


Figure 6. Scale Correction unit

Figure 7 shows the timing diagram of the QRD module. The vectoring CORDIC gives the real value output and the rotation angle in 13 clock cycles thereafter the rotation CORDIC makes use of the angle and performs rotation of the given input in next 13 clock cycles. Therefore, the overall latency of the QRD module is 26 clock cycles for performing the QRD of 2x2 real channel matrix. The computational complexity of proposed QRD module is tabulated in Table 1. The proposed QR Decomposition of 2x2 real channel matrix requires 84 additions and for a 2x2 complex channel matrix requires 295 additions. The number of addition operations performed in each CORDIC unit is 3 and hence, for 13-pipelined vectoring CORDIC unit it is 39 and 2 addition operations for Scale Correction Unit together there are 41 addition operations. In pipelined rotation unit 39 additions for 13 stages and 4 additions for 2 scale correction unit together there are 43 additions. Hence, the proposed design for a 2x2 complex matrix requires 16% reduced number of additions compared to Givens rotation method by Hwang in [14]. The 2x2 complex channel matrix is implemented using two proposed QRD modules out of which two modules will operate in a parallel manner. Therefore, the latency taken by 2x2 complex matrix will be 52 clock cycles.

As the proposed design is scalable, the QRD module design can be utilized to decompose a 4x4 channel matrix. Four QRD modules are required for 4x4 real channel matrix and it takes 104 clock cycles to obtain an upper triangular matrix which is 42% lesser compared with literature [15]. The decomposition requires 336 addition operations which is 9% lesser compared to work done in [14].

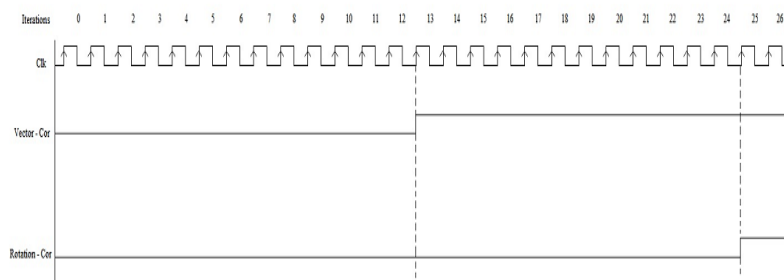


Figure 7. Timing Diagram

Table 1. Computational Complexity Comparison

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Scheme	Matrix Dimension	Addition operations
Proposed real QRD	2x2	84(43+41)
Proposed complex QRD	2x2	168
Complex Givens Rotation [14]	2x2	200
Real QRD (4x4)	4x4	336
Real Givens Rotation[14]	4x4	368

Table 2 depicts the Synthesis report of QRD module for 2x2 real channel matrix and 2x2 complex channel matrix. The design was targeted to Xilinx Virtex 5 FPGA. The minimum time period taken for the design is 2ns i.e. 1cc. Therefore, for 2x2 real matrix and 2x2 complex matrix the latency taken by the module is 52ns and 104ns respectively. The number of LUTs used, the number of occupied slices, the number of Block RAMs used and the on-chip power consumed by the design at 100MHz FPGA clock frequency are listed in the table. The Xpower analysis report gives the on-chip power consumption of the module.

Table 2. Synthesis Report for 2X2 Matrix

Device	Xilinx Virtex 5 xc5vsx240t-2ff1738	
	Resources	
No. of LUTs used	2112	8812
No. of occupied slices	586	2376
No. of Block RAMs used	18	53
On-chip power(mW) at 100MHz	12	44

REFERENCES

- [1] A.J.Paulraj,D.A.Gore,R.U.Nabar, and H.Bolskei, "An overview of MIMO communications-A key to gigabit wireless," Proceedings of IEEE, vol.92,no.2,pp.198-218,Feb.2004.
- [2] Hua Li, Jing Bai, Shujian Liao, Juanping Wu, "Simulation models for MIMO Wireless Channels," TELKOMNIKA Indonesian Journal of Electrical Engineering, Vol.11, No.1, pp. 158-166, 2013.
- [3] R.Andraka, "A survey of cordic algorithms for FPGA based computers," Proceedings of Sixth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays,Monterey,CA,USA,February 1998.
- [4] Kuang-Hao Lin,Chang R.C,Chein-Lin Huang, Feng-Chi Chen, "Implementation of QR decomposition for MIMO-OFDM detection systems" Proceedings of 15th IEEE International Conference on Electronics,Circuits and Systems,pp.57-60,2008.
- [5] Hwang.Y.T, Chen.W.D, "Design and implementation of a high-throughput fully parallel complex-valued QR factorization chips" , IET Circuits, Devices & Systems,5,pp.424-432,2011.
- [6] Awais Ahmed, Syed Haider Abbas, Muhammad Faheem Siddique, Hussnain Haider, "Evaluation of High Speed Hardware Multipliers Fixed point and Floating Point", International Journal of Electrical and Computer Engineering, Vol.3, No.6, pp.805-813,2013.
- [7] G.L.Nazar,C.Gimmler,N.Wehn, "Implementation comparison of the QR decomposition for MIMO detection", Proceedings of the 23rd symposium on Integrated circuits and system design,pp.210-214,2010.
- [8] Pramod K.Meher,Javier Valls, Tso-Bing Juang et.al, "50 Years of CORDIC:Algorithms,Architectures and Applications," IEEE Transactions on Circuits and Systems-I:Regular Papers,Vol.56,No.9,pp.1893-1907,2009.
- [9] A.Shirly Edward, S.Malarvizhi, "Reconfigurable Supercell design for Pseudo Inverse Module using Xilinx System Generator" Proceedings of International Conference on Advances in Communication,Network and Computing, Elsevier Science and Technology, pp.215-220, 2013.
- [10] Zahid Khan, Tughrul Arslan et.al, "Area and Power Efficient VLSI architecture for computing pseudo inverse of channel matrix in a MIMO Wireless System",19th IEEE International Conference on VLSI Design,2006.
- [11] C.M.Rader, "VLSI systolic arrays for adaptive nulling" , IEEE Signal Processing Magazine, Vol.13,4,pp.29-49,1996.
- [12] Huang,Z-Y. and Tsai, P.-Y., "Efficient implementation of QR decomposition for Gigabit MIMO-OFDM systems" , IEEE Transaction on Circuits and Systems,Vol.58,pp.2531-2542,Oct.2011.
- [13] Vaibhav S Hendre, M Murugan, Sneha Kamthe, " Performance Analysis of Transmit Antenna Selection with MRC in MIMO for Image Transmission in Multipath Fading Channels Using Simulink," International Journal of Electrical and Computer Engineering(IJECE), Vol.5, No.1, pp.119-128, 2015.
- [14] Yin-Tsung Hwang,Wei-Da Chen, "A low complexity complex QR factorization design for signal detection in MIMO OFDM systems" ,IEEE International conference,pp.932-935,2008.
- [15] Aslan,S., Niu,S., and Saniie,J., "FPGA Implementation of Fast QR Decomposition Based on Givens Rotation," Proceedings of 55th IEEE International Midwest Circuits Systems, pp.470-473, 2012

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Dr. Shirly Edward.A is from Chennai and received her B.E. in Electronics and Communication Engineering from Madras University and M.Tech. in VLSI Design from SRM University in the year 2001 and 2007 respectively. She received her Ph.D degree from SRM University in 2017. Her main research interests are implementation of the detection algorithms for MIMO Systems and VLSI Digital Signal Processing. She is a member of IET and Life member of ISTE



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