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Performance Enhancement in Active Power Filter (APF) by FPGA Implementation

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ABSTRACT

The generated electrical power in present days is not able to meet its end-user requirement as power demand is gradually increasing and expected to be increasing more in future days. In the power quality management, the parameters/factors like harmonic currents (HC) and reactive power (RP) yields the major issues in the power distribution units causing transformer heating, line losses, and machine vibration. To overcome these issues, several control mechanisms have been presented and implemented in recent past. The control algorithm based on synchronous reference frame (SRF) offers a better response by dividing the HC and RP. But the SRF based control algorithm requires better synchronization among the utility voltage and input current. To achieve this, the existing researches have used digital signal processing (DSP) and microcontroller, but these systems fail to provide better performance as they face issues like limited sampling time, less accuracy, and high computational complexity. Thus, to enhance the performance of active power filter (APF), we present an FPGA based approach. Also, to validate the performance of the proposed approach, we have used Xilinx 14.7 and Modelsim (6.3f) simulator and compared with other previous work. From the results analysis, it is found that the approach has good performance.

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1. INTRODUCTION

The role of power electronics in power system has been widespread in almost all the sectors like industries, commercials, etc. But, when the end users load of the power system is non-linear these power electronics devices generates harmonic currents (HC) and reactive power (RP) and which impacts on the power quality [1]. Hence, to resolve the HC and RP issues and achieve the significant power quality passive filters (PF) were designed. But, PFs lags with the some of the issues concerning size, fixed compensation and resonance problems. These limitations of the PF has lent towards the design of active filters (AF) [2], [3]. The AF has got more significant features over the PF to tackle the power quality issue. The power quality indicates the interaction between source power and hardware component.

The undamaged operation of the power system at normal operating condition is known as good power quality.

In case the hardware is malfunctioned /damaged in power system at normal operation then it is a power of poor quality.

To improve power quality and harmonic elimination, various researches were presented. Latha et al. [4] discussed the control strategy for 3-phase shunt APF with low current measurements. This strategy was

compared with the outcomes of dynamic and study state responses and found the effectiveness of source current than load current measurements. The combinational work of Balasubramanian and Palani [5] expressed the simulation-based analysis for shunt hybrid APF by siusng PQ theory. This improves the performance (i.e., power quality) in the passive filter within hybrid APF. The work of Hasan et al. [6] proposed the linear quadratic regulator (LQR) controller-particle swarm Optimization (PSO) based harmonic suppression mechanism for shunt hybrid APF. This outcome with smother current and voltage signals with less processing time.

The power quality represents the wellness of electrical power towards end-user devices. The main reason for the power quality issues is harmonic waveforms. The power harmonics exhibit different undesirable consequences in the distribution system [7]. The harmonic waveforms cause various issues like voltage distortion, higher voltage stresses, resistive losses, lower motor proficiency, etc., in the power system. Various harmonics generating devices have made power management requirements. A harmonic is generated due to the abnormal behavior of load and also demands the control over these harmonics. The significant way to maintain these aspects is by using the combination of APF for harmonic suppression and harmonic compensation. The APF is a more prominent solution because it reduces both RP and HC and is smaller in size and doesn't need any prerequisites as in PF [7]. The SRF based approaches were used to divide HC and RP, by which good power quality, can be achieved. But, it needs proper synchronization between the utility voltage and input current. Hence, DSP and other software-based mechanisms were used that causes computational complexity, low/limited sampling rate and less accuracy. As these mechanisms consume higher CPU time that causes computational latency [8], [9]. Thus, recently AFs proposed by implementing the multi-dimensional DSP. The control algorithms were used with single-DSP in low pass filter (LPF) for low sampling rate and time delay compensation. These implemented methods can bring more hardware complication and software design patterns and also in many of the cases causes the accuracy and performance issue.

In this paper, a FPGA based mechanisms for APF performance enhancement is presented. The paper is composed of various sections like Section 2 gives APF system configuration. Section 3 gives the problem description. Section 4 gives the research methodology of FPGA implantation in APF. Section 5 algorithms implementation and the Section 6 gives results analysis, and conclusion of the paper is explained with the significance of the proposed method in section 7.

2. OPERATING PRINCIPLE OF APF

The current power system based industries use some semiconductor based devices in furnaces, un-interrupted power supplies (UPS), computer-power supplies, etc. These devices were widely used because of there low cost, flexibility, energy efficiency and also bring the improvement in the power quality by reducing HC and utilizing RP. But, these processes can cause resonance issue, generation of more neutral current, low power-factor, etc. Thus, PF was presented to solve these HC and RP issues caused due to non-linear load. But, PFs got larger size and resonance issues. Later, the APFs were presented to solve the limitations of the PF and bring the improvement in the power quality. The main significance of AF over the PF is that it has smaller size and more flexible functional applications [10].

2.1. APF Configuration

The Figure 1, indicated with the SRF mechanism [11-13] based system configuration of APF and the blocks of it are explained below.

a. Distortion detection: The block contains RP and HC as current identifiers, and the clock detects the distorted parameters of load current, i.e., $i_r abc$ and derive the Voltage Source Inverter (VSI) reference current i_r.
b. Phase Locked Loop (PLL): The PLL mechanism based block that can able to detect the synchronized phase information's of ($v_a, v_b \; and \; v_c$) instantaneously.
c. Inverter-current (I-C) control: This block uses a PWM that ensures that the output VSI current i_c which tracks accurate reference waveform.
d. VSI module: This block act as power converter and injects the waveforms of load current. In this, dc capacitor is used as supply for converter as voltage source.

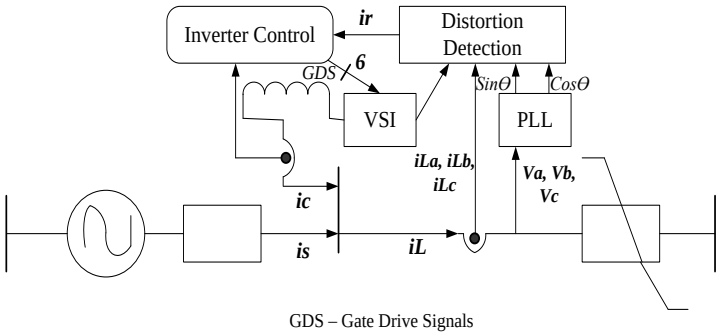

Figure.1. APF Configuration

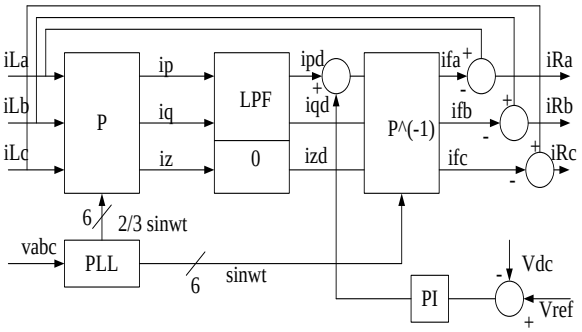

Figure 2. Current-Reference (C-R) Generator

In the Figure 2, current reference (C-R) generator is discussed which is having 3ϕ load current and is transformed as dqz vector forms.
From parks transformation principles,

$$i_{pqz}=[i_p \quad i_q \quad i_z]^T$$
$$\rightarrow i_{pqz} = P\times[i_{La} \quad i_{Lb} \quad i_{Lc}]^T \tag{1}$$

Later, the abc frame components can become dc current terms i.e., i_{pd}, i_{zd} *and* i_{qd} of dqz the frame. Also, harmonics are transformed into the ac components using frequency shift. The negative component i_{qd} is set as zero to compensate the RP currents. The instantaneous active power (AP) currents can be obtained by using inverse Parks transformation, where i_{fa} , i_{fb} *and* i_{fc} are the AP currents and are obtained from dc terms,

$$i_{fabc}=[i_{fa} \quad i_{fb} \quad i_{fc}]^T = P^{-1}\times[i_{pd} \quad i_{qd} \quad i_{zd}]^T \tag{2}$$

Subtracting i_{fabc} from i_{Labc} and distorted components are obtained. The obtained, current is considered as instantaneous reference currents, i.e i_{Ra} ., i_{Rb} and i_{Rc} of the VSI module.
Considering Equation (1) and Equation (2):

$$P = \frac{2}{3}\times\begin{bmatrix} \cos wt & \cos(wt-\frac{2}{3}\pi) & \cos(wt+\frac{2}{3}\pi) \\ -\sin wt & -\sin(wt-\frac{2}{3}\pi) & -\sin(wt+\frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3}$$

$$P^{-1} = \begin{bmatrix} \cos wt & -\sin wt & 1 \\ \cos(wt - \frac{2}{3}\pi) & -\sin(wt - \frac{2}{3}\pi) & 1 \\ \cos(wt + \frac{2}{3}\pi) & -\sin(wt - \frac{2}{3}\pi) & 1 \end{bmatrix} \quad (4)$$

In case the value of i_c becomes similar to i_r reaches then compensation of RP and HC is done through APF, which leads to sinusoidal source current in phase with voltages. The system in the figure.3, with load parameters in APF, will lead to unity power factor and low total harmonic distortion (THD). The dc voltage regulator can be taken into consideration and output current i_{dc} can be generated, which depends on the difference between the reference voltage v_{ref} and dc-bus voltage v_{bc}. In case of fluctuation in dc voltage occurs, then regulator starts controlling RP transfer and receives between dc capacitor and ac grid to attain constant dc voltage. The zero sequence i_z components compensate the zero sequence current in 3ϕ, 4-wire systems, and are zero in this application [14].

3. PROBLEM IDENTIFICATION

In the power distribution system, the RP and the HC may offer some of the serious issues causing transformer heating, line losses, malfunctioning of power equipment and machine vibration. Various control mechanisms were examined from which Synchronous Reference Frame (SRF) for control algorithm makes significant results with simple implementation and efficient response. This algorithm offers the capability of decomposition or separation of the RP and HC. Also, these algorithms demand utility voltage phase information by which necessity of synchronizer for better synchronization of S-C with the utility voltages. Various algorithms such as protection module, dc voltage regulator, analog to digital (A-D) converter drivers and directed-current (d-c) controller, etc., need to be used for synchronization. The above process leads digital controller realization in a system having high sampling rate. The DSP based and other software-based mechanisms provide allowable flexibility and computational ability. The implementation of these systems with control algorithm consumes higher CPU time causing computation latency. Also, APF with multi-DSP or single-DSP were used but which leads low sampling rate and time delay compensation among the low power filter (LPF).

The above method causes the complication during designing software and hardware that may inject the reduction of compensation accuracy and APF performance. Thus, the implementation of FPGA based control algorithms will execute all the above-stated procedures/steps simultaneously with hardware implementation.

4. RESEARCH METHODOLOGY

In this, a system is presented based on FPGA (Figure 3). However, the more difficult issue is how to reduce the number of functional units (such as adders, dividers, and multipliers that are the big issues for the finite hardware resource of FPGA). In this, the basic signal-processing blocks of an APF: three-phase PLL, and current directed controller are discussed.

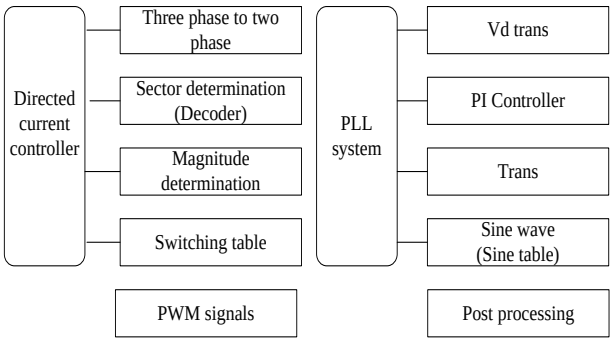

Figure 3. The proposed system architecture

4.1.3. Phase PLL System

APFs are installed at the point with a significant degree of voltage distortion caused by nonlinear loads and APFs themselves. Therefore, the quality of voltage phase information obtained from the identifier is very crucial under this condition. Usually, a PLL system is employed to obtain the phase information synchronized with the utility voltages in real-time. Zero-crossing point-1 detection method is one of the widely used PLL systems, but it has relatively poor behavior under harmonics, frequency-variation, unbalance, or noise conditions. In this paper, three-phase PLL is shown, which provides excellent tracking capability under these conditions.

During ideal operation, the input data Vabc can be represented with 1 p.u. Amplitude as:

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \sin\theta' \\ \sin(\theta' - 2/3\,\pi) \\ \sin(\theta' + 2/3\,\pi) \end{bmatrix} \quad (5)$$

Apply Park's transformation (3) to (5), the 3ϕ voltages in dqz frame as:

$$V_{abc} = \begin{bmatrix} V_d & V_q & V_z \end{bmatrix}^T = P \times V_{abc} \quad (6)$$

Consider reference component (Vdr) = 0, then Vd can be obtained from (6) under PLL-locked (steady state) condition.

$$V_d = \lim_{\theta' - \theta} \sin(\theta' - \theta) = \theta' - \theta = \Delta \quad (7)$$

From above $\sin(\theta' - \theta)$ is equal to $\theta' - \theta$ when θ' approaches θ. i.e., $V_d = \Delta$ and will approach zero under phase-locked condition. The loop error (Δ) gives angular frequency (ω) via a proportional-integral (PI) controller. Finally, an integrator is used to produce the phase output. From (7), we can know that Δ is derived from Vd only. The computation of Vq and Vz should be neglected to reduce computing-resource consumption. Thus, the equation of the phase-error detection can be simplified as

$$\Delta = V_d = V_a \times \cos(\theta) + V_b \times \cos(\theta - \frac{2}{3}\pi) + V_c \times \cos(\theta + \frac{2}{3}\pi) \quad (8)$$

Using above model (Figure 4), a compact 3ϕ PLL system is realized and is shown in Figure 5. From above, equation VII, $V_d = \Delta$ and which includes loop error calculation. Thus, the result forwarded to PI controller uses "+" sign in the feedback loop, as shown in Figure 4. Later, the Δ need to multiplied by two constants (Kp, Ki). However, if Ki is adjusted to be a power of two, the multiplication can be substituted by a shifting operation, which is much simpler and area-efficient in FPGA applications. Also, the proportional calculation is produced by an Np bits shifter. It is noted that a Ni bits shifter is added in the integral procedure to truncate the output to the same width of the proportional action result.

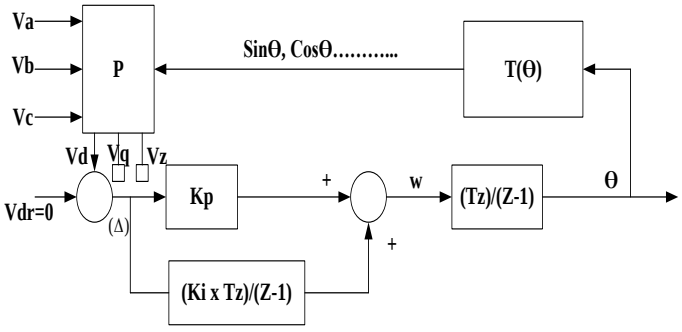

Figure 4. 3ϕPLL in discrete time domain

The sinusoidal function T(θ) is implemented by look-up table method using the internal RAM of FPGA. Considering saving the RAM resource, only a one-quarter size sinusoidal table (0 ~ π/2) is required because of the symmetric relation of the sinusoidal function. The entire process is shown in Algorithm 1:

Algorithm 1: for PLL:

Input: va, vb, vc
Output: sine/cosine signals
Start:
Step-1: Define 3ϕ va, vb, vc
Step-2: set Vdr=0
Step-3: Get $V_d = \Delta$, (Δ) --is loop error
Step-4: Generate phase output by integrator
Step-5: multiply constants Kp and Ki
Step-6: Get the output from shifters Np and Ni add to adder
Step-7: Use sinusoidal table (0 ~ π/2) for sinusoidal function
Step-8: Perform post-processing
Step -9: Obtain sine/cosine signals
End

As a result, an address generator must be inserted to generate the six different lookup addresses from a single-input θ. Also, a postprocessor has to be designed to produce the correct outputs from the compact table. The address generator and postprocessor are both controlled by a finite-state machine as shown in Figure 6.

4.2. Directed Current Controller

The compensated APF currents are complex and vary continuously. Thus, the inverter-current controller needs to respond more quickly to high tracking accuracy. When the instantaneous magnitude of the error-current (ΔIM) is beyond the outer hysteresis tolerance Mo, the outer control loop is activated. In this mode, the magnitude of ΔI is so large that the PWM pattern should force ΔI to change back to the origin in the opposite direction as rapidly as possible. If the ΔI locates in the region I, then V1 should be selected because of its strongest capability to reduce ΔI effectively. When ΔIM is beyond the inner hysteresis tolerance Mi, and within the outer tolerance, the inner control loop will be activated. In this mode, the reference voltage vector (Vref) is essentially an intermediate variable, which can be predicted as the following expression where L is the ac inductor, and T is the sampling period.

$$V_{ref} = V^n + \frac{L}{T}\Delta I \tag{9}$$

A detailed prediction criterion of the reference voltage vector is discussed, and there is also the criterion of the optimal switching output V^n, which is determined by the previous PWM output vector V^{n-1} and the region of ΔI. Furthermore, when V^{n-1} = V6, then the optimal voltage space vector should be V2. The V2 can force ΔI to the opposite direction, and the voltage stress (Vref − V2) applied to the ac inductor is the lowest one of the seven possible values. The lower the voltage stress applied to the ac inductor, the longer time the error-current vector remains in the hysteresis. Therefore, a lower switching frequency can be achieved using this strategy.

The algorithm for hardware implementation gives the detailed block of hardware implementation. In the first step, we consider 3φ reference input, i.e., Ri. In step 2 the Ri is converted to 2φ by using the shifter (Sh) and adders (ad) shown in Figure 7. Later magnitude module (Magm) and sector identification (Si) is generated using 2φ and decoder respectively. Then the generated outputs are applied to generate pulse width modulation (PWM) outputs by using the switching generators (Sg) and switching table (St).

Figure 8 is shows the decomposition of Vref.

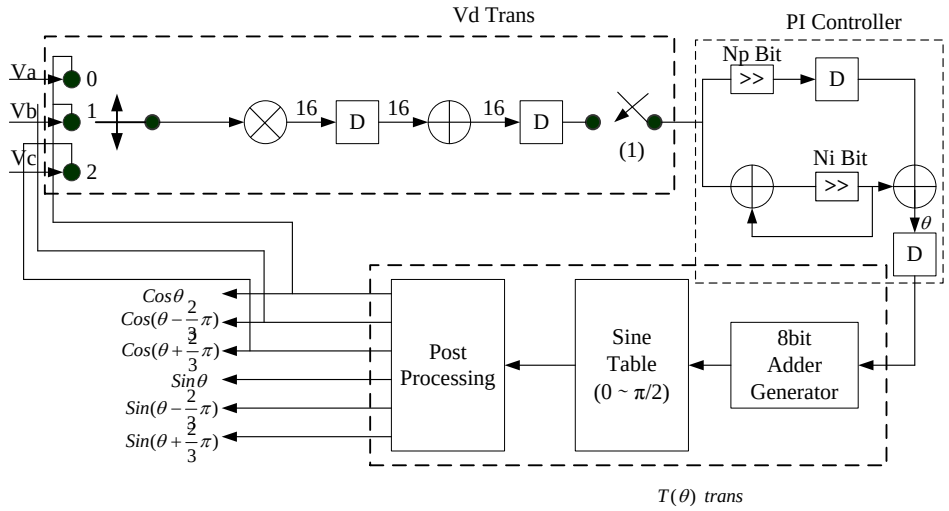

Figure 5. 3φ PLL System

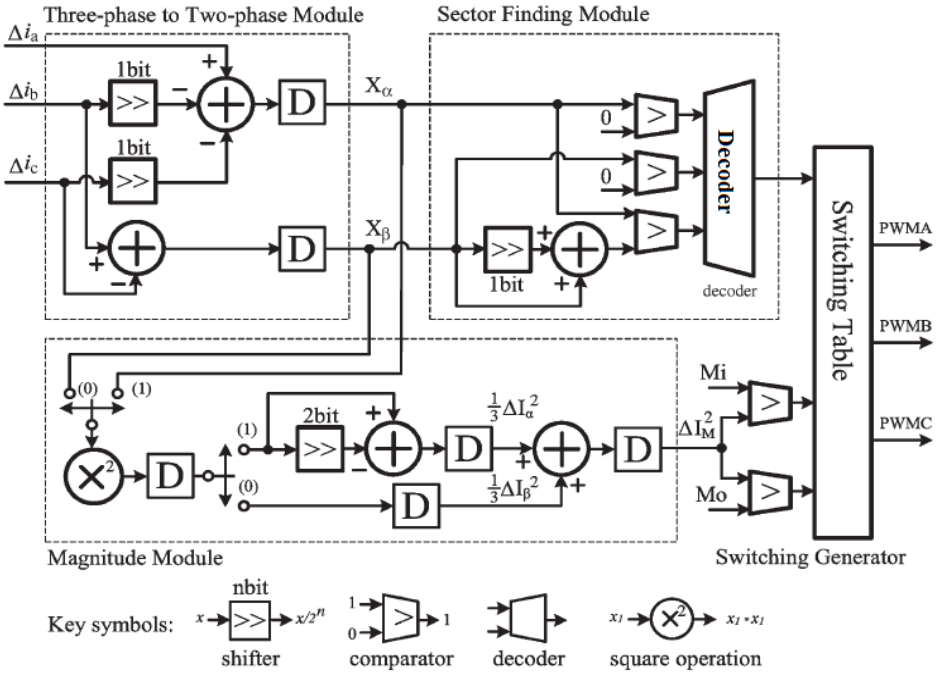

Figure 6. Hardware implementation

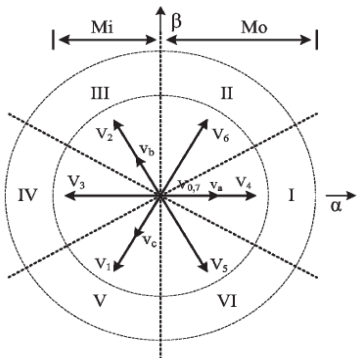

Figure 7. Space vector

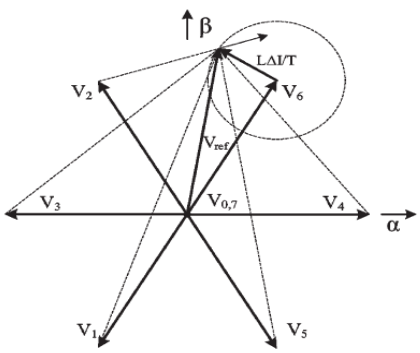

Figure 8. Decomposition of Vref

The hardware implantation is briefly explained by the following algorithm.

Algorithm 2: for hardware implementation:
Input: R_i
Output: PWM
Start:
Step-1: Define 3ϕ R_i
Step-2: Convert "3ϕ R_i" *to* "2ϕ R_i."
Step-3: Generate "Magm" from 2ϕ R_i
Step-4: Generate "Si" by decoder table
Step-5: Combine "Magm+Si"
Step-6: Get PWM
End

Table 1. Improved sector identification

a[0]	a[1]	a[2]	b[2:0]	Sector No	Vector angle
1	X	1	001	I	(-30°, 30°)
1	1	0	010	II	(30°, 90°)
0	1	0	011	III	(90°, 150°)
0	X	1	100	IV	(150°, 210°)
0	1	0	101	V	(210°, 270°)
1	1	0	110	VI	(210°, 330°)
1	1	1	000	-	-

Table 2. Switching output

ΔI sector	$\Delta I_m < M_1$					$\Delta I_m \geq M_0$		
I	4	5	6	7	4	4	4	4
II	6	0	6	2	6	4	6	6
III	2	3	2	2	6	7	2	2
IV	3	3	3	3	0	1	2	3
V	1	1	3	1	5	1	7	1
VI	5	5	0	1	5	5	4	5
V^{n-1}	(0,7)	(1)	(2)	(3)	(4)	(5)	(6)	

5. RESULTS

The outcome of the proposed study is simulated using soft-computational approach using ModelSim 6.3f and Xlinix ise14.7 and Spartan 3 FPGA board.

5.1. 3φPLL Module Results

In the RTL (Figure 9), the inputs to this system are voltages va_in, vb_in, vc_in and system clock clk and system reset rst, and output are cosa, cosb, cosc and sina,sinb and sinc . Simulation results of 3φ PLL system is shown in figure.10. Here we have used active high reset. When the reset switch is low, the 3φ PLL System yields sine and cosine waves with different phases as shown in Figure 10.

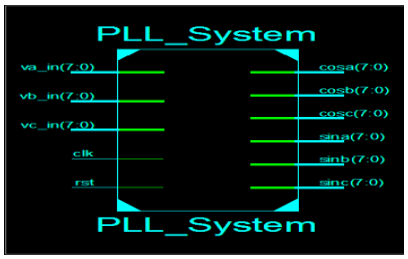

Figure 9. RTL outcome of 3φPLL System

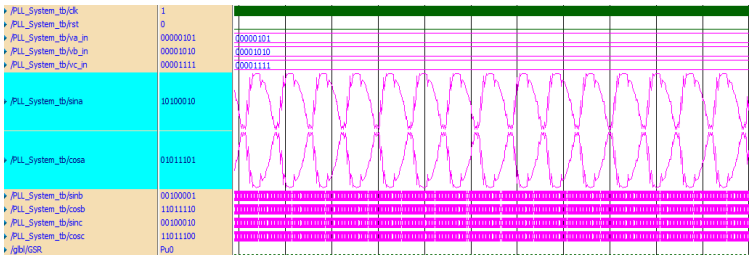

Figure 10. 3φ PLL System simulation

5.2. Direct Current Controller

The RTL schematic of the Direct current controller is represented with Figure 11. The inputs to this system are delia, delib, deltic, mi, mo and system clock clk and system reset rst and the outputs are pwma, pwmb, and pwmc. From the simulation (Figure 12.) results of the direct current controller, we can see that the three pulse width modulation outputs will change according to the changes in the inputs delta_a, delta_b, and delta_c.

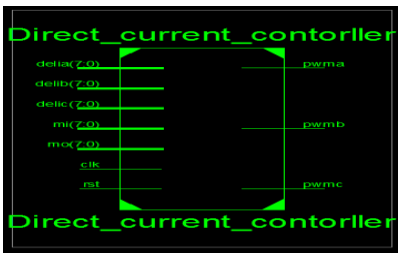

Figure 11. RTL of Direct current controller

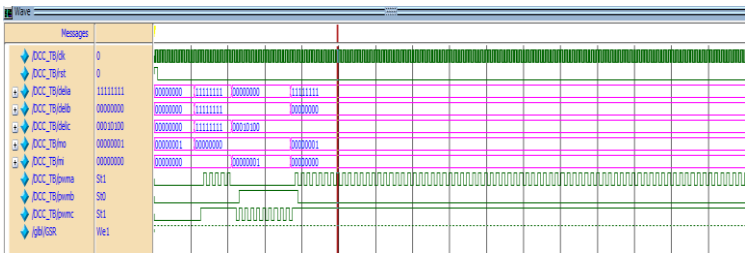

Figure 12. Simulation Results of Direct current controller

Table 3. Design summary of Direct Current Controller

Logic utilization	Utilization
Slices	4%
Slice Flip Flops	1%
4-input LUTs	4%
Bonded IOBs	52%
MultiBx1BSIOs	6%
GoLKs	12%

Table 4. 3φ PLL System design summary

Logic utilization	Utilization
Slices	3%
Slice Flip Flops	1%
4-input LUTs	2%
Bonded IOBs	34%
MultiBx1BSIOs	15%
GoLKs	4%

The resource utilization of the FPGA for designing of 3φs PLL System is shown in Table 3. The resource utilization of the FPGA for designing of Direct Current Controller System is shown in Table 4.

6. CONCLUSION

This paper discusses an APF system based on FPGA to bring the dynamic performance in APF. The system is implemented with 3ϕ phase locked loop (PLL) and directed current controller. The performance of the proposed model is compared with Charles and Vivekananda [15] and analyzed by Xilinx 14.7. And simulated using Model sim 6.3f Simulator The results obtained tabled in Table 5.

Table 5. Performance analysis

Parameters	Charles and Vivekanandan [15] Logic Utilization	Proposed model Logic Utilization
Flipflop slices	9%	2%
LUT	41%	6%
Slices occupied	49%	7%

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