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A 300 GHz CMOS Transmitter Front-End for Ultrahigh-Speed Wireless Communications

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ABSTRACT

This paper presents a 300 GHz transmitter front-end suitable for ultrahigh-speed wireless communications. The transmitter front-end realized in TSMC 40 nm CMOS consists of a common-source (CS) based doubler driven by a two-way D-band power amplifier (PA). Simulation results show that the two-way D-band PA obtains a peak gain of 21.6 dB over a -3 dB bandwidth from 132 GHz to 159 GHz. It exhibits a saturated power of 7.2 dBm and a power added efficiency (PAE) of 2.3%, all at 150 GHz. The CS based doubler results in an output power of 0.5 mW at 300 GHz. The transmitter front-end consumes a DC power of 205.8 mW from a 0.9 V supply voltage while it occupies an area of 2.1 mm^2.

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1. INTRODUCTION

According to the current trend, frequency used for wireless communication will reach terahertz band in 2020. Unallocated frequency region beyond 275 GHz with vast bandwidth can be potentially utilized for ultrahigh-speed wireless communication. In particular, 300 GHz band is attractive since propagation decay in air around 300 GHz is relatively low. However, since studies on terahertz wireless communication including 300 GHz band are still in early stage when only a few transceivers operating above 275 GHz were reported [1] [2] [3]. Since the maximum operating frequency or unity-power-gain frequency, $f_{\max}$, of the n-type MOSFET even with advanced CMOS process is below 300 GHz, realization of 300 GHz RF front-end is challenging. One solution is to use frequency multipliers. A 300 GHz CMOS RF front-end was reported using a tripler [4]. However, the tripler generates not only the desired RF signal but also the higher-order spurious. As a result, the RF signal may be distorted by a higher-order spurious. On the other hand, since quadratic nonlinearity of a MOSFET is stronger than its cubic counterpart, a doubler can generate higher output power than a tripler does.

In this paper, we are going to present the designs and simulations of a 300 GHz transmitter front-end as illustrated in Fig. 1. It includes the CS based doublers (DBLs) driven by the two-way D-band PA. When the doubler is employed, the 300 GHz output signal can be generated from the 150 GHz input one. The paper is organized as follows. Section 2 introduces the architectures of the proposed 300 GHz transmitter front-end including detailed descriptions of circuit topologies. The simulation results are presented in section 3 and conclusions are given in the last section.

2. DESIGN OF 300 GHz TRANSMITTER FRONT-END

2.1. Transmission Lines and Rat-Race Balun

The 300 GHz transmitter front-end is designed using TSMC 40 nm 1P10M CMOS GP process. Its back end consists of 10 copper layers and a top aluminum redistribution layer (RDL). The cross-view of grounded coplanar wave-guide transmission lines (GCPW-TLs) are depicted in Fig. 2 [5]. The GCPW-TL with the characteristic

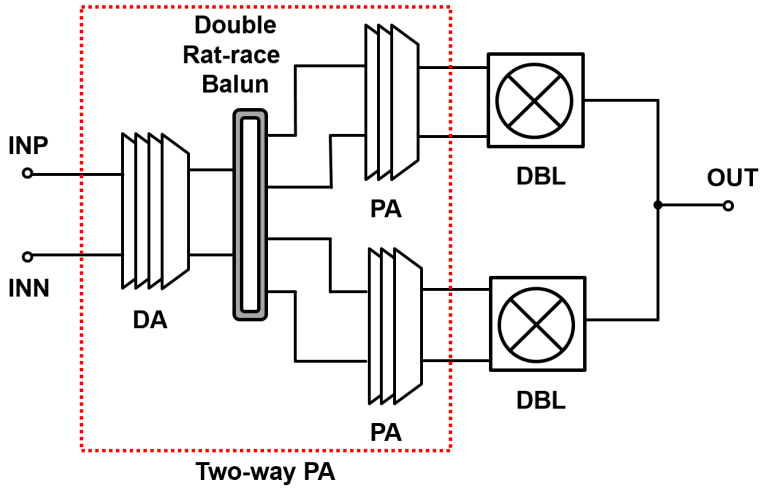
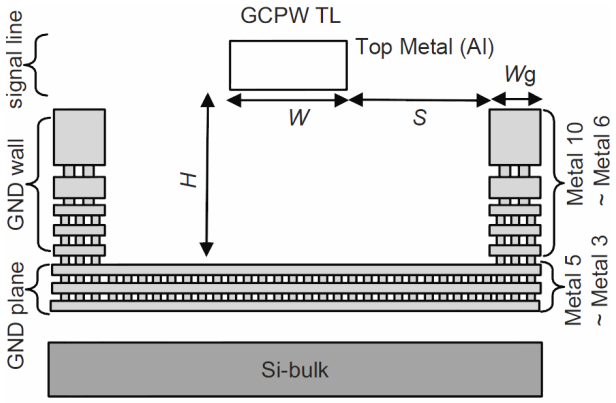


Figure 1. The proposed 300 GHz transmitter front-end.

impedance of 50 Ω (the 50 Ω GCPW-TL) is used for shunt stubs and connecting to the output pad of the 300 GHz doubler. Its signal line consists of the RDL layer with a width of 9 µm. Ground (GND) walls composed of the 6th to 10th metal layers with a width of 2.7 µm are placed on the both side of the signal line at the distance of 7.2 µm. The GCPW-TL with the characteristic impedance of 71 Ω (the 71 Ω GCPW-TL) is used for the shunt stubs of the PA's matching networks, doubler's matching networks and the series stubs of rat-race baluns. The width of the top-layer signal line is 2.9 µm, and the GND wall placed at a distance of 7.6 µm from the signal line has the width of 1.8 µm. The 3nd to 5th metal layers are meshed and stitched together with vias to form the GND plane. Electromagnetic (EM) sim-



	50-Ω TL	71-Ω TL
W [µm] :	9.0	2.9
S [µm] :	7.2	7.6
Wg [µm] :	2.7	1.8
H [µm] :	7.0	7.0

Figure 2. The cross-view of the GCPW-TLs.

ulation by ANSYS HFSS shows that the attenuation constant, α, of the 50 Ω and 71 Ω GCPW-TLs is 1.0–1.4 dB/mm and 1.2–1.6 dB/mm at 100–150 GHz, respectively. The shunt stubs of the inter-stage networks are arranged adjacent across a common GND wall, and the space between the GCPW-TLs is 17 µm. The near-end and far-end crosstalk simulated by EM simulation are below -30 dB and -34 dB at 100 GHz and 250 GHz, respectively. It indicates that the cross-coupling between stubs is negligible.

As illustrated in Fig. 3, the double rat-race balun composed of the 71 Ω GCPW-TLs is designed for generating the differential signal from the single-ended one. The length of the GCPW-TL unit of the double rat-race balun is 300 µm which is equivalent to $\lambda/4$ at 150 GHz (λ is the wave length). The compact design is realized by folding the GCPW-TLs and sharing the GND wall.

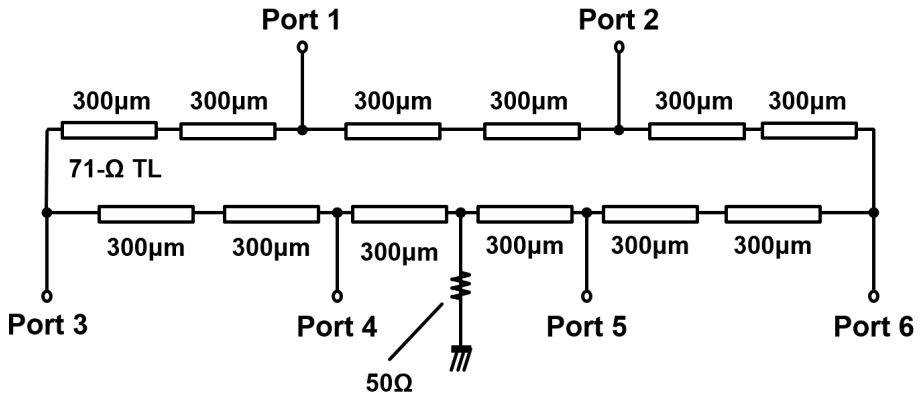


Figure 3. The 150 GHz double rat-race balun.

2.2. Two-Way D-Band Power Amplifier

The circuit schematic of the proposed D-band PA is shown in Fig. 4. It includes an input matching network, an output matching network, three fully differential amplifying stages and inter-stage matching networks. For bandwidth enhancement, multi-stage matchings using capacitors and inductive GCPW-TLs are adopted. The series capacitors and shunt GCPW-TLs form 4th-order high-pass filters at the input ports. The outputs of the PA are directly matched to the inputs of the doubler. The inter-stage matching networks are based on PI networks for wideband performance. All of the capacitors also act as coupling capacitors while the DC bias voltages are applied across the GCPW-TLs. The bias voltages are common to all amplifying stages. The shunt stubs composed of 71 Ω GCPW-TLs are arranged regularly with sharing GND walls. The connection between the MOSFETs, MOM capacitors and GCPW-TLs are made by the 8th to 10th metal layers. The lengths of the GCPW-TLs and the MOM capacitor values are determined by a nonmetric optimization process taking into account the models of MOSFETs, MOM capacitors and GCPW-TLs. The far end of each shunt stub is terminated by a wideband decoupling power line with very low characteristic impedance (the 0 Ω TL).

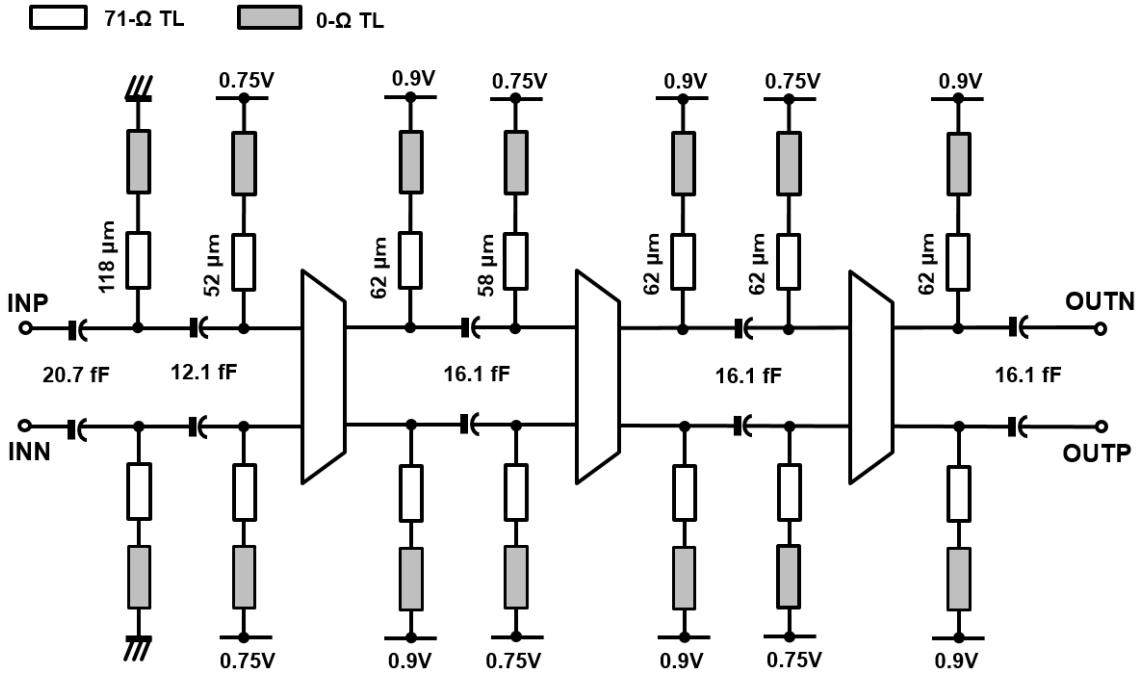


Figure 4. The proposed D-band PA.

The internal negative feedback path caused by the parasitic gate-drain capacitor, C_{GD} limits the power gain and reverse isolation, and potentially causes instability. In order to improve the stability without compromising the

gain of the MOSFET, the internal feedback in the transistor has to be reduced. An elegant technique to accomplish this is to neutralize C_{GD} in a differential pair by using cross coupling capacitors [6]. Fig. 5a shows the core of the amplifier that is a fully differential pair with capacitive neutralization. The cross coupling capacitor, whose value is 16.1 fF, is determined to obtain high gain. Fig. 5b reveals the parasitics associated at each node of the amplifier core. The parasitic components are extracted using bond-based design which is a measurement-based design approach to avoiding the difficulty associated with layout parasitics when ordinary layout parasitic extraction (LPE) tools used for chip design do not extract inductances.

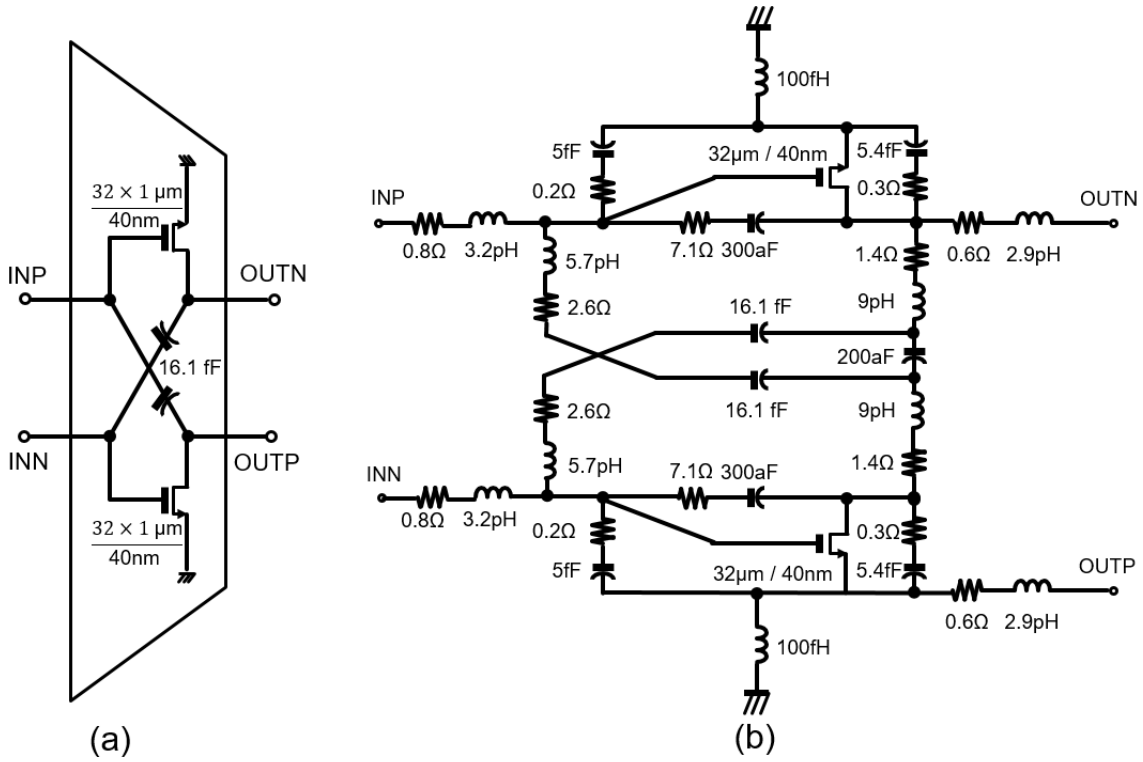


Figure 5. Amplifier core (a) and its equivalent circuit with extracted parasitics (b).

The two-way PA is formed by connecting two D-band PAs in parallel as depicted in Fig. 1. The driver amplifier (DA) at the input is employed as the pre-amplifier before the input power is divided by the double rat-race balun. The DA has a similar topology as the D-band PA does. It consists of four fully differential amplifying stages with cross-coupling capacitors. Many-stage amplifiers for terahertz frequencies tend to occupy a large area since inter-stage matching networks consist typically of several passive devices that are much large than MOSFETs. To realize cost-effective chips, area reduction is important. In order to reduce the area of the amplifier, we proposed the "fishbone layout" [7]. In this technique, GCPW-TL stubs used in matching networks are arranged regularly at narrow spacings, and the GCPW-TLs themselves are designed to be narrow, thereby reducing the footprint.

2.3. 300 GHz CS Based Doubler

As the name suggest, the 300 GHz CS based doubler exploits the quadratic nonlinearity of the MOSFET. It upconverts the signal at the output of the D-band PA into RF signal at 300 GHz frequency band. The main reason using active frequency doubler is that it can achieve conversion gain over broad bandwidth while getting also good DC to RF efficiency. The complete circuit of the proposed doubler with all component values are given in Fig. 6. The same as power amplifiers, the active frequency multipliers work in different classes. In this design, the doubler is biased to operate in an equivalent class-AB power amplifier where it is very stable and have good gain, efficiency and output power. The doubler generates harmonics by rectifying the sinusoidal input signals when is biased near its pinch-off, and the input sinusoids turn the MOSFETs on over part of their cycles. Due to the balanced topology, the even harmonics are generated in phase thus being summed up while the odd harmonics are generated out of phase thus being suppressed. The outputs are tuned to the second harmonic while other harmonics including the fundamental frequency are further suppressed by the output PI matching networks. The second harmonic signals leaked through

the MOSFETs to the input ports are shorted by using $\lambda/2$ short stubs. The inputs of the doubler are conjugate-matched to the optimal loads of the preceding D-band PA.

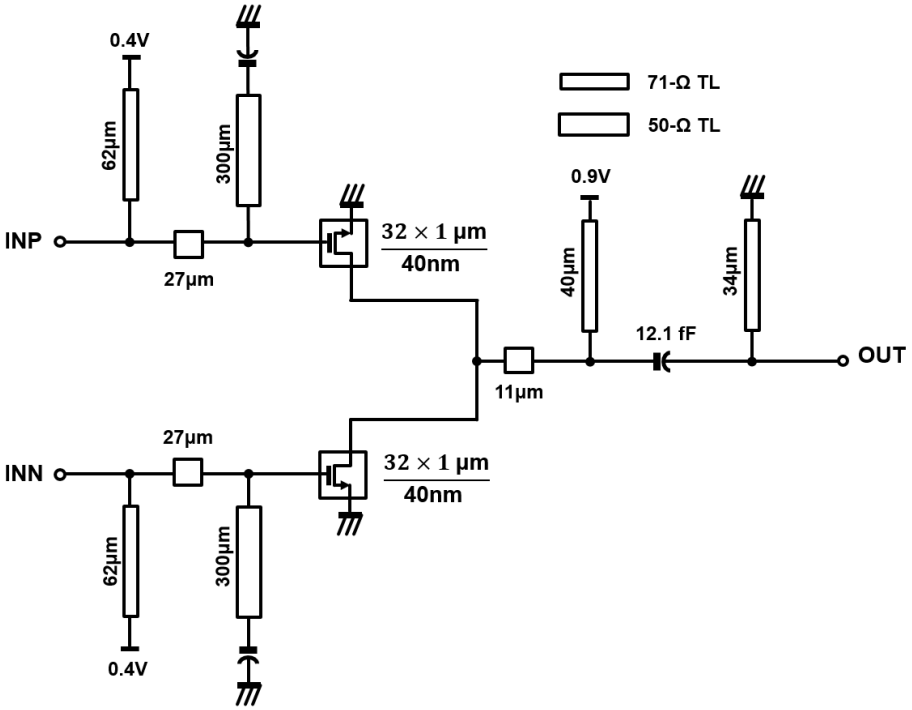


Figure 6. The proposed 300 GHz CS based doubler.

3. SIMULATION RESULTS

Simulation results of the 300 GHz transmitter front-end for TSMC 40 nm CMOS technology are achieved using the Cadence's Virtuoso Analog Design Environment. Circuit design at very high frequencies involves more detailed considerations than at lower frequencies when the effect of parasitic capacitances and inductances can impose serious constrains on achievable performance. Thus, all components used for simulation are RF models provided by TSMC.

3.1. Two-Way D-Band Power Amplifier

Fig. 7 shows the simulated S-parameters of the two-way D-band PA. S_{11} remains below -7 dB while S_{22} is less than -10 dB over the -3 dB bandwidth from 132 GHz to 159 GHz. Both input and output return loss indicate wideband performance. The D-band PA achieves a peak gain of 21.6 dB over the band of interest. The reverse isolation is lower than -140 dB (not shown in the figure). A high reverse isolation guarantees high stability for the PA. Fig. 8 and Fig. 9 plot the output power and PAE versus input power, respectively. At 150 GHz, the designed PA obtains a saturated power of 7.2 dBm and a peak PAE of 2.3% at –6 dBm input power. The output referred 1 dB compression point (OP1dB) is 4 dBm. The two-way PA consumes a power of 199.4 mW from a 0.9 V supply voltage.

3.2. 300 GHz Transmitter Front-End

Fig. 10 shows the simulated S-parameters of the 300 GHz transmitter front-end. As can be seen in this figure, both input and output return loss indicate good matchings. Fig. 11 and Fig. 12 show the output power of the transmitter versus input power and output frequency, respectively. At 150 GHz input frequency, the transmitter exhibits a saturated power of -2.2 dBm. It obtains an output power of -2.8 dBm which is equivalent to 0.5 mW at 300 GHz and covers a -3 dB bandwidth from 274 GHz to 323 GHz. The harmonic power levels are plotted in Fig. 13 where the odd harmonic levels are very low due to the balanced structure of the CS based doubler. Fig. 14 shows the layout of the 300 GHz transmitter front-end. It occupies an area of 2.1 mm^2 including probe pads. The transmitter consumes a power of 205.8 mW from a 0.9 V supply voltage. Table 1 summarizes the performance of the proposed design and compares it to other published transmitters operating in a similar frequency range.

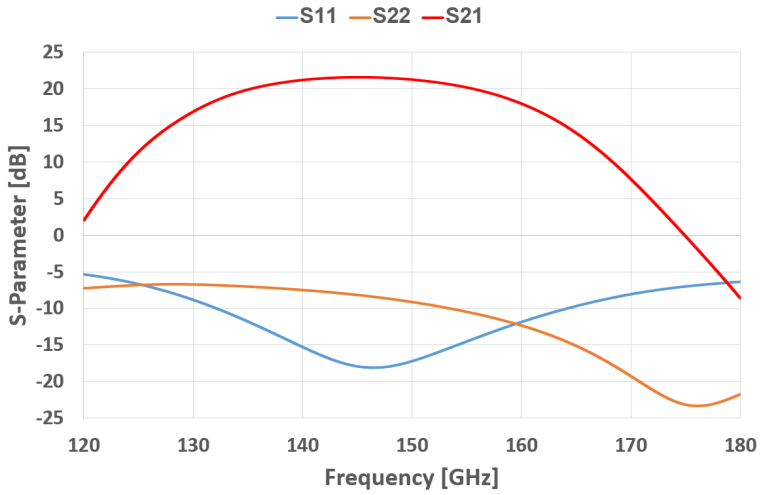


Figure 7. The simulated S-parameter of the two-way D-band PA.

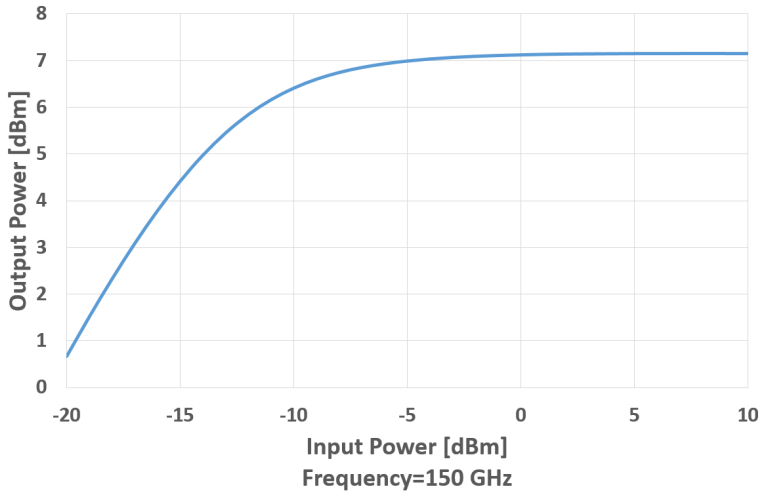


Figure 8. The simulated output power versus input power of the two-way D-band PA.

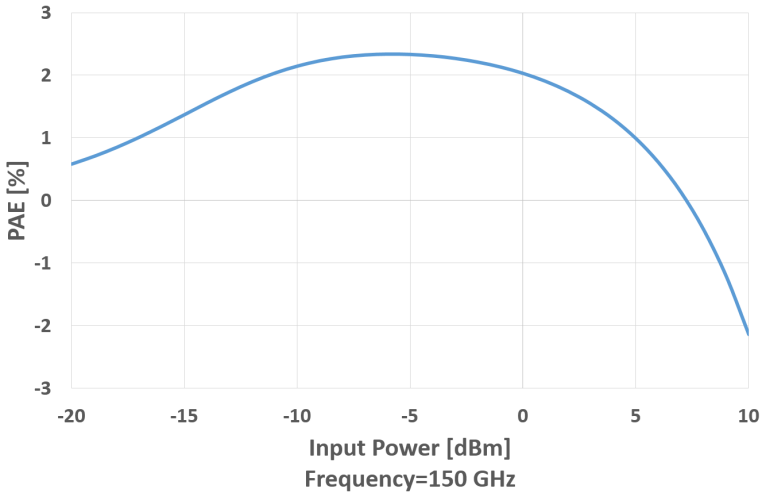


Figure 9. The simulated PAE versus input power of the two-way D-band PA.

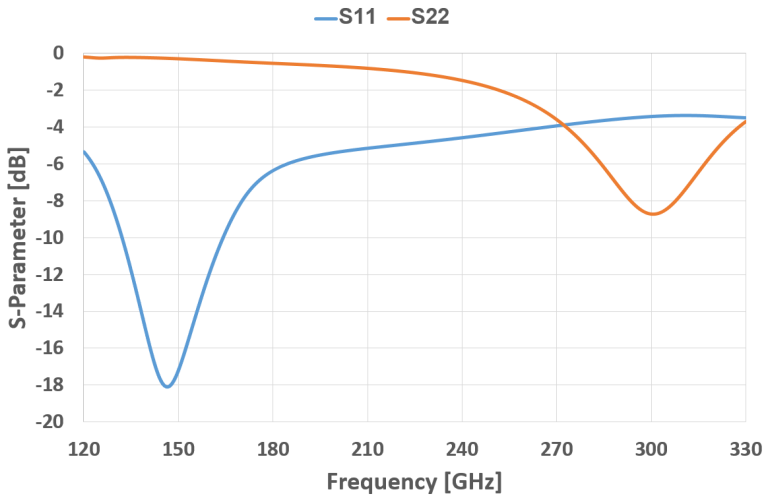


Figure 10. The simulated S-parameter of the 300 GHz transmitter front-end.

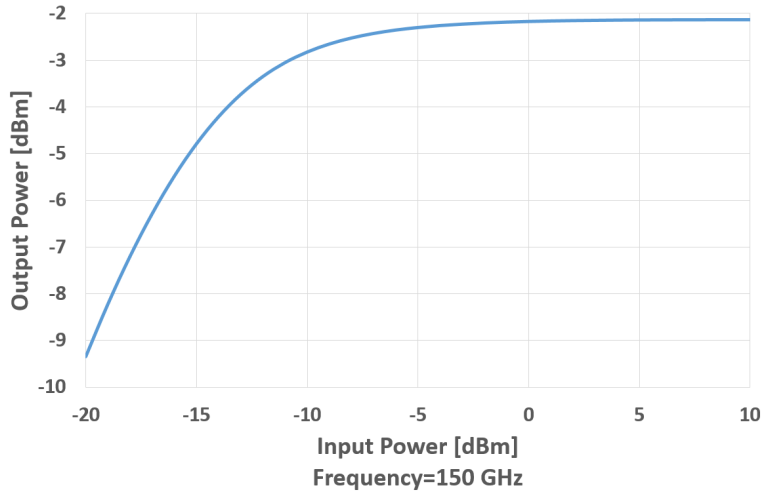


Figure 11. The simulated output power versus input power of the 300 GHz transmitter front-end.

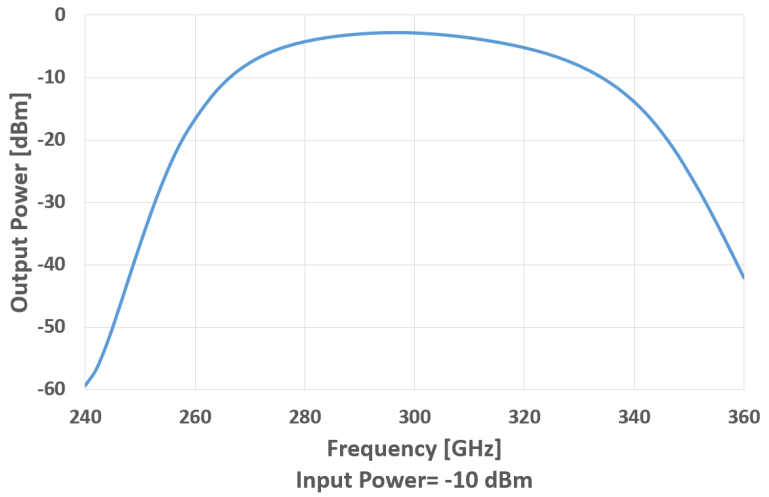


Figure 12. The simulated output power versus output frequency of the 300 GHz transmitter front-end.

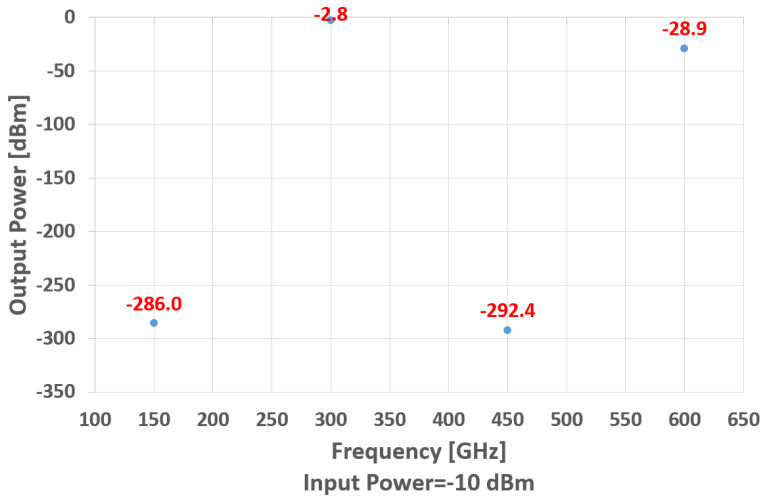


Figure 13. The simulated harmonics of the 300 GHz transmitter front-end.

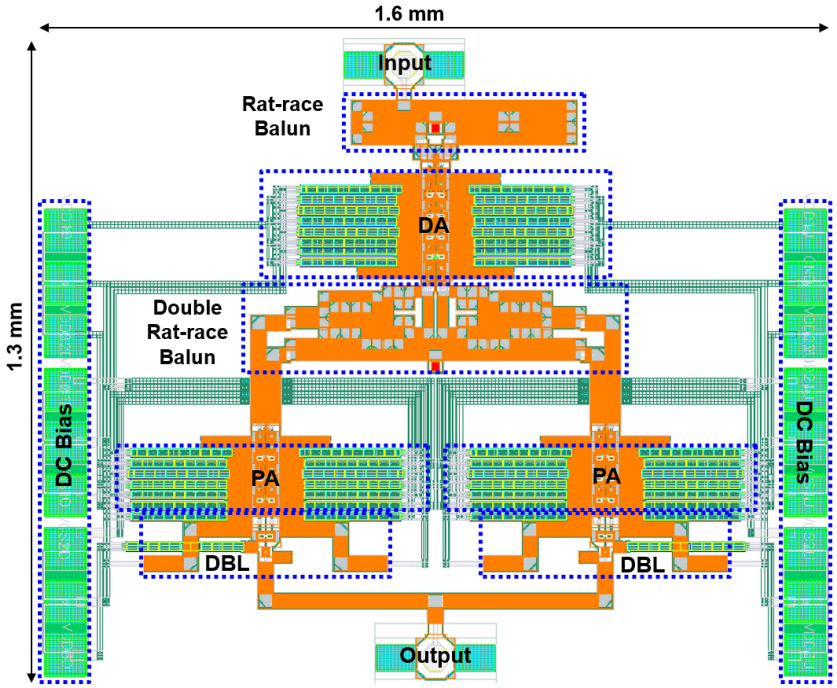


Figure 14. The layout of the 300 GHz transmitter front-end.

Table 1. Comparison with the previous published transmitters

Ref.	Technology	Power cons. (W)	RF frequency (GHz)	Output power (dBm)
[1]	0.25 µm InP	–	300	–
[2]	50 nm InP	–	340	-17.5
[3]	40 nm CMOS	1.4	275–305	-14.5
[4]	65 nm CMOS	0.22	240	0
This work	**40 nm CMOS**	**0.2***	**274–323***	**-2.8***

*Sim. results

4. CONCLUSIONS

In this paper, we have presented the designs and simulations of the 300 GHz transmitter front-end targeted for ultrahigh-speed wireless communications. The two-way D-band PA obtains the peak gain of 21.6 dB, the saturated power of 7.2 dBm and the PAE of 2.3%. The CS based doubler results in the peak output power of 0.5 mW at 300 GHz while covering the -3 dB bandwidth from 274 GHz to 323 GHz. Supplied by the 0.9 V supply voltage, the transmitter front-end consumes the DC power of 205.8 mW while it occupies the area of 2.1 mm^2.

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Tuan Anh Vu received the B.S degree and M.Sc degree in Electronics and Telecommunications Technology from University of Engineering and Technology, Vietnam National University in 2006 and 2009, respectively. In 2013, he received Ph.D degree in the field of analog/mixed-signal RF nanoelectronics from University of Oslo, Norway. Since 2014, he has been a lecturer at Faculty of Electronics and Telecommunications, VNU University of Engineering and Technology. Dr. Tuan Anh Vu was doing postdoc at Department of Semiconductor Electronics and Integration Science, Hiroshima University, Japan. His research interests are analog RF integrated circuit designs including power amplifiers, low noise amplifiers, mixers, frequency multipliers, etc.

Minoru Fujishima received his B.E., M.E. and Ph.D. degrees in Electronics Engineering from the University of Tokyo, Japan, in 1988, 1990 and 1993, respectively. He joined the faculty of the University of Tokyo in 1988 as a research associate and was an associate professor of the School of Frontier Sciences, University of Tokyo. He was a visiting professor at the ESAT-MICAS Laboratory, Katholieke Universiteit Leuven, Belgium, from 1998 to 2000. Since 2009, he has been a professor of the Graduate School of Advanced Sciences of Matter, Hiroshima University. He is currently serving as a technical committee member of several international conferences. His current research interests are in the design of low-power ultrahigh-speed millimeter- and short-millimeter-wave wireless CMOS circuits. He is a member of IEEE and JSAP.