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Impact of multiple channels on the Characteristics of Rectangular GAA MOSFET

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ABSTRACT

Square gate all around MOSFETs are a very promising device structures allowing to continue scaling due to their superior control over the short channel effects. In this work a numerical study of a square structure with single channel is compared to a structure with 4 channels in order to highlight the impact of channels number on the device's DC parameters (drain current and threshold voltage). Our single channel rectangular GAA MOSFET showed reasonable ratio Ion/Ioff of 10^4, while our four channels GAA MOSFET showed a value of 10^3. In addition, a low value of drain induced barrier lowering *(DIBL) of* 60mV/V was obtained for our single channel GAA and a lower value of with 40mv/v has been obtained for our four channel one. Also, an extrinsic transconductance of 88ms/µm have been obtained for our four channels GAA compared to the single channel that is equal to 7ms/µm.

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1. INTRODUCTION

Over the past decades, the Metal oxide Semiconductor (MOSFET) has repeatedly been scaled down in size. However, as the size reduction of planar bulk MOSFET continues, leakage increases, the control of short-channel effects becomes increasingly difficult in planar-bulk architecture [1]. Today different new architectures such as Multiple-gate MOSFETs are considered as a very good alternative replacing bulk MOSFET allowing keeping up with the continuous reduction in device dimensions imposed by Moore's law. The non planar transistors have been found to be more appropriate to the highly scaled transistors lengths. These devices provide better control over the channel thus reducing short channel and hot carriers effects [2]. Indeed, the use of several gates has revealed good electrostatic control of the channel with the opportunity of higher reduction in channel length compared to conventional MOSFETs .New architectures called MUGFETS that are Double-Gate, Triple-Gate, Junctionless FET, PI- Gate, Omega- Gate, Surrounding Gate "square Gate-All- Around MOSFETs and Cylindrical Gate-All- Around) are very promising devices for very short channel lengths [3], [4]. Short channel effects" SCEs" such as threshold voltage roll-off, off-state leakage current, drain Induced Barrier Lowering (DIBL) and subthresholde swing SSs are significantly reduced in multiple gate architectures [5-8]. Among these multiple gate structures, GAA structures offer superior control over the channel due to its surrounding gate structure, which in turn reduces SCEs effectively [8-10]. MUGFETs devices show a very promising possibilities, advantages over single MOSFETs, in relation to the control of SCEs and the achievement of very promising sub-threshold swing

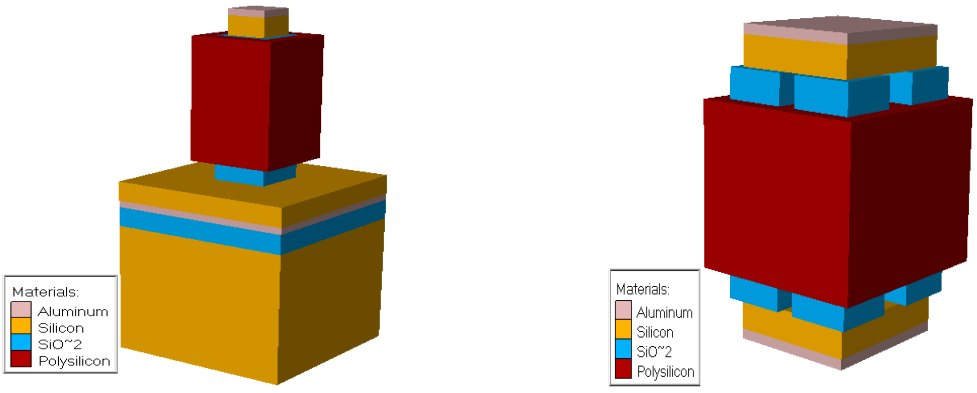
values, a high immunity to SCEs, its low drain induced barrier lowering, high gate controllability, higher current drivability, mobility enhancement and reduction of leakage currents [10].

These devices are considered as excellent candidates for future CMOS integration. Among all MUGFETs devices, GAA structures have gained considerable attention from device and circuit developers. Additionally to the effective suppression of SCEs, MUGFETs devices show exceptional current drive and have the merit that they are perfectly compatible with conventional CMOS processes. The rectangular GAA MOSFETs considered in our study, are a multi-gate structure, their architecture are based on a SOI triple gate structure. The vertical GAA structure has a higher yield [11]. It is considered as a potential candidate for future energy-efficient electronics [12]. In a vertical MOSFET device, the current is orthogonal to the surface of the wafer. In n-channel MOSFET devices, a stack of n+ p n+ silicon is made by epitaxial growth or implantation, then a gate is put around the structure. This architecture has proved to be a realistic approach to sub-100nm channel length devices [14]. Since the introduction of GAA MOSFET, much different architecture has been proposed, using high-k dielectrics [13,15] or ultra-thin silicon channel with possibility to using in channel III-V material ZnO or organic material like Pantacen for different application of MUGFETs devices [16], [17]. A 15nm Channel length in a vertical gate MOSFET has recently been demonstrated [18], [19]. Vertical MOSFETs show better performances than bulk planar devices. They are attractive structures that show better performances than bulk planar devices even if there is no leading design or fully optimized fabrication process for the moment. The GAA MOSFET, which is basically a 3-D structure, cannot be analyzes directly using the conventional way. It can be analyzed by Laplace's equation in rectangular coordinates by means of using a series expansion in Bessel functions [20].

In this work, a simulation of Bohm quantum potential (BQP) model was used to calculate a position dependent potential energy term using an auxiliary equation derived from the Bohn interpretation of quantum mechanics [21]. In this paper we set up a 3D device simulation framework using the SILVACO technology Computer Aided Design (TCAD). In our simulation quantum effects are considered. These have been achieved using the Bohm quantum potential (BQP) model.

2. DEVICE DESCRIPTION

The simulation data presented in this work have been obtained by using SILVACO TCAD tool. The geometry of the two rectangular GAA MOSFETs studied are shown in Figure 1, the cross-section of our four channels GAA MOSFET studied is shown in Figure 2.



(a) (b)

Figure 1. (a) One channel, (b) Four channels Rectangular GAA MOSFETs

As shown in Figure 1 the first device studied is one channel GAA MOSFET, the second one is a four channels GAA MOSFET. All the channels are identical and have the same geometrical parameters. We can see that the gate completely surrounds the square silicon channels where conduction takes place. The devices details of our two GAA are given in Table 1. SILVACO TCAD simulator is used with the adequate models in all our study.

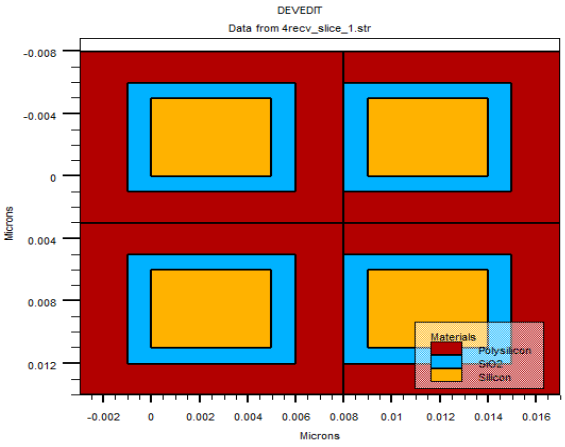


Figure 2. Cross-section of the four channels GAA MOSFET studied

Table 1. Parameters value of our two square GAA devices

Device Parameters	Values
Gate length	19 nm
Channel length	22nm
Channel width	5 nm
Channel heigth	5 nm
gate oxide thickness	2 nm
S/D concentration	1E20/cm^3
Channel concentration	1E17 /cm^3
Buried oxide layer thickness	8nm
substrate layer thickness	50nm

The geometry of our rectangular cross section GAA device confines the electrons in the plane perpendicular to the transport axis. In this case, a 1D electron gas is considered electrons are confined perpendicularly to the transport axis. The quantum charge density can be expressed by [21], [22]:

$$\rho(y,z) = \frac{q}{\pi}\left(\frac{2mk_BT}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \Psi_n^2(y,z)\Im_{-\frac{1}{2}}\left(\frac{E_F - E_n}{k_BT}\right) \quad (1)$$

where q is the electron charge, E_F is the Fermi level, ψ_n is the wave function belonging to energy level En, $\Im_{-\frac{1}{2}}$ *is* the complete Fermi-Dirac integral of order -1/2.

3. RESULTS AND ANALYSIS

All our results were carried out at room temperature. Our Simulation results had been obtained using Atlas Silvaco Software. Typical transfer characteristics I_{ds}-V_{gs} leads to determining different device parameters, like threshold voltage Vth, subthreshold slope SS or off-state leakage current I_{off}. All these extracted parameters allow revealing the performance of the devices in accordance to their scaling. Figure 3 and Figure 4 show the I_{DS} versus V_{GS} *and* I_{DS} versus V_{DS} characteristics at T=300°K.

In order to increase our device current, wider transistors with higher on-currents are obtained using a multiple channel connected together. The current drive is proportional to channels number. Transfer and output characteristic for one, two, three and four channels are shown in Figure 5 and Figure 6.

AS shown in Figure 6, the drain current obtained with four channels device is four times higher than the current obtained by one channel. We can conclude that n-channels connected together allow to obtain a current n- times higher than the current obtained for one channel device. Transconductance g_m is an important parameter for small-signal analysis of analog circuits. Generally, it is important to analyze the transconductance g_m and also transconductance efficiency (g_m/ID) as it provides useful design guidlines. The sensitivity of g_m and (g_m/ID) on process related parameters gives deeper insight of circuit performance. Figure 7 and Figure 8 show the transconductance versus gate voltage for our single channel and our four

channels devices. We can observe that peak tranconductance is occured four our single channel device at V_{GS}= 0.4 volts, whereas for our four channel device, this peak is occured at VGS= 0.85 volts.

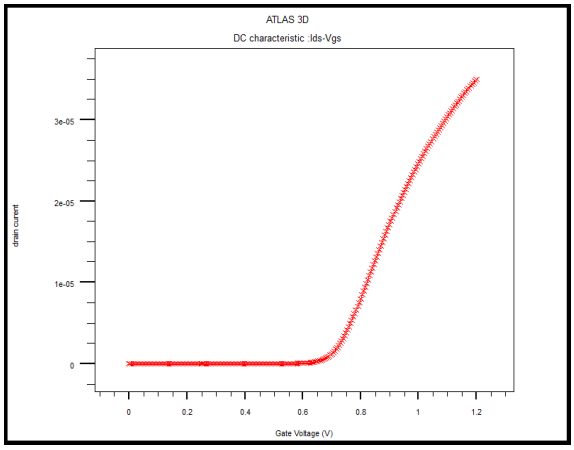


Figure 3. Transfer characteristic of a four channel rectangular GAA

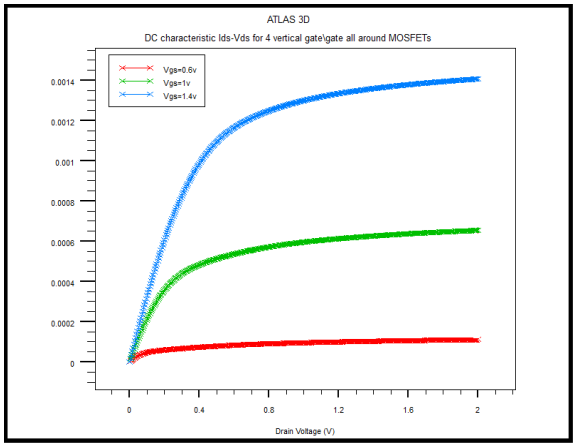


Figure 4. Output characteristics of our four channels rectangular GAA MOSFETs.

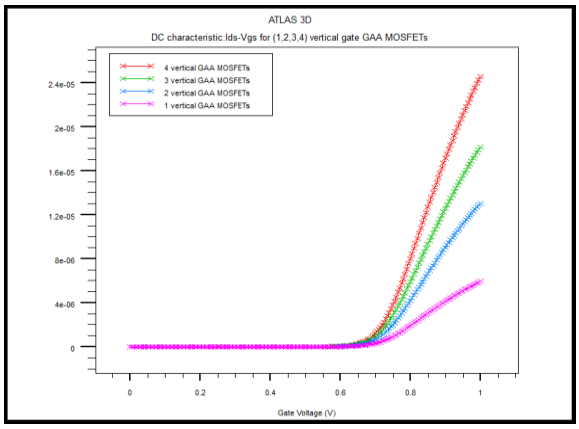


Figure 5. Transfer Characteristics of one, two, three and four channels rectangular GAA

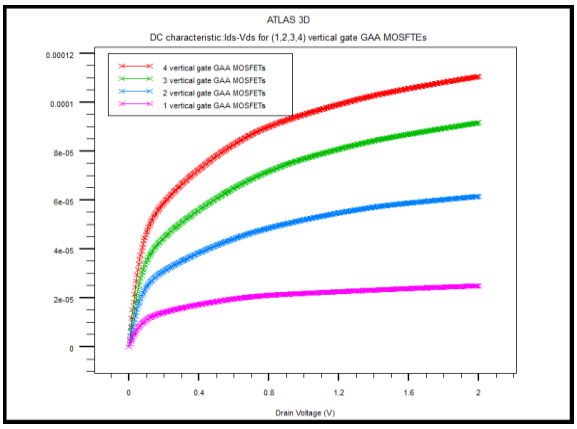


Figure 6. Output Characteristics for (one channel, two channel, three channel and four channel vertical rectangular GAA MOSFETs

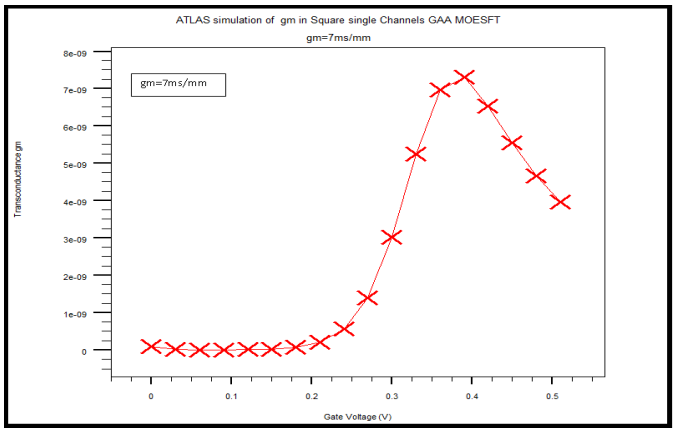


Figure 7. Transconductance g_m versus gate voltage for one channel rectangular GAA MOSFET

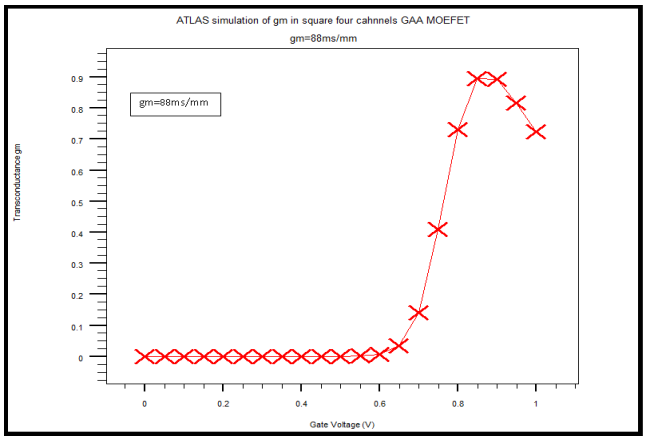


Figure 8.Transconductance g_m versus gate voltage for four channels rectangular GAA MOSFET

The simulated curves exhibit a maximum of 7ms/µm in single channels and 88ms/µm in four channels GAA MOESFT at V_{DS}=1.0 V. This peak appearing in the curve of the transconductance depends mainly on the gate bias V_{GS} and reflects the DC behavior of the simulated MOSFETs, which correspond to the channels modulated by different gate voltages. The DC characteristics obtained for a four channels devices are better, compared with a sample channel device that has obviously a slight inferior electrical properties earlier reported [23-24], the total parasitic resistance is usually dominated at low Ohmic contact resistance which is highly wanted, and can be attributed to the increase of carrier concentration or/and the increase of carrier mobility [25-27], We can note from our results that the g_m value is more important for our four channel GAA MOEFTS compared to the single channel one .

Table 2. Variation of the device electrical parameters as function of channels number

	One Channel GAA MOSFET	Two Channels GAA MOSFET	Three Channels GAA MOSFET	Four Channels GAA MOSFET
Dibl (mv/v)	60	55	50	40
Ion(A)	5.35E-07	1.24E-07	1.73E-07	2.28E-6
Ioff(A)	2.13E-13	1.80E-12	1.94E-12	1.78E-11
Ion/Ioff	2,5E6	0.68E5	0.89E5	1.20E5
SS (mV/dec)	62.5	73	73.7	72

One of the major challenges for the miniaturization of the MOS transistor is to ge t a high report Ion/Ioff. These nanometer MOSFET impose new technological challenges and reveal new phenomena that we cannot neglect, with Ion defined as the drain current when Vgs = V_{ds} = V_{dd} and I_{off} as the drain current when Vgs= 0 and V_{ds} = V_{dd} [28- 29].The MOSFETs have a high DIBL which is generally greater than 100mV / V for lengths less than 50 nm that we can show in Table 2. The reduction in channel lengths improves the electrostatic and thus reduces the DIBL (less than 20mV / V for a gate length of 50 nm).

4. CONCLUSION

In this work, a 3D simulation of 22nm four channels rectangular Gate MOSFETs on Si substrates using Silvaco software was presented. Our device exhibited high current density with a value of 30mA/mm, and a peak of extrinsic transconductance equal to 88ms/mm at V_{DS}=1 V, a cut-off frequency equal to 300GHz, fmax equal to 800 GHz and DIBL=60mV/V. These results demonstrate the possibility of using this technology in different application. This result also allows us to see the impact of channels number on the electrical characteristics of the device.

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