

TCAD Simulations and Small Signal Modeling of DMG AlGaN/GaN HFET

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ABSTRACT

This article presents extraction of small signal model parameters and TCAD simulation of novel asymmetric field plated dual material gate AlGa_N/Ga_N HFET first time. Small signal model is essential for design of LNA and microwave electronic circuit by using the proposed superior performance HFET structure. Superior performances of device are due to its dual material gate structure and field plate that can provide better electric field uniformity, suppression of short channel effects and improvement in carrier transport efficiency. In this article we used direct parameter extraction methodology in which S-parameters of device were measured using pinchoff cold FET biasing. The measured S-parameters are then transformed into Y-parameters to extract capacitive elements and then in to Z-parameters to extract series parasitic elements. Intrinsic parameters are extracted from Y-parameters after de-embedding all parasitic elements of device. Microwave figure of merits and dc performance are also studied for proposed HFET. The important figure of merits of device reported in the paper include transconductance, drain conductance, current gain, transducer power gain, available power gain, maximum stable gain, maximum frequency of oscillation, cut-off frequency, stability factor and time delay. Reported results are validated with experimental and simulation results for consistency accuracy.

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1. INTRODUCTION

Due to unique properties of GaN material, it is possible to obtain large current densities in GaN-based HFETs [1], [2]. GaN based devices are also very useful for high frequency high temperature microwave applications such as radar systems [3], [4]. In the recent past, studies have been done on asymmetric MOSFETs [5], junctionless FETs [6] and dual material gate AlGaAs/GaAs HEMTs structures that uses two metals of different work functions [7]. Since analytical models help us to understand internal solid state device physics thus expected to be consistent with physical behavior of device. An accurate small signal model of HFET is extremely valuable for designing of important active circuits generally used for high frequency applications [8-9]

These small signal compact models define physical characteristics and various limitations of active devices accurately [11], thus used for design of low noise power amplifiers by electronics and microwave engineers in industry. Small signal models of advanced devices are needed for CAD based simulations [12] for analysis and validation of newly developed device structures [13]. In present scenario, analytical models are much exploited for getting true feedback about optimization of fabrication process in semiconductor industries [14], [15]. In past most of small signal models developed for conventional HEMT structures are based on various approaches of device modelling [16], [17]. One of initial kind of detailed small signal

model that describe extraction procedure of FET structures, was proposed in 1988 by Dambrine, et al [18]. In recent past many researchers have developed variety of techniques and methods according to their used material system and conventional device structures [19], [20]. Requirement for development of small signal model for DMG AlGa_{0.3}N/GaN HEMT structure is felt since long but no such model for enhanced device structure is reported in recent past. In this paper we proposed small signal model for DMG GaN HFET structure incorporating field plate that can be exploited for advanced microwave circuit designs and for CAD based simulations.

It is possible to classify some existing modeling methods in three broad categories: whole optimization, partial optimization [21] and direct extraction methods [22], [23]. For the proposed DMG AlGa_{0.3}N/GaN HFET, the direct parameter extraction approach is used as it provides better consistency between parameter values and physical structure of device. This approach also facilitates extraction process to run faster than other techniques described earlier. Extraction is carried out using low as well as higher frequency as cold FET structure thus assures higher extraction accuracy [24]. Extracted small signal model parameters and dc as well as ac simulation results can provide clear insight about use of proposed device for microwave ranges of frequencies.

2. DEVICE STRUCTURE AND MODEL FORMULATION

2.1. Device Structure for Parameter Extraction and TCAD Simulations

Self explanatory schematic view of device structure of dual channel dual material gate Al_{0.3}Ga_{0.7}N/GaN HFET is shown in Figure 1(a). In the proposed unique device the dual material concepts are based on previously fabricated devices by W. Long et al. [7]. Epitaxial layers of HFET were grown by MOCVD on a 2.5-inch sapphire substrate. Drain and source terminal ohmic contacts were formed by Ti/Al/Ni/Au metal stacks, followed by rapid thermal annealing at 884°C for 50 seconds in nitrogen environment. Dual material gate was e-beam defined keeping total gate length of 1µm. Ni/Au metallization process was used to form dual metal gate Schottky contacts with the AlGa_{0.3}N cap layer. A Si₃N₄ surface passivation layer was deposited using PECVD. In order to reduce source inductance via-holes were formed using plasma dry etching. Field plate is formed to increase E-field uniformity that further reduces current collapse in device (Li, et al., 2016).

For completing the fabrication process of the device using 100µm² gate area a standard gold plated air brdge process was used. Metals M₁ (Au) and M₂ (Ni) having work functions φ_{M1}(=5.3eV) and φ_{M2}(=4.4 eV) respectively define dual metal gate with width W (=100µm) for the device. A 3nm AlGa_{0.3}N cap layer interface between n-Al_{0.3}Ga_{0.7}N layer of 18 nm thickness that is followed by UID AlGa_{0.3}N spacer layer of 3 nm thickness. Purpose of introducing UID AlGa_{0.3}N spacer layer is to reduce ionized impurity scattering. A 2µm thick GaN channel layer is used to form heterointerface that creates 2-DEG conductive channel in the device. Sapphire substrate is used for device structure as it can withstand higher operating temperature as a power switching device.

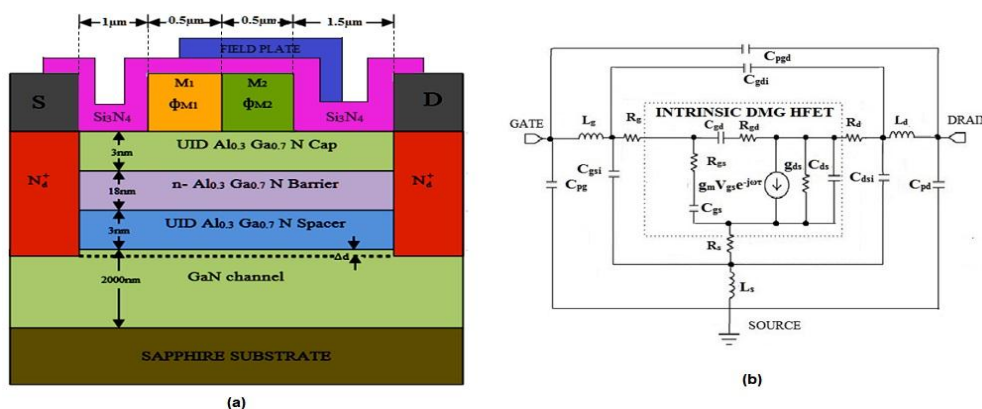


Figure 1. (a) Cross sectional schematic of enhanced asymmetric DMG Al_{0.3}Ga_{0.7}N/GaN HFET (b) Small signal equivalent circuit model

2.2. Analytical Small Signal Circuit Mode Description

Figure 1(b) represents small signal equivalent circuit model for the proposed unique device structure. R_g, R_s and R_d represent parasitic resistances of gate, source and drain respectively. L_s, L_d, L_g

represent source, drain and gate electrodes inductances respectively. C_{pd} , C_{pg} , and C_{pgd} , represent device contact pad capacitances between drain-source, gate-source and gate drain respectively. C_{pdi} , C_{pgdi} , and C_{pgi} are inter-electrodes capacitances between drain-source, gate-drain and gate-source respectively. R_{gs} and R_{gd} represent input and output channel region resistances. C_{ds} , C_{gs} , and C_{gd} , represent intrinsic capacitances between drain-source, gate-source and gate-drain respectively. g_{ds} and g_m represents drain conductance and transconductance of device. The $g_m V_{gs}$ in small signal model represent current generator in the output circuit, where V_{gs} represents as gate to source voltage with a phase shift of $e^{-j\omega\tau}$. Symbol (τ) represents transit time through the velocity saturated region of the 2DEG-channel. The ω is angular frequency (rad/sec) of the applied RF signal at gate terminal of device.

2.3. Method for Parameter Extraction

Parameter extraction is performed by using direct method as suggested by Minasian [25] and later modified by Dambrine et al [18] and Bertho and Bosch [26]. Initially S-parameter extraction is carried out for shunt extrinsic elements of device under pinch off mode of biasing keeping frequency with in 5GHz range thre after for series elements at higher frequency range. These measured S-parameters are then successively transformed into Y-parameters and then in to Z-parameters in order to obtain values of all the shunt and series parasitic elements. Again after de-embedding of all the parasitic elements, the intrinsic Y-parameters are obtained. At the end intrinsic elements are derived by separating real and imaginary parts of intrinsic Y-parameters.

2.4. Extrinsic Parameters Extraction and Analytical Expressions

The extrinsic capacitive elements are extracted from imaginary Y-parameters under pinch-off condition ($V_{gs} < V_{pinch-off}$ and $V_{ds}=0V$). Now the equivalent voltage controlled current source forming intrinsic part of device is disabled. In case of low frequency input in the range of 5 GHz, the whole circuit can be treated as a capacitive network as shown in Figure 2(a). Following Equations can appropriately describe the relationship between extrinsic capacitances and imaginary parts of the Y-parameters under pinched off condition:

$$\text{Im}(Y_{11}) = j\omega(C_{pg} + C_{gsi} + C_{gsp} + C_{gdp} + C_{gdi} + C_{pgd}) \quad (1)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -j\omega(C_{gdp} + C_{gdi} + C_{pgd}) \quad (2)$$

$$\text{Im}(Y_{22}) = j\omega(C_{dsp} + C_{pd} + C_{dsi} + C_{gdp} + C_{gdi} + C_{pgd}) \quad (3)$$

In Figure 2(b) imaginary Y-parameter curves with in frequency range of 5GHz are shown. It is clear that Y-parameters have sufficient linearity at low frequency range (below 5GHz). Therefore, the parasitic capacitances can be safely extracted from the slop of imaginary Y-parameter curves. Here, C_{gsp} , C_{gdp} and C_{dsp} provide intrinsic substitute of pinched of cold FET part of circuit. Assumption is made as [27]

$$C_{dsp} = 12C_{pd} \quad (4)$$

Due to asymmetric device structure ratio of gate-drain spacing with that of gate-source spacing is 1.5. So the relationship of its capacitance can be expressed as

$$C_{gsp} = 1.5C_{gdp} \quad (5)$$

Since size and shape of all pads are same so these capacitances can be treated as equal in value as

$$C_{pg} = C_{pd} = C_{pgd} \quad (6)$$

Considering device structure C_{dsi} is larger than pad capacitances. An assumption is made here as

$$C_{gdp} = C_{gdi} \quad (7)$$

Under high frequency small input signal with gate forward biased ($V_{gs} \geq 0$) drain at zero potential ($V_{ds} = 0V$), small signal equivalent circuit is reduced as in Figure 3(a). In this condition gate leakage current (I_g) flows and internal device capacitances are shunted with conductance open circuited. Since all inter electrodes capacitances are inside of parasitic resistance so no approximation needed by keeping precision of compact model as intact. At this specific bias point, the following simplified Equations of Z-parameters are valid:

$$Z_{11} = R_s + R_g + \frac{R_c}{1+r} + \frac{\eta kT}{qI_g} + j\omega(L_s + L_g) + \frac{1}{j\omega C_{gf}} + \frac{1}{j\omega C_{sf}} \quad (8)$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{r} + j\omega L_s + \frac{1}{j\omega C_{sf}} \quad (9)$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) + \frac{1}{j\omega C_{df}} + \frac{1}{j\omega C_{sf}} \quad (10)$$

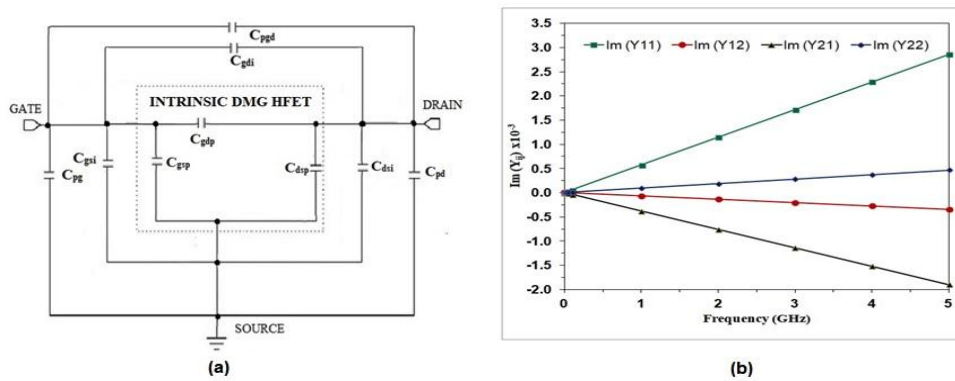


Figure 2. (a) Reduced equivalent circuit under low frequency cold FET pinchoff condition (b) Imaginary Y-parameters versus frequency plot

In the above expressions, R_c , represents channel resistance and r represents ratio of channel resistance between gate to drain and gate to source i.e ($r = R_{cgd} / R_{cgs}$). As per our proposed asymmetric device structure value of r is 1.5 considering source and drain separation from gate. C_{df} , C_{gf} and C_{sf} , represent fringing capacitances resulting at drain, gate and source terminals respectively in cold FET high frequency equivalent circuit. Also $\eta kT / qI_g$ in Equation (8) gives the differential resistance of the Schottky diode. In this expression, η , K and T represent ideality factor of diode, Boltzmann constant and absolute ambient temperature respectively. Now by transforming Y-parameters in to Z-parameters, R_g , R_s and R_d can be extracted from the $Re(Z_{ij})$ curves. By multiplying ω by imaginary parts of impedances, following expressions are obtained

$$\text{Im}(\omega Z_{11}) = \omega^2(L_s + L_g) - \frac{1}{C_{gf}} - \frac{1}{C_{sf}} \quad (11)$$

$$\text{Im}(\omega Z_{12}) = \omega^2 L_s - \frac{1}{C_{sf}} \quad (12)$$

$$\text{Im}(\omega Z_{22}) = \omega^2(L_s + L_d) - \frac{1}{C_{df}} + \frac{1}{C_{sf}} \quad (13)$$

The $\omega \text{Im}(Z_{ij})$ versus ω^2 plot is shown in Figure 3(b). Slope of these curves can be used to extract values of L_g , L_d and L_s respectively. The imaginary part of the Z-parameters increases linearly with frequency but real part is independent from frequency variations. The value of R_c is determined by forming following Equations by using pinch off Z-parameters as follows

$$\text{Re}(Z_{22 \text{ pinch-off}}) = R_s + R_d \quad (14)$$

Also, from Equation (10) it is noted that

$$\text{Re}(Z_{22}) = R_c + R_d + R_s \quad (15)$$

$$R_c = \text{Re}(Z_{22}) - \text{Re}(Z_{22 \text{ pinch-off}}) \quad (16)$$

2.5. Intrinsic Parameters Extraction and Analytical Expressions

The intrinsic part of the device can be described by the following Y-parameters:

$$Y_{11 \text{int}} = \frac{\omega^2 C_{gs}^2 R_{gs}}{\delta} + \frac{\omega^2 C_{gd}^2 R_{gd}}{\theta} + j\omega \left(\frac{C_{gs}}{\delta} + \frac{C_{gd}}{\theta} \right) \quad (17)$$

$$Y_{12 \text{int}} = -\frac{\omega^2 C_{gd}^2 R_{gd}}{\theta} - j\omega \frac{C_{gd}}{\theta} \quad (18)$$

$$Y_{21 \text{int}} = g_m e^{-j\omega\tau} - \frac{\omega^2 C_{gd}^2 R_{gd}}{\theta} - j\omega \frac{C_{gd}}{\theta} \quad (19)$$

$$Y_{22 \text{int}} = g_{ds} + \frac{\omega^2 C_{gd}^2 R_{gd}}{\theta} + j\omega \left(C_{ds} + \frac{C_{gd}}{\theta} \right) \quad (20)$$

where

$$\delta = 1 + u^2 \quad (21)$$

$$u = \omega C_{gs} R_{gs} \quad (22)$$

$$\theta = 1 + v^2 \quad (23)$$

$$v = \omega C_{gd} R_{gd} \quad (24)$$

Therefore, the value of individual intrinsic parameter can be derived from Equations (17) to (20) by separating real and imaginary parts of $Y_{11 \text{int}}$, $Y_{12 \text{int}}$, $Y_{21 \text{int}}$ and $Y_{22 \text{int}}$ and using following expressions

$$C_{gd} = -(1 - v^2) \frac{\text{Im}(Y_{12 \text{int}})}{\omega} \quad (25)$$

$$R_{gd} = \frac{v}{(1 + v^2) \text{Im}(Y_{12 \text{int}})} \quad (26)$$

$$C_{gs} = (1 + u^2) \frac{\text{Im}(Y_{11 \text{int}}) + \text{Im}(Y_{12 \text{int}})}{\omega} \quad (27)$$

$$R_{gs} = \frac{u}{1 - u^2} \text{Im}(Y_{11 \text{int}} + Y_{12 \text{int}}) \quad (28)$$

$$g_m = |Y_{21int} - Y_{12int}| \tag{29}$$

$$\tau = -\frac{1}{\omega} \arctan\left(\frac{\text{Im}(Y_{21int} - Y_{12int})}{\text{Re}(Y_{21int} - Y_{12int})}\right) \tag{30}$$

$$C_{ds} = \frac{\text{Im}(Y_{22int} + Y_{12int})}{\omega} \tag{31}$$

$$g_{ds} = \text{Re}(Y_{22int} + Y_{12int}) \tag{32}$$

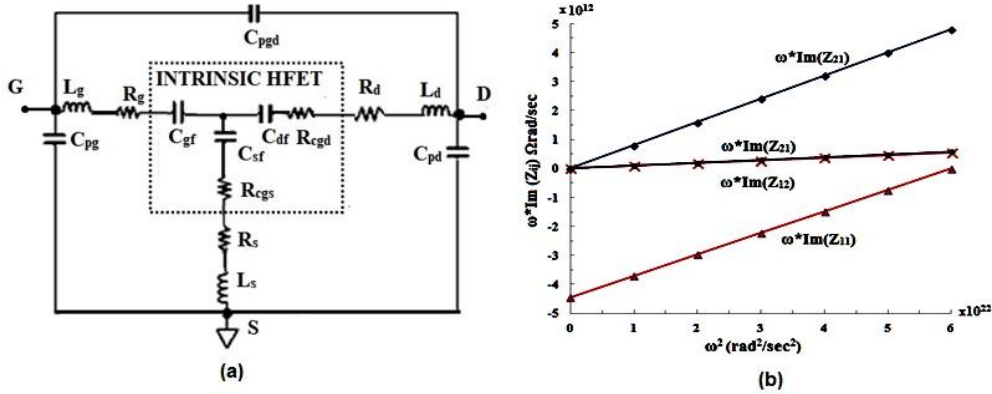


Figure 3. (a) Reduced cold FET high frequency equivalent circuit under forward gate bias ($V_{gs} > 0$) (b) $\omega \text{Im}(Z_{ij})$ versus ω^2 plot

Extrinsic parameters as listed in Table 1, are extracted for $1 \times 100 \mu\text{m}^2$ gate size device at ambient temperature (T) = 305K. The capacitances are extracted for $f_L=0$ to 5GHz, $V_{gs} = -8\text{V}$, $V_{ds}=0\text{V}$. For series inductances and resistances, $f_H=5$ to 200GHz, $V_{gs} = -3\text{V}$, $V_{ds}=0\text{V}$ is applied. Intrinsic parameters as listed in Table 2, are extracted from S-parameters measured at $V_{ds}=10\text{V}$ and $V_{gs} = -1\text{V}$, $T=305\text{K}$, $f_H=5$ to 200 GHz. These parameters are also validated with recently reported results [28] [29].

Table 1. Extracted extrinsic parameters of small signal circuit model

Extrinsic Parameters	L_g	L_s	L_d	R_g	R_d	R_s	C_{pg}	C_{pd}	C_{pgd}	C_{dsi}	C_{gsi}	C_{gdi}
Value	42.4pH	0.6pH	52.5pH	6.5Ω	11.2Ω	4.2Ω	18fF	23fF	13fF	18fF	18fF	5fF

Table 2. Extracted intrinsic parameters of small signal circuit model

Intrinsic Parameter	C_{gd}	C_{gs}	C_{ds}	R_{gd}	R_{gs}	g_{ds}	g_m	τ
Value	2.22fF	1.23fF	2.12fF	1.8KΩ	3.1Ω	500mS/mm	800mS/mm	0.91pS

2.6. Characterization and Modelling of Microwave Figures of Merits

Microwave performance of device was characterized using Agilent Technologies N5230A network analyzer. The system calibration ensured with a short-open load-through calibration standard. Figure 4 shows block diagram for extraction of S-parameters by using two port matching lossless output and input network. Circuit shows E_s , Z_s and Z_L as excitation source, source impedance and load impedances respectively. P_i , P_A , P_L and P_{avo} represent input power, available input power, power delivered to load and available power at output respectively.

Paper models following figure of merits for proposed unique device P Transducer power gain (G_{TP})

$$G_{TP} = \frac{P_L}{P_A} \quad (33)$$

For $S_{12}=0$ values unilateral transducer power gain (G_{UTP}) is obtained as

$$G_{UTP} = \frac{P_L}{P_{A_{S_{12}=0}}} \quad (34)$$

Available power gain (G_{AP})

$$G_{AP} = \frac{P_{avo}}{P_A} \quad (35)$$

Since $P_{avo} \leq P_A$, thus power gain $G_{AP} \geq G_{TP}$

Maximum available gain (G_{MAX}) occurs for the simultaneous conjugate match at the input and output port if the transistor is unconditionally stable i.e. ($k > 1$) and given as

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|} \left(k \pm \sqrt{k^2 - 1} \right) \quad (36)$$

Where k represents stability factor of device and obtained as

$$k = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad (37)$$

Maximum stable gain (G_{MS}) occurs when the two port are resistively loaded till stability factor becomes unity i.e. ($k = 1$), G_{MAX} of the two port of Equation (36) becomes maximum stable gain and obtained as

$$G_{MS} = \frac{|S_{21}|}{|S_{12}|} \quad (38)$$

Maximum unilateral transducer power gain (G_{UTPM}) is obtained when the transistor becomes unconditionally stable and obtained as

$$G_{UTPM} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \quad (39)$$

Maximum unilateral power gain (G_{UPM}) is largest gain and obtained as

$$G_{UPM} = \frac{\frac{1}{2} \left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{k \left| \frac{S_{21}}{S_{12}} \right| - \text{Re} \left(\frac{S_{21}}{S_{12}} \right)} \quad (40)$$

Current gain $|H_{21}|$ is important and used to obtain cut off frequency of device

$$|H_{21}| = \frac{2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \quad (41)$$

Cut off frequency (f_c) for DCDMG AlGaIn HEMT at which short circuit current gain rolls off to 0 dB can be obtained as

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})[1 + (R_s + R_d)g_{ds}] + C_{gd}g_m(R_s + R_d)} \tag{42}$$

Maximum oscillation frequency (f_{max}) can be determined by using intrinsic and extrinsic components of device as

$$f_{max} = \frac{f_t}{2\sqrt{((R_g + R_s + R_{gs})g_{ds} + 2\pi f_t C_{gd} R_g)}} \tag{43}$$

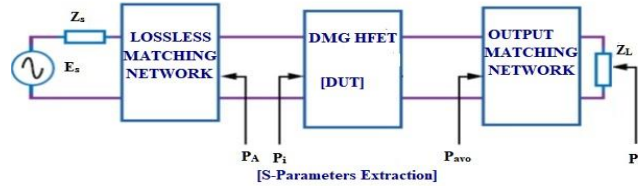


Figure 4. Block diagram of matching impedance network for s-parameters measurement

3. RESULTS AND DISCUSSIONS

We used MATLAB and Silvaco TCAD ISE [13] as modeling and device simulation tools respectively for our research work. GaN material based device models (print srh, albrct.n) and polarization based models are applied for considering piezoelectric and spontaneous polarization effects at the heterointerface of the GaN device structure as described in ATLAS user manual of Sivaco TCAD. Figure 5(a) shows comparison of simulated [13] and experimental [30] output current voltage characteristics of device for various gate-to-source voltages (V_{gs}). Figure 5(b) shows comparison of simulated and experimental [30] input characteristics of DMG AlGaIn/GaN HFET. It is evident from graph that gate has effective control on drain current in DE mode of operation.

The device stability analysis has been done with the help of Smith plots. Figure 6(a) shows model and measured s-parameters [29]. Smith plots analysis reveals that proposed device capacitance increases with frequency. At the lowest input frequency the input reflection coefficient, i.e. $S_{11}=+1$, represents maximum reflection and open circuit. With the rise in frequency the input reflection coefficient moves towards clockwise direction in the circle of capacitance and approaches to the matching point at $S_{11}=0$. Since, at the matching point no reflections would occur because of the impedance matching and this confirms good performance of device at higher frequency range. Similarly output reflection coefficient S_{22} moves from maximum reflection to minimum reflection towards matching point in the circle of capacitances. Graphs also depicts that with rise in frequency, both the transmission coefficients (S_{21}) and (S_{12}) move towards clockwise direction in the circle of inductances assuring good performance of device at microwave frequency range.

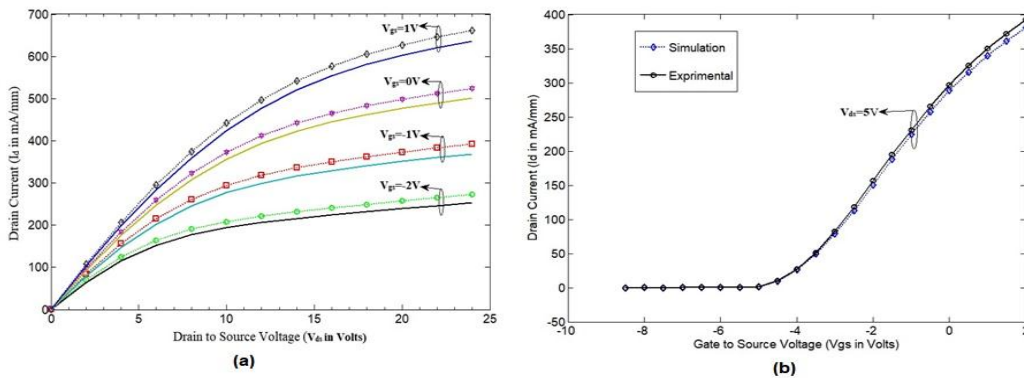


Figure 5. (a) Output current voltage (I_d - V_{ds}) characteristics simulated (dashed lines with symbols) experimental (solid lines symbols) (b) Transfer (I_d - V_{gs}) characteristics curve

The device simulation and measured gains [19], [30] are plotted as a function of frequency at a gate bias of $V_{gs}=-1V$ in Figure 6(b). On comparison the results are found to be within close conformity thus validating device performance in microwave frequency range. Graph clearly demonstrates that the gains decrease with the rise in frequency and the cut-off frequency (f_t) occurs at 68 GHz and maximum oscillation (f_{max}) occurs at 178GHz. In Figure 7(a), the variation of capacitances i.e. C_{gd} , C_{gs} , C_{gg} and C_{ds} are demonstrated with the rise in frequency. It clearly shows that capacitance values remain almost constant up to 200GHz frequency range that is covering maximum oscillation frequency of device. Figure 7(b) demonstrates the simulated and experimental variation of cutoff frequency with V_{gs} at the $V_{ds}=24V$. Figure 8 shows variation of simulated and experimental transconductance with V_{gs} . Comparison of simulation and experimental results [30] validate device suitability for microwave range of frequency.

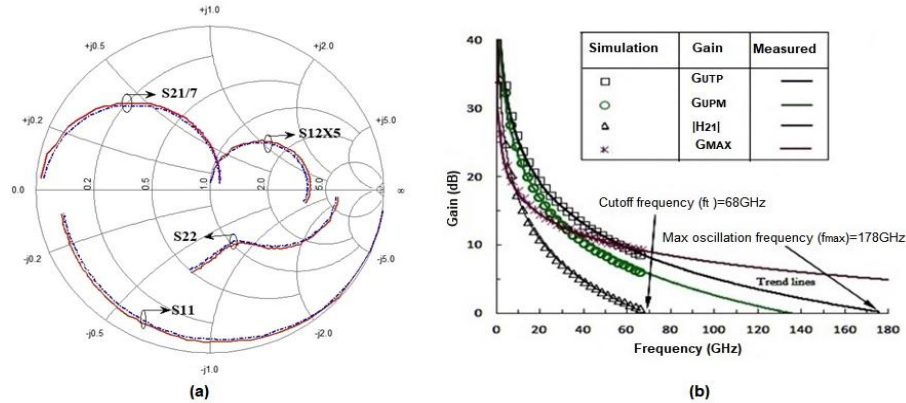


Figure 6. S-parameters (S11, S12, S21 and S22) plot on smith chart, simulated (dashed blue lines) measured (solid red lines) at bias $V_{ds}=24V$ and $V_{gs}= -1V$, frequency $f_{start}=1GHz$ and $f_{stop}=200 GHz$ (b) Gains versus frequency plot for $V_{ds}=24V$ and $V_{gs}= -1V$.

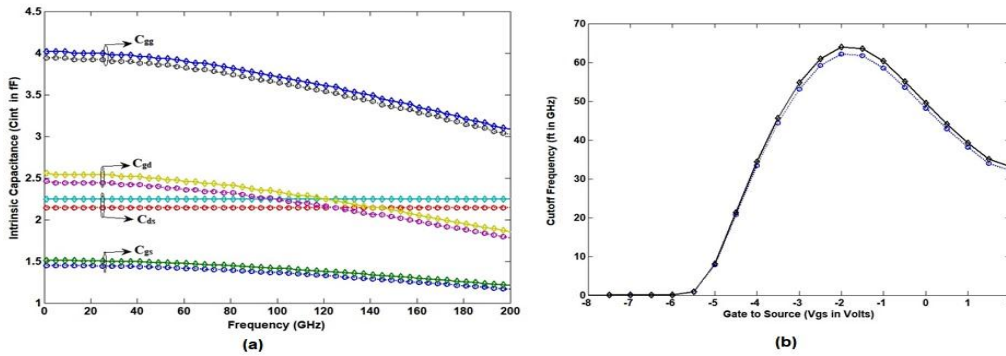


Figure 7 (a) Capacitances versus frequency plot model (dashed lines with circles) simulation (solid lines with diamonds) at $V_{ds}=5V$ and $V_{gs}= -1V$ (b) Cutoff frequency versus V_{gs} plot, simulation (solid line with diamonds) experimental (dashed line with circles) at $V_{ds}=5V$

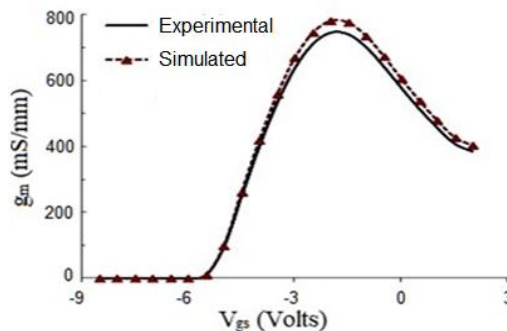


Figure 8 Transconductance (g_m) versus gate to source voltage (V_{gs})

4. CONCLUSION

Finally it can be concluded that the extracted small signal model parameters of dual material gate $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ HFET structure are accurate and predict proposed device suitability for LNA that can operate in microwave range of frequencies. Device structure is simulated for analysis of transfer characteristics, output current voltage characteristics and microwave figure of merits. Simulated results are compared with experimental data to analyze device performance and behavior under dc biasing. We obtained maximum oscillation frequency (f_{max}) of 178 GHz and cut-off frequency (f_t) of 68 GHz as enhanced device features. Important figure of merits analysed and reported in the article include current gain $|H_{21}|$, transducer power gain (G_{TP}), unilateral transducer power gain (G_{UTP}), maximum stable gain (G_{MS}), maximum available gain (G_{MAX}), transconductance (g_m), drain conductance (g_{ds}), stern stability factor (k), available power gain (G_{AP}) and time delay (τ) to assess microwave performance of proposed device. Extracted parameters are validated for consistency and accuracy with experimental results and found to be in close conformity.

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