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Performance Analysis of 3-Level 5-Phase Multilevel Inverter Topologies

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ABSTRACT

Now a day's many industrial applications requires high power. Some other appliances may require intermediate power either more or less depending upon their operation. With these consequences, MULTI LEVEL INVERTERS are introduced in 1975.for above intermediate voltage applications. The name MULTI LEVEL began with the three-level converter.By enormous advancement in power semiconductor switches, in electric drives increasing the phase number greater than the conventional three phase especially in locomotives, naval, aerospace, and electrical vehicles industry has many advantages than three phase. In this view, here five phase VSI has developed. This paper aims at comparing the performance of conventional two level inverter Diode clamped and Capacitor clamped topologies of 5-phase multilevel inverter (3-level) using sinusoidal pulse width modulation. SPWM is highly economical, has more efficiency, controllability. These circuits are analyzed by using simulation software package such as MATLAB.

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1. INTRODUCTION

An inverter takes the input signal from the rectifier i.e unidirectional current and the output of the inverter is a sinusoidal square wave with distortion.

Now-a-days, with the advancement of the power electronic devices are efficiently employed for high voltage and high current applications. Here with the conventional inverters comprise various problems are related to low power quality, immense voltage stresses, common mode noise, pressure on motor bearing etc. These problems are overcome by increasing the number phases and levels instead of conventional inverters, called as multi level [1], [2] inverters**.** Multiphase (more than three phases) is very much popular due to their eminent features compared to conventional three-phase counter parts. In order to drive the multiphase machine, it requires same phase input w.r.t the number of phases at the output. This paper mainly focuses on five phase, because even after failure of one phase, the performance does not degraded much [3], [4]. At this juncture, five phase two level, three level inverter topologies are presented. The main motto of the five phase topologies are preferred because it eliminates the fifth harmonics and multiples of five.

2. TWO LEVEL FIVE PHASE INVERTER

Single-phase Voltage source inverters are favored for flat capability operations, three phase VSI's are favored for intermediate to immense operations. Whereas multi-phase VSI's are favored tremendous power applications. At this moment five phase topology is to develop to control amplitude, phase, and frequency. The five-phase VSI topology is shown in Figure 1.There are ten switches having a phase difference of 36^0. Each phase conducts 72^0. Upper leg switches are S_1, S_3, S_5, S_7, S_9 and lower leg switches are S_6,S_8,S_{10},S_2,S_4.In each leg, no two switches are (i.eS_1S_6, S_3S_8, S_5S_{10}, S_7S_2, S_9S_4) cannot be switched ON at a time, it could be causes the short circuit across the dc link voltage supply.

Five phase two level VSI be controlled in ten operating modes. In each mode five switches are conducting among two of them are from upper leg and three switches are from the lower leg or vice versa. Each leg phase shift is 72^0.The switches are turned ON and OFF as complimentary of the each leg i.e first leg have two switches S_1 and S_6, ifS_1 ON,S_6 in OFF mode. The conduction states are followed the same switching pattern in order to avoid the short circuit.

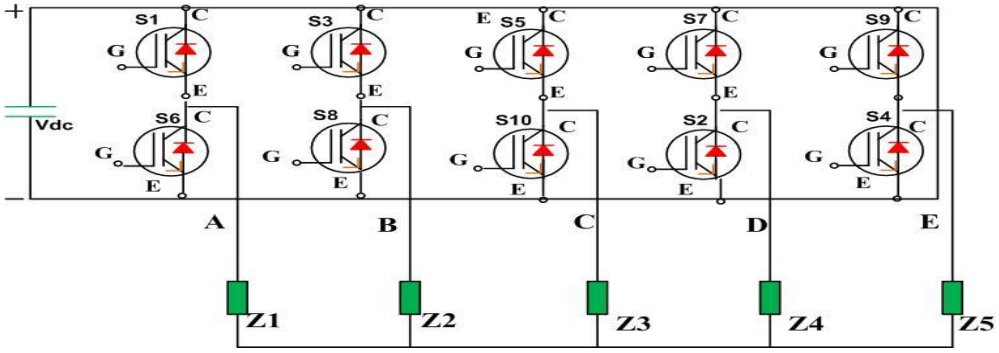


Figure 1. Conventional Two Level Five Leg Inverter

During mode I-$0 \leq \omega t \leq 36^0$, switches S_1, S_8, S_{10}, S_7, S_9 are turned on. Similarly the remaining switches are turned on according to their operating modes. Table I shows below the operating modes of conventional two level five phase or five leg inverter. All impedances are same connected to the switches. The impedances Z_1, Z_4, Z_5 are in parallel, and connected to positive polarity and Z_2, Z_3 are in parallel connected to negative polarity. The combinations of these two parallel connections of impedances are further connected in series with each other.

Table 1. Operating Modes of Five Phase Inverter

Operating Modes	Conduction Period	No. of Switches Turned ON
Mode I	$0 \leq \omega t \leq 36^0$	$S_1S_7S_8S_9S_{10}$
Mode II	$36^0 \leq \omega t \leq 72^0$	$S_1S_2S_8S_9S_{10}$
Mode III	$72^0 \leq \omega t \leq 108^0$	$S_1S_2S_3S_9S_{10}$
Mode IV	$108^0 \leq \omega t \leq 144^0$	$S_1S_2S_3S_4S_{10}$
Mode V	$144^0 \leq \omega t \leq 180^0$	$S_1S_2S_3S_4S_5$
Mode IV	$180 \leq \omega t \leq 216^0$	$S_2S_3S_4S_5S_6$
Mode VII	$216^0 \leq \omega t \leq 252^0$	$S_3S_4S_5S_6S_7$
Mode VIII	$252 \leq \omega t \leq 288^0$	$S_4S_5S_6S_7S_8$
Mode IX	$288^0 \leq \omega t \leq 324^0$	$S_5S_6S_7S_8S_9$
Mode X	$324^0 \leq \omega t \leq 360^0$	$S_6S_7S_8S_9S_{10}$

3. MULTILEVEL INVERTERS

By the attractive features of a multilevel converters like reduced common node voltage, stress across the switches etc, also less amount of switching losses operating at low switching frequency to get high efficiency of the converter and low distorted output, therefore these inverters are introduced with increasing number of levels and number of phases. Here, conventional multi level inverters are designed by increasing the number of phases [5-10].

3.1. Classification of Multilevel Converters

Multilevel inverters mainly categorized based on the type of source.

1. Common DC source
2. Separate DC source

In the common source DC inverters there are two topologies:

a. Diode clamped
b. Flying capacitor (Capacitor clamped)

In this paper, the emphasis is only on the Common DC source Inverters.

3.2. Five Phase Diode Clamped Multi Level (FDCML) Inverters

Five Phase DCML Inverters are mainly employing to diminish the voltage stress across the switching devices by transversally connected diodes. D.C voltage applied across the two clamped capacitors. The applied voltage collectively shared by the two capacitors as half of the applied dc voltage. The focal point of the DC link or the two capacitors be "O" it is common for all five phases.

The voltage dividing is accomplish with the help of the diodes connected to the neutral point and that is also why this topology is very often called diode-clamped topology and neutral point topology. Figure 2 represents the five phase diode clamped multi level inverter (FDCML), there are 20 power devices, 10 clamping diodes and 2 capacitors. All switches of individual phase are separated into complementary switching pairs: S_{a1} and S_{a2},S'_{a1} and S'_{a2},of one single leg which means that if one device from the complementary pair turns ON, further one be turn OFF and vice versa. Correspondingly for all the remaining leg switches are operated.

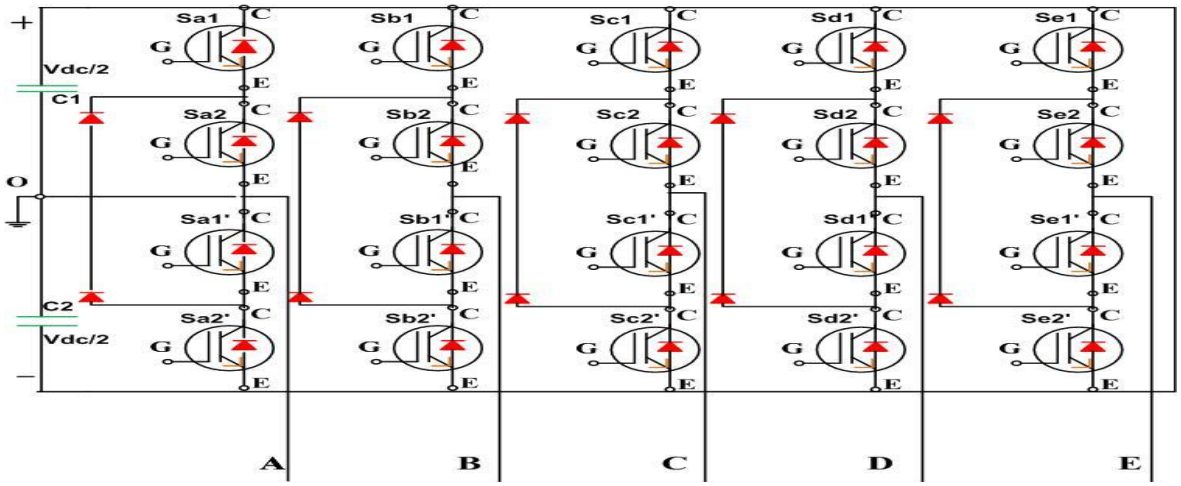


Figure 2. 3-level FDCML Inverter

The phase voltage V_{an} has operated in three modes: Vdc/2, 0, and –Vdc/2:
For the first operating mode ,Vdc/2 two devices are turned ON, here S_{a1}&S_{a2} to be ON; for negative polarity of dc voltage ,–Vdc/2 S'_{a1}&S'_{a2} to be ON; for 0 level, Sa2 and Sa1' to be ON. When switch ON it represents by "1", OFF means "0".

Advantages:

a. This type of multi level inverter can be generalized, and the principles used in the fundamental three level topology can be extended for use in topologies with any number of levels.
b. The applied Voltages shared as Vdc/2 across switching devices.
c. If number of levels is increased, it shows very low harmonic content it could be keep away from the requirement of filters.
d. Power devices are operated at low switching frequency, therefore switching losses are very low, and consequently efficiency is high.
e. Reactive power control is also possible.
f. In favor of back to back intertie system this control technique be employed.

Disadvantages:
a. The main drawback of the DCMLI, if number of levels increased, it necessitate enormous amount of clamping diodes.
b. It's firm to control real power in favor of respective converters.

3.3. FIVE PHASE FLY BACK CAPACITOR CLAMPED MULTI LEVEL INVERTER (FCMLI)

Meynard and Foch introduced a flying-capacitor-based inverter in 1992[5]. The arrangement of this inverter be analogous to the DCML inverter apart from the clamping diodes, capacitors are employed. If *N* level converter considered phase and line voltage is equal to the number of levels together with the reference, (2*N-1*) level respectively. Here every capacitor and the power device has the identical voltage rating, it requires (*N-1*) capacitors.

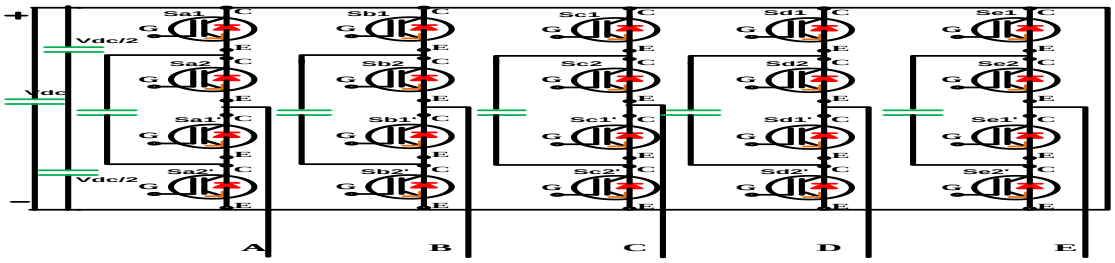


Figure 3. 3-level 5-leg Fly Back Capacitor clamped MLI

The voltage fusion in FCMLI be easy than a DCMLI. Here clamping capacitors gives the switching device voltage to one level of the capacitor voltage. The switching operation of FCMLI is not identical to the diode clamped multi level inverter.

Figure 3 represents the Five phase Fly Back Capacitor clamped multi level inverter (FDCML), there are 20 power devices, 5 clamping capacitors and 2 DC link capacitors.If anyone follow the similar operation of DCMLI, then capacitors are get short circuited. If the fly back capacitors are connected effectively, here capacitor voltage has no discharge path way because the capacitor connected switching devices are turned OFF. The operating modes of FCMLI are shown in Table 2.

Table 2. Switching States of Fly Back Capacitor Clamped Multi Level Inverter

Output Voltage	No Of Switches Turned ON			
	S_{a1}	S_{a2}	S'_{a1}	S'_{a2}
$V_{dc}/2$	1	1	0	0
	0	1	1	0
0	1	0	0	1
$-V_{dc}/2$	0	0	1	1

Advantages:
a. It overcomes the problems that are associated with the DCML inverter topologies i.e clamping diodes.
b. Moreover, balancing the capacitor charging and also diminishes the voltage stress across the power devices
c. It is possible to control equally active and reactive power being used in HVDC transmission.
d. Voltage levels of the capacitor balancing are offered by phase redundancies.
e. Similar to the diode clamped multi level inverter topology If No. of levels be increased, therefore the harmonic distortion will be very small, then no need of usage of filters in the circuit.

Disadvantages:
a. It is difficult to manage the voltage levels paths of all the capacitors.
b. In favor of real power transmission consumption of switching along with efficiency level are very poor.
c. Huge no. of capacitors are used, Therefore FCML inverters are more expensive and bulky than clamping diodes in DCML inverters.

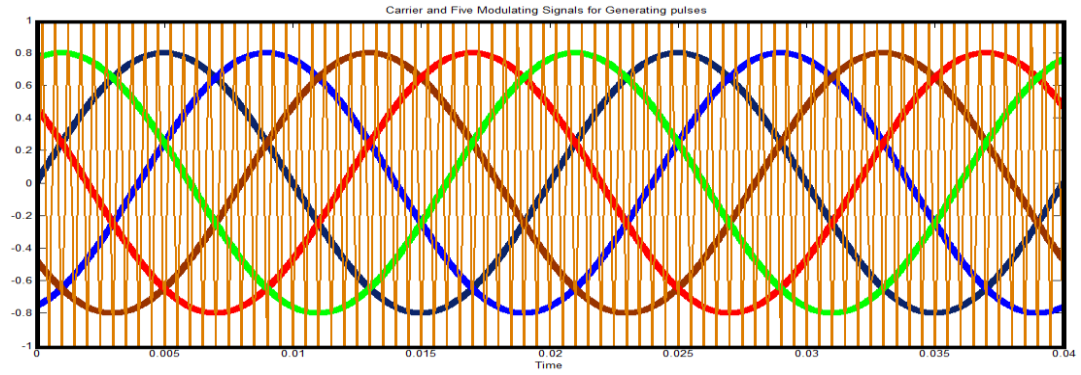
Control Strategies:

Extremely well known Pulse Width Modulation (PWM) procedure for two level are utilized to achieve

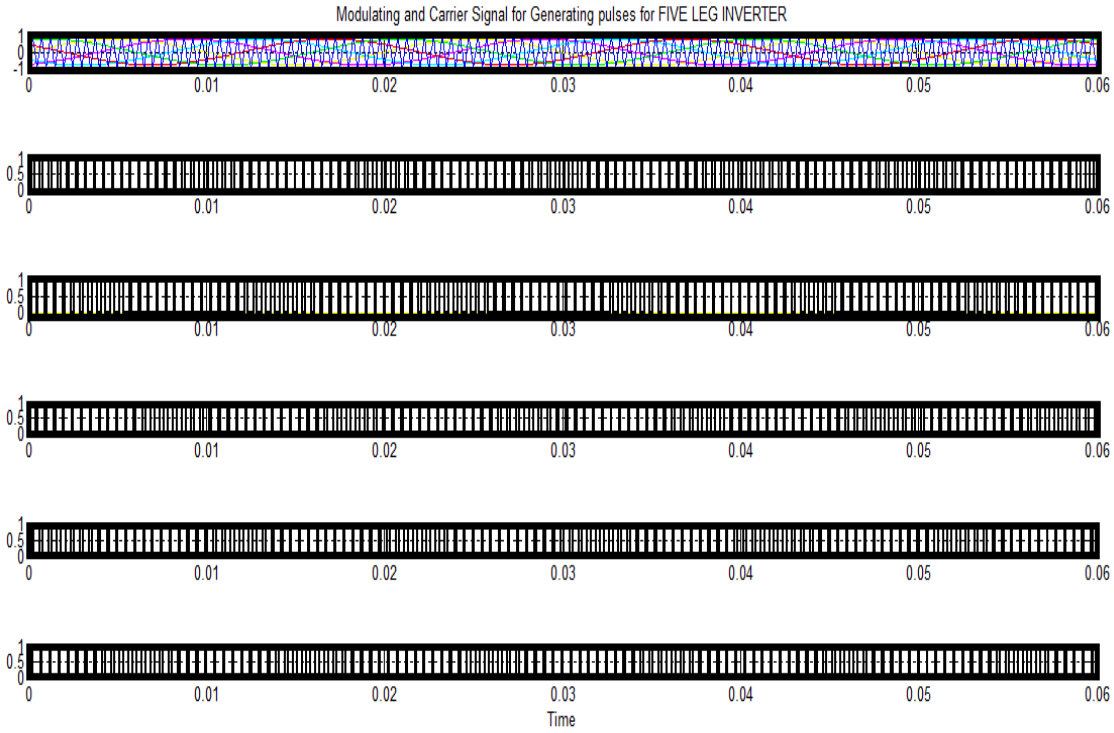
a. Ample continuous modulation spectrum
b. Diminished switching losses
c. Low total harmonic distortion.

For the most part of PWM schemes for high power inverters are the carrier based PWM (sine-triangle PWM or SPWM) techniques and the space vector based PWM techniques. SPWM schemes be more flexible furthermore simple to implement [8].

In general for an inverter has 'N' levels then the no. of carrier signals (N-1) are required. The modulating signal or the reference signal is a pure sine wave. Carrier wave frequency should be greater than the reference or modulating signal frequency.



(a)



(b)

Figure 4. (a) Carrier and Five Modulation Signals for Gating Pulse Generation Of Two Level Five Phase Converter, (b) Gating Pulse Generation Of Two Level Five Phase Converter

For five phase conventional two level inverter requires, only one carrier waveform and five modulation signals as shown in Figure 4(a) and generation of pulses for all the five phases using SPWM technique as shown in Figure 4(b).

For five phase three level inverter requires, two carrier waveforms which are in phase over and under zero reference value by 180^0 phase shift. Now considered only one leg of three level five Phase converter, one modulation signals as shown in Figure 5. Likewise the generation of pulses are obtained for all the five phases using SPWM–Phase opposition disposition technique.

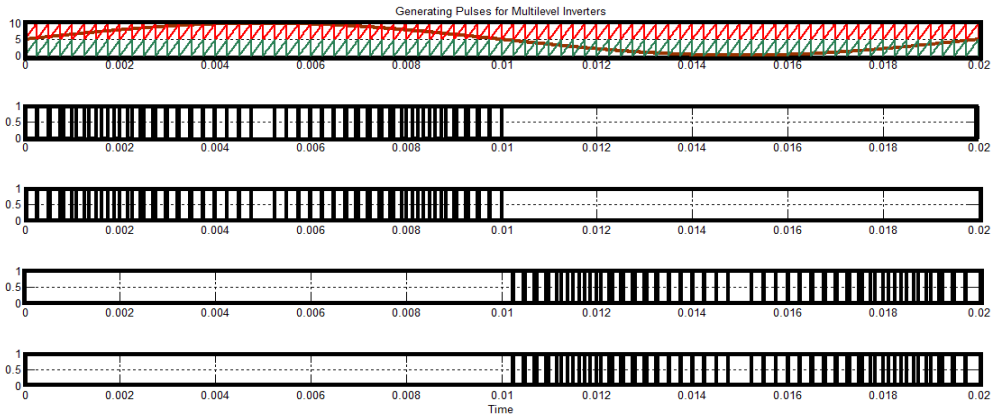
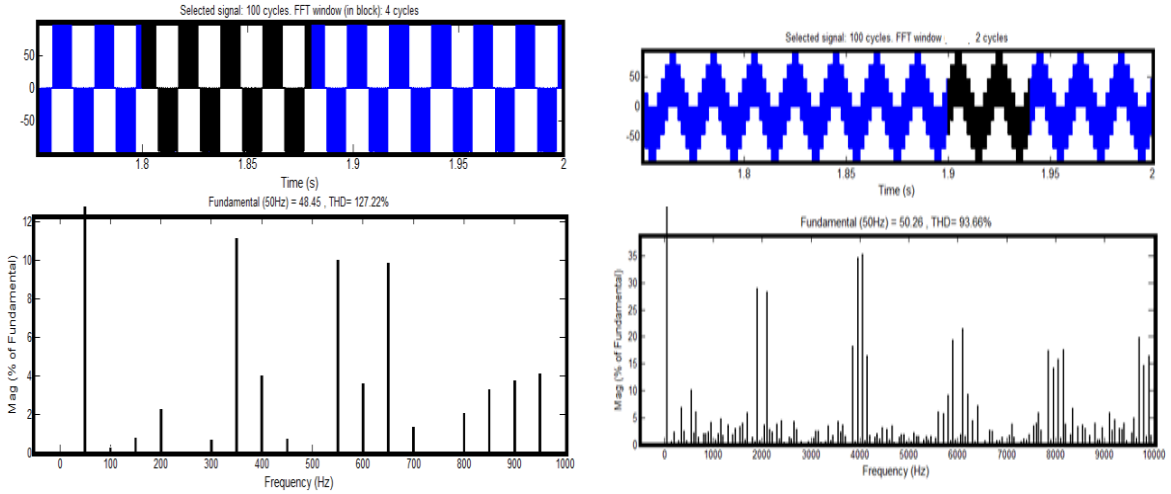


Figure 5. Carrier and Modulation Signal and Gating Pulse Generation Of Three Level Five Phase Converter – Single Leg

4. RESULTS

The simulations of five phase 2-level and 3-level inverters were carried out with dc supply of 100 V. The phase voltage and line voltage waveforms without and with filter are plotted. Using FFT analysis the fundamental values and total harmonic distortion are found shown in figures below and tabulated for a single leg (A-phase).

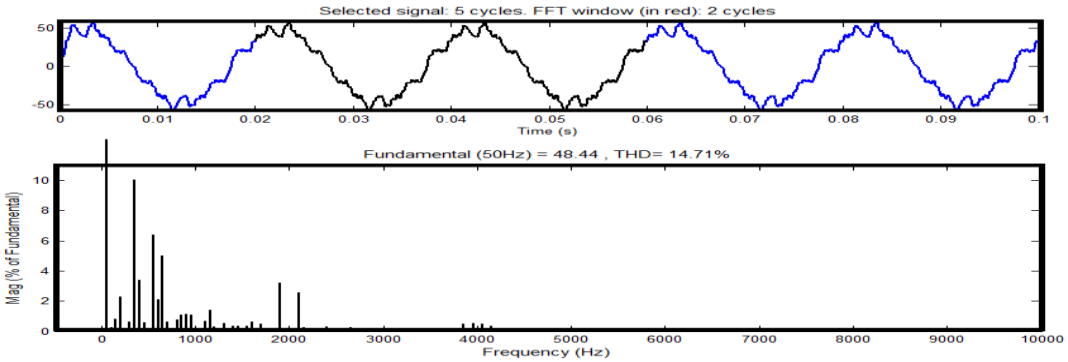
4.1. Conventional Two Level Line and Phase Voltages of Five Leg Inverter –Single Leg



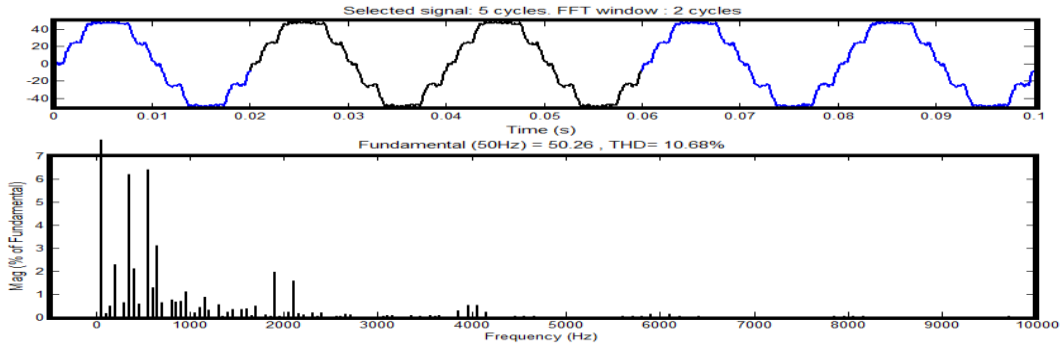
(a) (b)

Figure 6. (a) THD of Two Level Line Voltage of Five Leg Inverter-127.22%, (b) THD of Two Level Phase Voltage of Five Leg Inverter-93.66%

4.2. Two Level Filtered Line and Phase Voltages of Five Leg Inverter –Single Leg



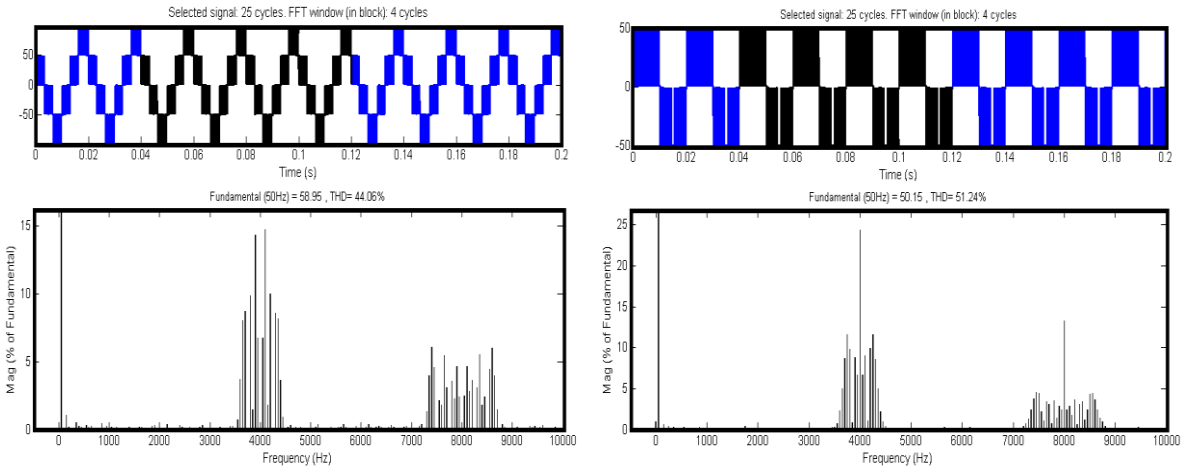
(a)



(b)

Figure 7. (a) THD of Two Level Filtered Line Voltage of Five Leg Inverter-14.71%, (b) THD of Two Level Filtered Line Voltage of Five Leg Inverter-10.68%

4.3. Three Level Line and Phase Voltages of Five Leg Diode Clamped Multilevel Inverter –Single Leg



(a) (b)

Figure 8. (a) THD of Three Level Line Voltage of Five Leg DCML Inverter-44.06%**,** (b) THD of Three Level Phase Voltage of Five Leg DCML Inverter-51.24%

4.4. Three Level Filtered Line and Phase Voltages of Five Leg Diode Clamped Multilevel Inverter – Single Leg

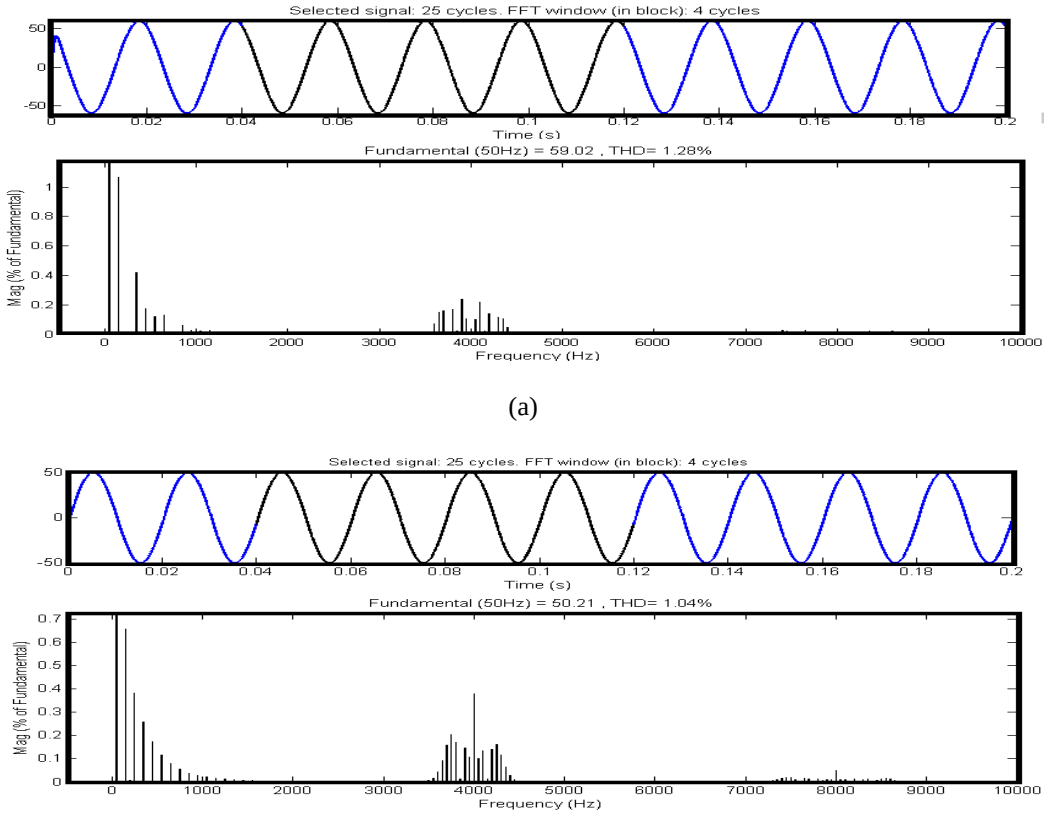
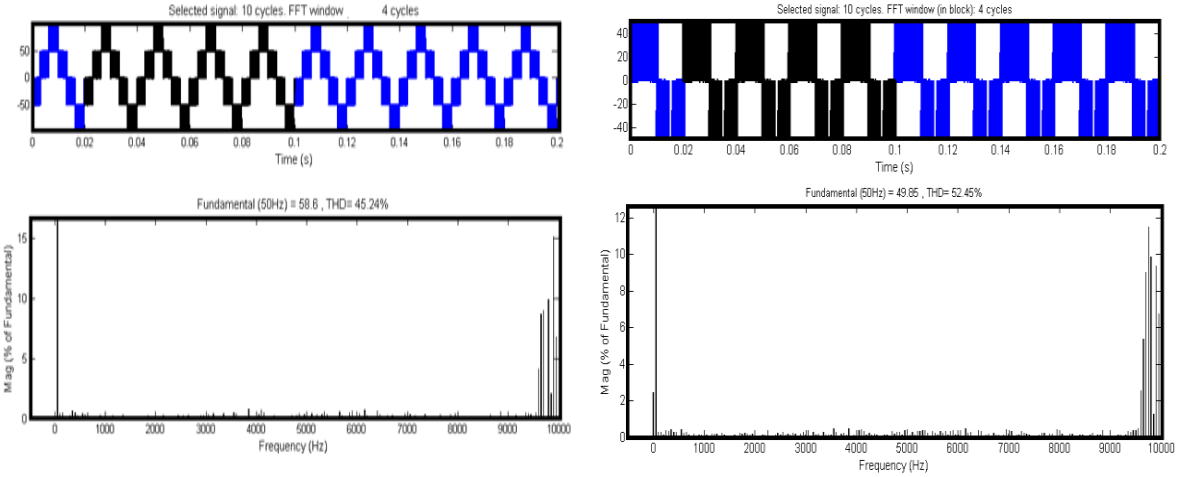


Figure 9. (a) THD of Three Level Filtered Line Voltage of Five Leg DCML Inverter-1.28%, (b) THD of Three Level Filtered Phase Voltage of Five Leg DCML Inverter-1.04%

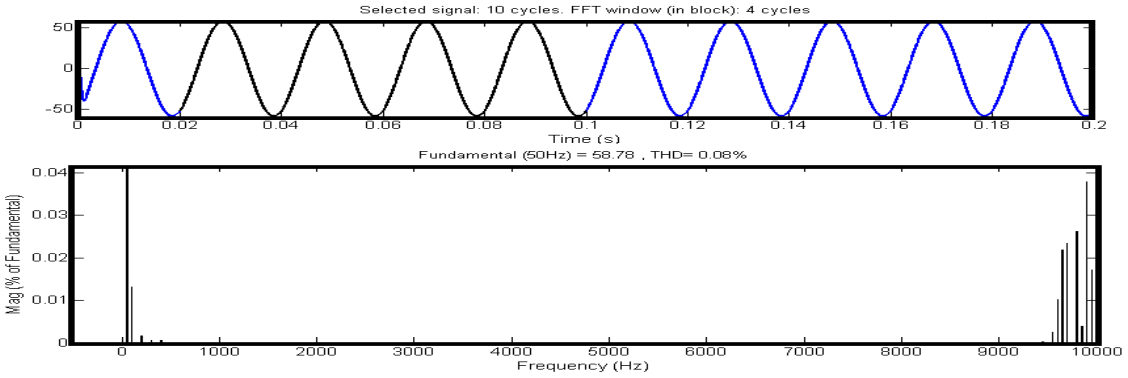
4.5. Three Level Line and Phase Voltages of Five Leg Fly Back Capacitor clamped Multilevel Inverter –Single Leg



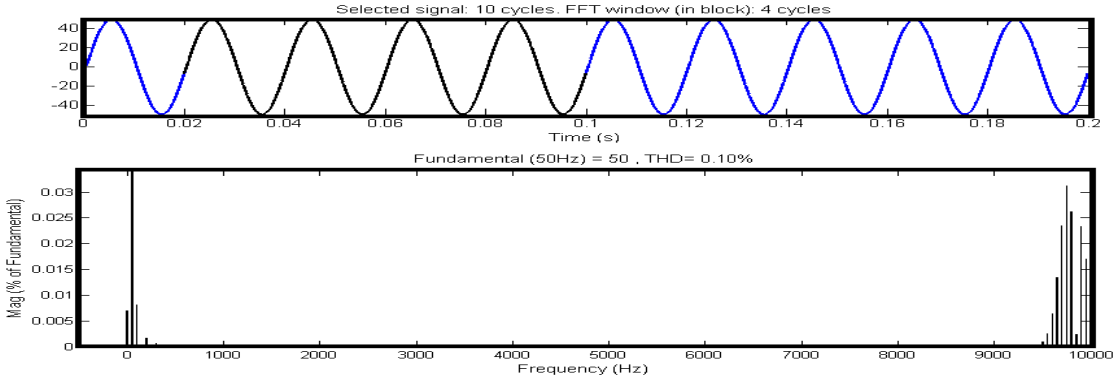
(a) (b)

Figure 10. (a) THD of Three Level Line Voltage of Five Leg FCML Inverter-45.24%**,** (b) THD of Three Level Phase Voltage of Five Leg FCML Inverter-52.45%

4.6. Three Level Line and Phase Voltages of Five Leg Fly Back Capacitor clamped Multilevel Inverter –Single Leg



(a)



(b)

Figure 11. (a) THD of Three Level Filtered LineVoltage of Five Leg FCML Inverter-0.08%, (b) THD of Three Level Filtered Phase Voltage of Five Leg FCML Inverter-0.1%

5. DISCUSSION

The FFT analyses of2-level five phase inverter line-to-line voltage and phase voltage waveform without and with filter are discussed and as shown in Figure 6 and 7. The FFT analyses of3-level five phase Diode clamped multi level inverter, line-to-line voltage and phase voltage waveform without and with filter are shown in Figure 8 and 9. The FFT analyses of3-level five phase Fly back capacitor clamped multi level inverter, line-to-line voltage and phase voltage waveform without and with filter are shown in Figure 10 and 11.The FFT analysis of Five phase 2-level inverter,3-level diode clamped, fly back capacitor clamped multi level inverter are summarized in Table 3.

Table 3. Total Harmonic Distortion of Three Types of Inverters

Types of Inverters	Total Harmonic Distortion			
	Phase Voltage		Line-Line Voltage	
	Without filter	With filter	Without filter	With filter
2 Level Five Phase Inverter	93.66%	14.71%	127.22%	10.68%
3 Level Five Phase DCML Inverter	51.24%	1.04%	44.06%	1.28%
3 Level Five Phase FCML Inverter	52.46%	0.08%	45.24%	0.1%

6. CONCLUSION

This paper provides the relative analysis of five phase 2-level inverter,3-level diode clamped and capacitor clamped inverters. It is observed that the total harmonic distortion produced by the multilevel inverter system is less than that of conventional two level inverters .By using the diodes in diode clamped inverter it diminishes the voltage stress across the power devices. Five phase diode clamp three level inverters have turn into an efficient and practical solution for largest output levels and the low Total Harmonics Distortion percentage. Here, the main advantage of five phase system, it eliminates the 5^{th} harmonics. The performance of conventional two level inverter Diode clamped and Capacitor clamped topologies of 5-phase multilevel inverter (3-level) using sinusoidal pulse width modulation (SPWM) are presented and the simulation results are carried out by FFT analysis and the summarized THD values are shown in Table 3.

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