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The Effect of Different Dielectric Materials in Designing High Performance Metal-Insulator-Metal (MIM) Capacitors

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ABSTRACT

A Metal-Insulator-Metal (MIM) capacitor with high capacitance, high breakdown voltage, and low leakage current is aspired so that the device can be applied in many electronic applications. The most significant factors that affect the MIM capacitor's performance is the design and the dielectric materials used. In this study, MIM capacitors are simulated using different dielectric materials and different number of dielectric layers from two layers up to seven layers. The effect of the different dielectric constants (k) to the performance of the MIM capacitors is also studied, whereas this work investigates the effect of using low-k and high-k dielectric materials. The dielectric materials used in this study with high-k are Al_2O_3 and HfO_2, while the low-k dielectric materials are SiO_2 and Si_3N_4. The results demonstrate that the dielectric materials with high-k produce the highest capacitance. Results also show that metal-Al_2O_3 interfaces increase the performance of the MIM capacitors. By increasing the number of dielectric layers to seven stacks, the capacitance and breakdown voltage reach its highest value at 0.39 nF and 240 V, respectively.

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1. INTRODUCTION

Metal-insulator-metal (MIM) capacitors are widely used in many electronic applications. One of the application is for high voltage, low current power supply module, whereas, for this device application, MIM capacitors are required to exhibit agreeable electrical properties such as high capacitance density, sufficient resistance to dielectric breakdown which lead to high breakdown voltage, voltage linearity characteristics and low leakage current. By the year 2018, according to the International Technology Roadmap Semiconductor (ITRS) recommendations, higher capacitance density of > $5fF/\mu m^2$ and lower leakage current density of < $10nA/cm^2$ have to be achieved [1].

A standard MIM capacitor consists of two or more dielectric materials sandwiched between electrode and silicon substrate. Silicon dioxide and silicon nitride are dielectric materials commonly used in conventional MIM capacitors [2]-[7]. Although the dielectric can provide excellent voltage linearity properties and low-temperature coefficients, their capacitance density will be limited due to low dielectric constants (3.9 for SiO_2 and 7.5 for Si_3N_4). With the advancement in process integration and size scaling, MIM capacitor having a higher capacitance, breakdown voltage and lower leakage current can be produced. Therefore, adopting high-k dielectric materials is highly suitable to enable the MIM capacitor to achieve optimal performance. It has always been an issue for dielectric material regarding its leakage current and ability to handle high voltage. In order to develop advanced MIM capacitor, the use of a high-k material is a better solution.

Several of high-*k* dielectric materials have been proposed to be included in the MIM capacitors to increase the capacitance and reduce the leakage current [8]-[12]. The first factor to achieve the high capacitance is by using high-*k* dielectric materials, such as Al_2O_3 and HfO_2 which are widely used due to their high capacitance density, good thermal stability and high energy bandgap [13]-[17]. The second factor is when two or more dielectric materials are stacked or sandwiched, which lead to higher trapping probability [18]-[22]. This is due to the charge accumulation at the interface between the dielectrics as a result of differing conductivities [23].

In this paper, the study on multilayer dielectrics is performed based on dielectric layers/stacks with a low-*k*/low-*k* and high-*k*/high-*k* combinations for high voltage applications. In this study, the dielectric stacking is arranged started with two stacks up to seven stacks. The dielectric materials used in this work are SiO_2 and Si_3N_4 for low-*k* dielectric stacking and Al_2O_3 and HfO_2 for high-*k* dielectric stacking. The dielectric stacks are arranged with increasing number of layers in order to increase the device capacitance. The simulations are stopped at seven dielectric stacks due to the saturation in the capacitance value, which will be discussed in section 4.

2. SIMULATION METHODS

Sentaurus Device Editor or also known as SDE is used as a device structure editor. The software can simulate two-dimensional (2D) or three-dimensional (3D) process emulator to design electronic devices [24]. The device simulator, SDEVICE is used to perform tests and electrical characterization. This work applied drift-diffusion model with doping dependent mobility, doping dependent Shockly-Read-Hall (SRH) Auger and surface recombination for carrier transport and recombination. For the characterization, the applied bias is swept between 0 V to 300 V and a constant AC frequency of 1 MHz is applied to the capacitor.

3. SIMULATION OF THE DEVICE STRUCTURE

The MIM capacitor structure simulated in this work consists of aluminum (Al) as the metal contact and two different dielectric materials on a p-type silicon. Four different MIM capacitor designs are built using a different arrangement of dielectric stacks. The design of the four MIM capacitors is shown in Figure 1, which illustrates two, three, five and seven stacks of different dielectric layers. The dielectric materials used in this study with their dielectric constants and energy band gaps are listed in Table 1.

In this work, SiO_2 and Si_3N_4 layers are stacked in different arrangements as shown in arrangement 1 and 2 in Table 2. To compare the effect of different dielectric constants, Al_2O_3 and HfO_2 are used to replace the SiO_2 and Si_3N_4 layers and arranged in the same ways, as represented in arrangement 3 and 4 in Table 2.

The simulation is initially formed by building a 400 nm thick p-type silicon substrate doped with boron at a concentration of 5×10^{17} atoms/cm^3. The dielectric layers are then deposited on the substrate based on the arrangement shown in Table 2 at 100 nm thickness for each layer. The MIM capacitor is finally completed by depositing 30 nm metal layer on the top.

The two, three, five and seven stacks of dielectric materials are significantly observed in this work. However, it is found that the four and six dielectric stacks produced different stacking arrangement, where the interface between the top dielectric and metal produces very small charges which lead to low breakdown voltage [23],[26]. Hence this four and six dielectric stacks are not suitable for high voltage application, and both arrangements are disregarded.

Table 1. Dielectric constants and energy band gaps of the dielectric materials

Dielectric material	Dielectric Constant (*k*)	Energy Bandgap (eV)
SiO_2 (O)	3.9	8.9
Si_3N_4 (N)	7.5	5
Al_2O_3 (A)	8.5	6.2
HfO_2 (H)	22	5.9

Table 2. The arrangement of dielectric layers/stacks in the MIM capacitor.

Arrangement	2 stack	3 stack	5 stack	7 stack
1	ON	ONO	ONONO	ONONONO
2	NO	NON	NONON	NONONON
3	AH	AHA	AHAHA	AHAHAHA
4	HA	HAH	HAHAH	HAHAHAH

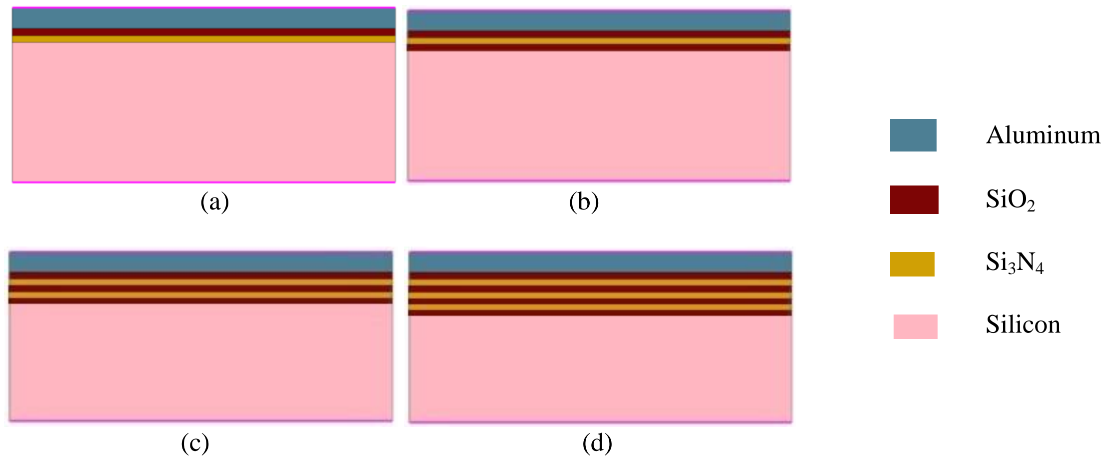

Figure 1. MIM capacitors with (a) two, (b) three, (c) five and (d) seven layers of dielectric materials

4. DEVICE CHARACTERIZATION AND PERFORMANCE

4.1. Capacitance-Voltage (*C-V*) Characteristics

Capacitance-Voltage (*C-V*) measurement is performed to analyze the impact of voltage on capacitance. Figure 2 (a) shows the *C-V* measurement for all four (two, three, five and seven dielectric stacks) simulated MIM capacitors. It is indicated that the MIM capacitor with a combination of AH obtained the highest capacitance value of 0.1377 nF, which is greater than other capacitance obtained from HA, ON, and NO at 0.089 nF, 0.032 nF, and 0.026 nF, respectively.

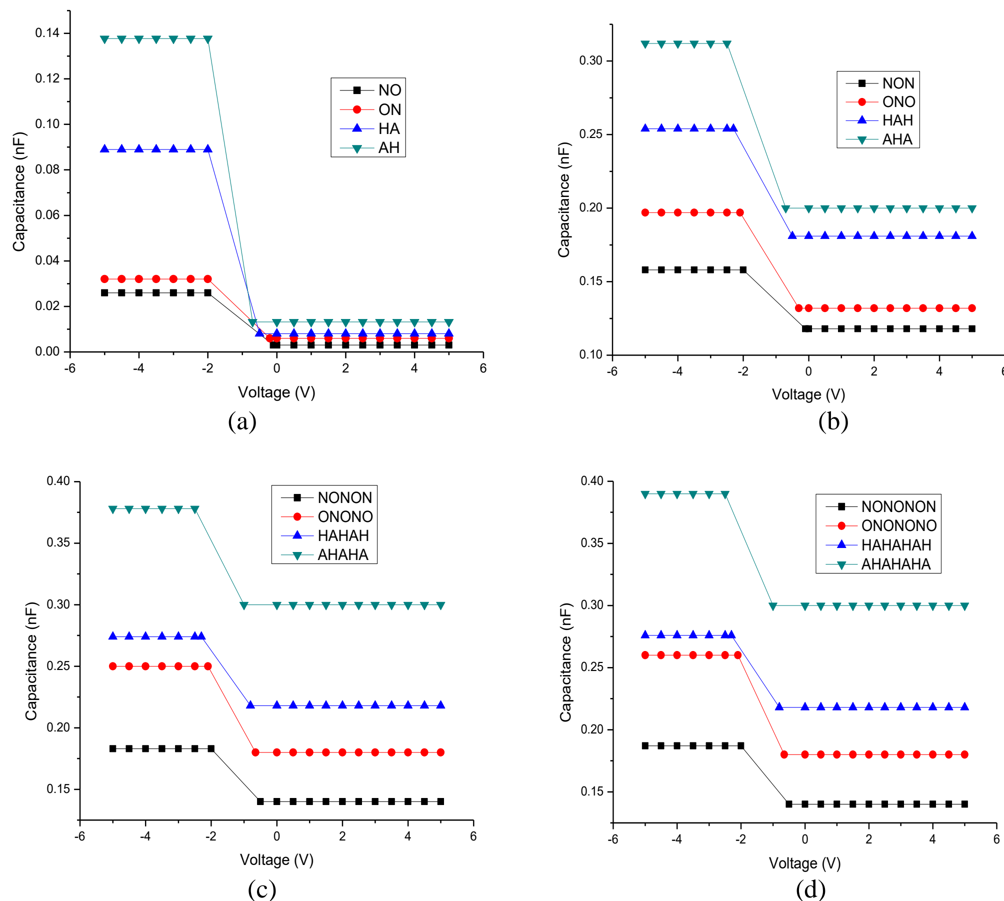

Figure 2. *C-V* measurement for (a) two, (b) three, (c) five and (d) seven stacked of MIM capacitors.

It is suggested that the difference in the capacitance values are due to the different dielectric constants. As AH has higher dielectric constant, it produces higher capacitance compared to ON and NO arrangement. However, the capacitance value is higher for AH compared to HA. This is caused by the higher amount of charges in AH due to the interfaces between metal-dielectric (Al-Al_2O_3) with high dielectric constant [23].

Figure 2 (b) shows the *C-V* measurement of three dielectric layers where the highest capacitance obtained from the AHA arrangement is 0.312 nF. The capacitance obtained from the other designs are 0.254 nF for HAH, 0.197 nF for ONO and 0.158 nF for NON. It is obvious that the combination of O and N will produce lower capacitance, which is caused by the lower dielectric constants. This result is in agreement with the results obtained from Figure 2 (a). The result also shows that the AHA arrangement produces higher capacitance compared to HAH. As mentioned earlier, this occurs due to a number of charges that are introduced at the metal-dielectric interface, where Al-AHA interaction produces a higher amount of charges compared to Al-HAH [23].

Figure 2 (c) shows the capacitance for five dielectric layers which demonstrates that the AHAHA arrangement produces the highest capacitance. Based on the seven dielectric layers shown in Figure 2(d), the highest capacitance is obtained from the AHAHAHA arrangement. Therefore the interaction of charges introduced at the Al-A interface significantly affects the total capacitance for all two, three, five and seven dielectric layers in MIM capacitor.

Figure 3 summarizes the capacitance values obtained from Figure 2. As mentioned earlier, it is clear that the four different dielectric layers/stacks arranged as AH, AHA, AHAHA and AHAHAHA produced higher capacitance because the dielectric materials consist of high dielectric constants combination and charges. The AHAHAHA (seven dielectric layers) generated the highest capacitance due to the high number of dielectric layers which give rise to higher charges trapped between the interfaces of dielectric layers. However, it is found that more than seven dielectric layers caused no significant increment in the capacitance and the values are saturated. The Al_2O_3 (A) that is placed in contact with the top metal, not only increase the number of charges but also has the ability to sustain higher voltage reliability than HfO_2 [25].

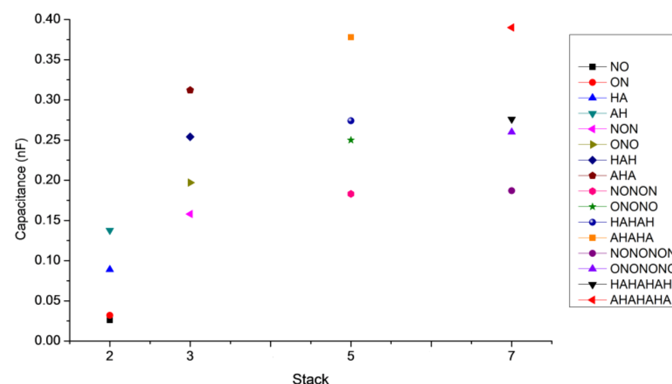

Figure 3. Capacitance for two, three, five and seven dielectric stacks

4.2. Current-Voltage (I-V) Characteristics

Figure 4 (a) shows the I-V characteristics for MIM capacitors with two stacks. It is indicated that the AH arrangement obtained the highest breakdown voltage of 98 V, which is greater than other breakdown voltages obtained from HA, ON, and NO at 80 V, 76 V, and 58 V respectively. This may be suggested by the difference in the dielectric constants and energy bandgaps [13]-[14]. As discussed previously, since it is in contact with the top metal and it has higher dielectric constant and energy bandgap than HfO_2, which cause the high breakdown voltage. The AH arrangement also causes the device to be able to sustain higher voltage stress compared to HA, ON and NO arrangements [25].

Figure 4 (b) shows the I-V characteristics of three dielectric stacks. It is observed that the highest breakdown voltage of 182 V is obtained from the AHA arrangement. The breakdown voltages obtained from other arrangements are 148 V for HAH, 135 V for ONO and 118 V for NON. With additional dielectric layer (3 layers), the arrangement of Al_2O_3 (A) in contact with the top metal produced the highest breakdown voltage and this result is in agreement with the result obtained from Figure 4 (a). It is also obtained that this arrangement produces higher breakdown voltage compared to HAH.

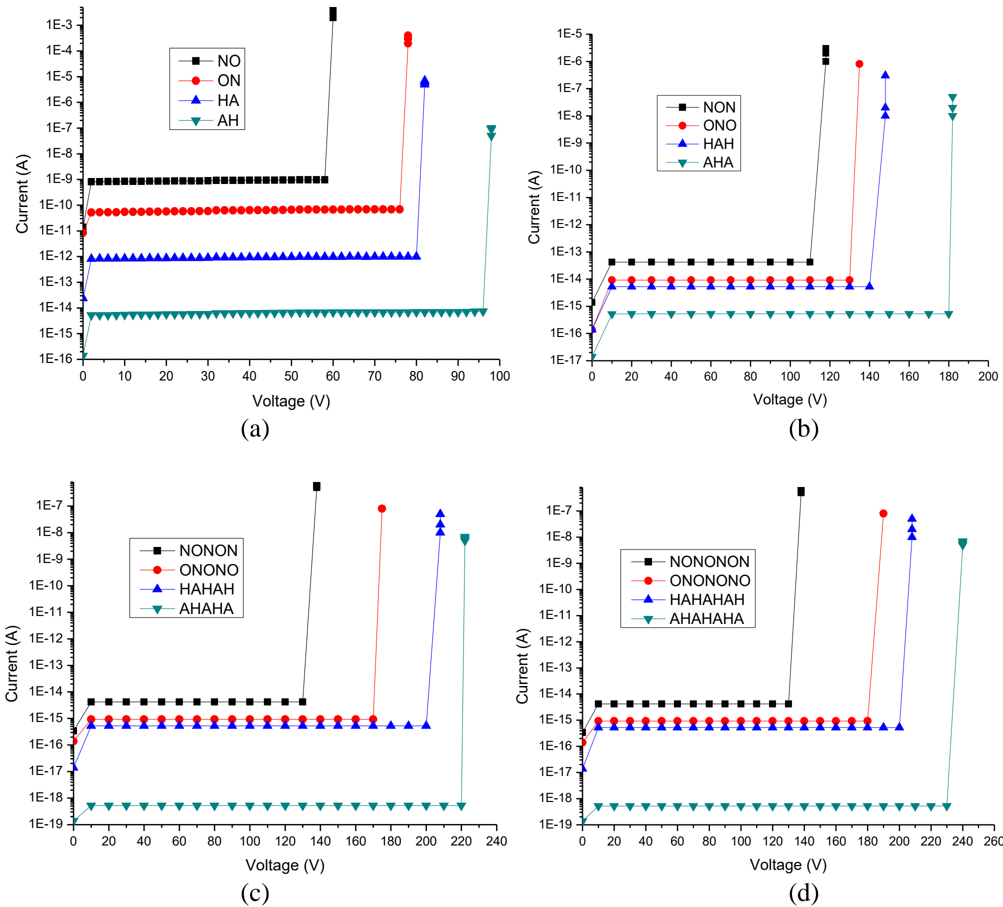

Figure 4. I-V curves for (a) two, (b) three, (c) five and (d) seven stacked of MIM capacitor

Figure 4 (c) shows breakdown voltages for five dielectric stacks, which demonstrate that the AHAHA arrangement produces the highest breakdown voltage. From the seven dielectric stacks in Figure 4(d), the highest breakdown voltage is obtained from the AHAHAHA arrangement. It is suggested that the amount of charges introduced at the Al-A interface significantly affects the total voltage stress given to all two, three, five and seven stacks of dielectric materials.

Figure 5 summarizes the breakdown voltages obtained from Figure 4. As mentioned earlier, high breakdown voltages only obtained from the dielectric combination between A and H, in which all the four arrangements (two, three, five and seven stacks) produce higher breakdown voltages than dielectric combination of O and N. Two significant factors that suggest this are the higher energy band gaps and dielectric constants [25] of both dielectrics A and H, as shown in Table 1.

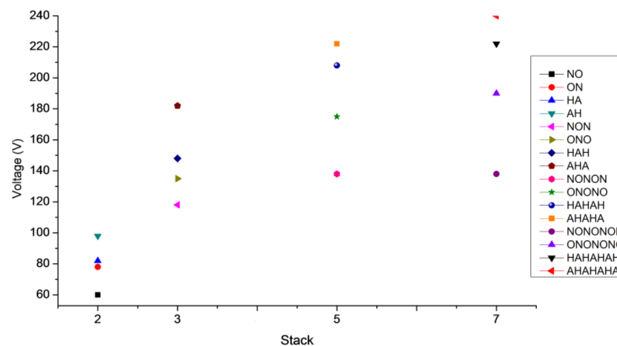

Figure 5. Breakdown voltages for two, three, five and seven dielectric stacks

Figure 5 also compares the breakdown voltages when the dielectric stacks are increased from two to seven. It is obtained that, the best dielectric materials to be on the top are SiO_2 (low-*k*) or Al_2O_3 (high-*k*). Previous studies have proven that SiO_2 or Al_2O_3 which are higher in energy band gaps than Si_3N_4 (low-*k*) and HfO_2 (high-*k*), allow the devices to operate at much higher voltages, frequencies, and temperatures [5],[6],[23],[26]. Hence this strengthens the analysis where the Al_2O_3 and HfO_2 lead to higher breakdown voltages than SiO_2 and Si_3N_4 at equivalent capacitance, as well as better resistance to electrical stress.

5. CONCLUSION

In this work, MIM capacitor using four different types of dielectric have been successfully designed and simulated using Synopsys Sentaurus TCAD tools. The results have demonstrated that higher capacitance can be achieved by using high-*k* dielectric. It has also found that a much greater capacitance value can be obtained with a suitable number of dielectric stacks, whereas this study has obtained that seven dielectric stacks produced the highest capacitance and breakdown voltage. It is also can be concluded that metal-dielectric (dielectric with high-k and high energy band gap) produced a high amount of charges, hence this lead to high capacitance value, high breakdown voltage and also better resistance against electrical stress. As in this study, it is found that Al_2O_3 (A) in contact with the top metal produced the highest capacitance and breakdown voltage.

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