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On the DIBL Reduction Effect of Short Channel Carbon Nanotube Field Effect Transistors

Khial Aicha[1], Rechem Djamil[2], Azizi Chrifa[3], Zaabat Mourad[4]
Laboratory of Active Components and Materials, University Larbi Ben M'hidiOum El Bouaghi
Oum El Bouaghi, Algeria
[1,3,4]Faculty of Exact Sciences and Natural and Life Sciences, University Larbi Ben M'hidi, Oum El Bouaghi, Algeria
[2]Department of Science and Technology, Faculty of Science and Technology, University Larbi Ben M'hidi,
Oum El Bouaghi, Algeria

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ABSTRACT

The Drain Induced Barrier Lowering (DIBL), in carbon Nanotubes-Fet (CNTFETS), is a challenging study that still needs investigation. Based on a numerical model, the Non-Equilibrium Green's Function (NEGF) approach was applied to simulate the DIBL effect in CNTFETS. In this study, the effect of theeength ction...o simulate the DIBL effect in carbon Nanotubes-Fet (CNTFETS), length gate ranging from 10 to 30 nm, for different temperatures (77K, 15K, 300K and 400K) on the DIBL was investigated. Then the variation of DIBL effect as a function of the nanotubes diameter varying over the following chiralities: (13, 0), (16, 0), (19, 0), (23, 0) and (25, 0) was undertaken. Afterworlds, we conducted the variation of DIBL impact as a function of the oxide thickness with the values: 1.5 nm, 3 nm, 4.5 nm, 6 nm and 7 nm. Moreover, the DIBL effect was carried at depending upon the high-k materials such as: SiO_2, HfO_2, ZrO_2, Ta_2O_2 and TiO_2. Finally, a conclusion is made basing at the different findings which revealed that the best reduce of DIBL impact was recorded under a liquid Nitrogen temperature of 77 K.

Corresponding Author:

Rechem Djamil,
Department of Science and Technology, Faculty of Science and Technology,
University Larbi Ben M'hidi,
Oum El Bouaghi, Algeria.
Email: rechem_dj@yahoo.fr

1. INTRODUCTION

Few years ago, considerable interest has been given to field-effect transistors (FETs) based on semiconducting carbon nanotubes (CN), due to their superior electronic properties. FETs have recently reached a higher performance [1]-[3]. The progress in engineering CNTFETs is due generally to their excellent DC characteristics [4]-[6]. This is because of their small diameter (~1nm), for single-walled carbon nanotubes, which consist of a single layer of graphene sheet wrapped up to form a seamless tube [7], possessing exceptional electrical properties, such as high current carrying capability [8] and excellent carrier mobility [9]. Both theory and experiments have demonstrated that these tubes can be either metallic or semiconductor, depending on the chirality of their atomic structure with respect to the tube axis.

For a long channel device, the barrier height depends principally of the gate voltage, where V_{DS} has no effect. In this case of the nano-scalle field-effect transistors, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. These conditions allowed the potential barrier between the source and the channel to prevent electrons from flowing to the drain. The barrier height decreases when a high drain voltage is applied. Hence, there is a further decrease of the threshold voltage. In

this case the source injects carriers into the channel surface and the gate does not play any role. This is known as drain induced barrier lowering (DIBL).

The DIBL can also be found in two dimensions devices of such as CNTFETs. However, because of CNTFETs structural and electrostatic properties, the DIBL effect in CNTFET has a new characteristic on the device performance, and it's rooting [10].

Some interesting work on the DIBL effect has been noticed, for example in reference [11], Fiori. G develops a numerical model based on NEGF, and shows that DIBL effect in short-channel CNTFETs can be reduced by a double-gate, triple-gate, or surround-gate device structure. In reference [12], the DIBL effect is observed in CNTFET manufactured on a silicon wafer by R. Thomas Weitz, and the observational $\frac{\Delta V_{TH}}{\Delta V_{DS}} = 700\ mV/V$. In reference [13] Though Fillo et al, pointed out the DIBL effect on C_{GD}. All these works did not explain the DIBL effect deeply.

Our work is based on a numerical simulation developed with non-equilibrium Green's function (NEGF) approach. We study the DIBL effect in CNTFET and its dependence on the gate length, the variation effect of Nanotubes diameter, oxide thickness and the source/drain doped.

Silicon dioxide (SiO_2) has facing the scaling limitation due to direct tunneling current that limits low power application and reliability. Recently, many high-k materials such as HfO2 (k=16), ZrO2 (k=25), Ta2O5(k=50), and TiO2 (k=35-100) [14],[15] have been introduced as alternative gate dielectrics to overcome leakage current problem. To consider the benefits of high-k gate dielectrics and CNTFETs, in this paper we present also the effects of high-k gate dielectric on the variation of DIBL. All these numerical studies have been done at wide range of temperature varying from 77 K to 400 K.

2. CNTFET STRUCTURE

A schematic cross-sectional is shown in Figure 1(a) and 1(b). The source/drain length is 20 nm with heavily doped which is 10^9 nm^{-1} (~0.01dopant/atom) and the channel is assumed intrinsic.

We study the variation of drain induced barrier lowering (DIBL) when technological parameters are varying. Such as Gate lengths, Nanotube diameters, Gate oxide thicknesses, high-k Gate dielectric constants and the source /drain doped.

The Gate lengths (Lg) of the CNTs used are 10nm, 15nm, 20nm, 25nm and 30nm. The chiralities used are (13,0), (16,0), (19,0), (23,0) and (25,0). The Gate oxide thicknesses (tox) used are 1.5nm, 3nm, 4.5nm, 6nm and 7nm. In addition the Gate dielectric constants are 3.9, 16, 25, 50 and 80. These dielectric constants correspond to the dielectric constants for SiO2, HfO2, ZrO2, Ta2O5, and TiO2 respectively. And the source/drain doping used are 2.5 m^{-1}, 4 m^{-1}, 6 m^{-1}, 8 m^{-1} and 10 m^{-1} (~0.01 dopant/atom).

For our simulations, we assume that the metal–Nanotubes contact resistance, RC=0, and carrier transport through Nanotubes is ballistic (no scattering). No gate-to-source or gate-to-drain overlap is assumed. The applied drain V_{DS} and gate V_{GS} biases vary from 0 V to 1 V. All calculations have been done at temperature ranging from 400 K down to 77 K..

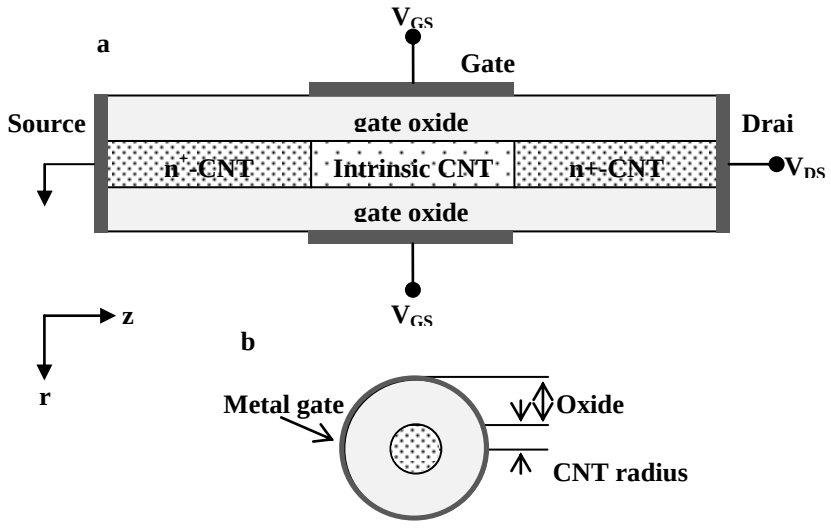

Figure 1. Symmetrical CNTFET considered in this work

3. SIMULATED DEVICE

In order to simulate the proposed devices, self consistent solution of the Poisson and Schrödinger equations has been performed within the NEGF formalism with a mode space approach presented in Ref. [15],[16]. The NEGF method represents an ideal approach for nanoscale device simulations. In this approach, a nanoscale device is conceptually characterized by an active region connected to two large, in-equilibrium electron reservoirs (source and drain). Current flows as a result of an applied external bias between the source and drain which drives the system into a non-equilibrium state. Given the system Hamiltonian, the self-energy functions and the contact electrochemical potentials, the NEGF approach is used to calculate the density matrix from which all other quantities of interest such as current are obtained [17].

The Poisson equation gives the electrostatic potential needed for calculating the Hamiltonian of the CNT. By solving the Schrödinger equation within the NEGF method, the density of states and the charge on the surface of the CNT is obtained. The new electrostatic potential is obtained through the use of the calculated charge and the solving of the Poisson equation using a 2-D finite difference method. The iteration between the Poisson and the Schrödinger equations continues until the self-consistency is achieved. Note that, ballistic transport was assumed.

It is convenient to solve Poisson's equations in cylindrical coordinates. Since the potential and charge are invariant around the nanotube, the Poisson equation is essentially a 2-D problem along the tube (z-direction) and the radial direction (r-direction) as Poisson equation is written as [18], [19]:

$$\nabla^2 V(r,z) = \frac{-q}{\varepsilon}[p - n + N_D^+ - N_A^- + n_T] \quad (1)$$

Where $V(r,z)$the electrostatic potential, q is is the magnitude of the electronic charge, ε is the dielectric constant, p and n are the hole and electron densities, respectively, N_D^+ is the concentration of ionized donors, N_A^- is the concentration of ionized acceptors, and n_T is the fixed charge. The fixed charge is an input to the model, and will be set to zero. The electron and hole concentrations (n and p, respectively) are computed by solving the Schrödinger equation with open boundary conditions by means of the NEGF formalism.

To calculate the Green's function for the device at a specific energy E, the following formula has been utilized [20]:

$$G(E) = [EI - H - \Sigma_S - \Sigma_D]^{-1} \quad (2)$$

Where 'I' is the identity matrix and 'H' is the Hamiltonian of the CNT, Σ_S and Σ_D are the self-energies for source and drain contacts, respectively.

The electron density is computed from the density of states (DOS), derived by the NEGF formalism. It can be calculated as follows:

$$n = \int_{Ei}^{+\infty}[D_S f(E - E_{FS}) + D_D f(E - E_{FD})]dE \quad (3)$$

Where Ei is the Fermi level within the CNT, f(E) is the Fermi-Dirac distribution, and $D_S(D_D)$, E_{FS} (E_{FD}) are the density of states and the Fermi energies of the source (drain), respectively. A similar expression applies for holes.

Once, self consistency is obtained, the source-drain current can be expressed as

$$I = \frac{4q}{h}\int T(E)[f(E - E_{FS}) - f(E - E_{FD})]dE \quad (4)$$

Where h is Planck's constant and T(E) is the transmission coefficient calculated by the NEGF formalism [20].

4. SIMULATED RESULTS

To check the accuracy of our numerical calculations, the drain currentIds vs. V gs was calculated using the non-equilibrium Green's function (NEGF) formalism (solidlines) and compared with simulated results presented in [21] (dotted lines). Good agreement has been found in Figure 2.

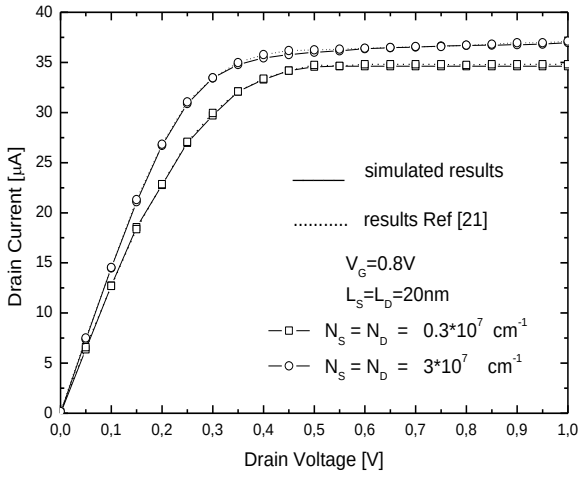

Figure 2. Comparison of the output characteristics between our model

In this section we present our numerical results on DIBL.

The DIBL is accessed using the classical formula for low V_{Ds} =50mV and high V_{Ds} =1V drain bias.

$$\text{DIBL} = \frac{V_{TH}(\text{Low VDS}) - V_{TH}(\text{High VDS})}{\text{High VDS} - \text{Low VDS}} \quad (5)$$

Simulated drain current I_{DS}characteristics for different gate voltage V_{GS} and different temperatures of CNTFET are traced in Figure 3.

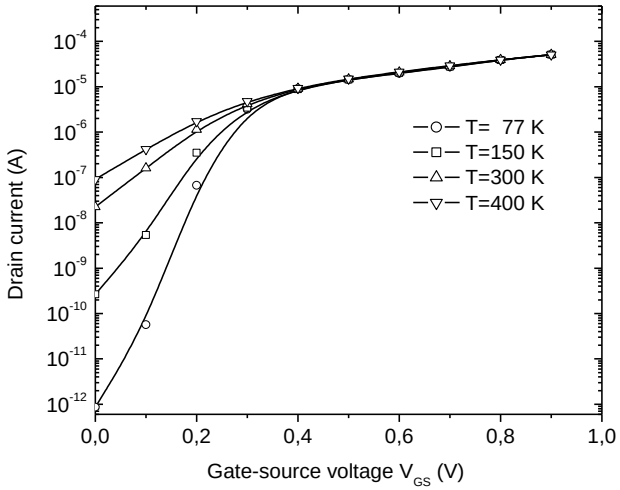

Figure 3. Tranconductance characteristics for different temperature.

This shows that the effect of temperature is more significant in lower gate-source voltage.We observe for this figure that when the temperature decreases the leakage current decreases also, so we get a CNTFET with better performance at lower temperature.It can be seen that the augmentation of the temperature results in shifting the characteristics to the left and it is clear that as the temperature gets over 150 K, the subthreshold current rises dramatically.The switching speed is more for low temperature i.e. as the temperature decreases the CNTFET becomes faster.

Figure 4 Presents the DIBL as a function of the gate length taken from 10 to 30nm for different temperature. For T=150 K, T=300 K, T=400 K the DIBL decreases with a nearly linear low when the gate length increases. We note a reduction around 54.64 % in DIBL. We note considerable reduction of DIBL when the temperature changes from 400 K to 77 K.For T=77 K (temperature liquid nitrogen) we observe that the DIBL is remain constant whatever the gate length is. In this case we obtained a small value of DIBL (around 20 mV/V).

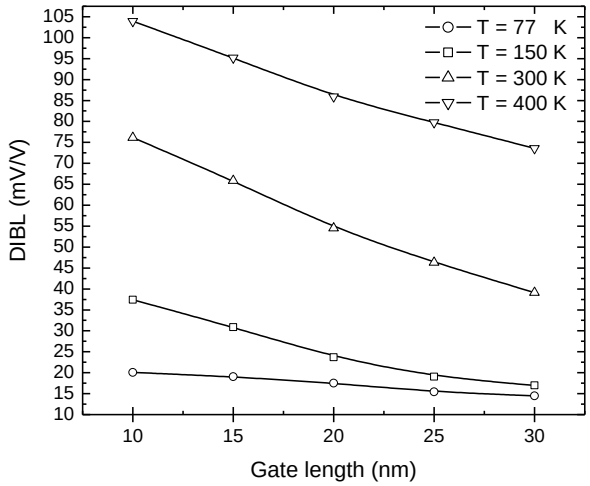

Figure 4. Drain induced barrier lowering (DBIL) versus gate length at different temperature.

In the Figure 5, we show the variation of DIBL against the Nanotubes diameter for different temperature varying from 77 K to 400 K.We observe an important reduction (around: 65.17%) in DIBL when the Nanotubes diameter decreases. Also it can be drawn that with the temperature decreasing from 400 K to 77 K, the DIBL decreases.The component present a good performance (DIBL) when we choose a low Nanotubes diameter and at low work temperature.These lead to that the effect of V_{Ds} on the potential barrier is small.

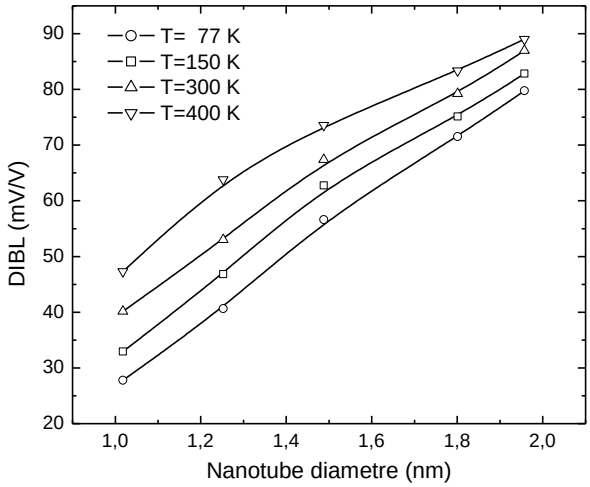

Figure 5. Drain induced barrier lowering (DBIL) versus the Nanotubes diameter at different temperature

The DIBL is calculated as a function of gate oxide thickness tox, this is illustrated in Figure 6. As we can see from the figure, when the tox decreases the DIBL decreases also.We note that when tox changes from 7 nm down to 1.5 nm an important reduction in DIBL around 67.20 % can be obtained.Furthermore the

DIBL is calculated as a function of temperature this is plotted in the same figure.The DIBL improve when the CNTFET work in low temperature significant reduction in DIBL about 59.49 % is found when the temperature changes from 400 K down to 77 K.

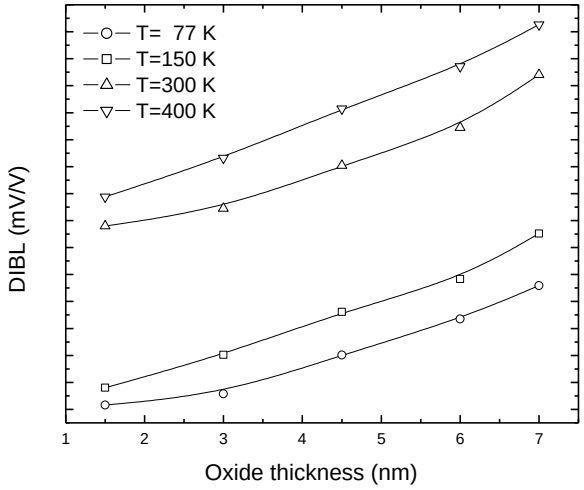

Figure 6.The DIBL variations with the gate oxide thickness at different temperatures.

In this section, to highlight our analyses we varying the gate dielectric permittivity from 3.9 to 80. As shown in Figure 7, it can be drawn that the DIBL is considerable improved when increasing K.At room temperature, one notes a reduction around 88.89 % of DIBL when K varies from 3.9 to 80. It can be observed that the lows the temperature is, the better the DIBL will be at all gate dielectric permittivity.It is worthily to mention when we varying the T that the large difference (around 50 %) is obtained when we use $S_iO_2$as gate dielectric.

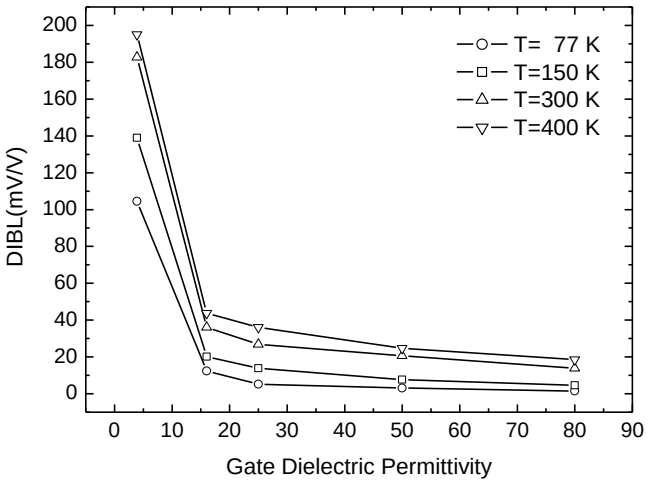

Figure 7. The DIBL variations with the gate dielectric permittivity at different temperatures.

Figure 8 presents the DIBL variation with the channel doping at different temperatures varying from 77 K to 400 K. From figure 8 we observed that when the channel doping decreasing, the DIBL decreases also and follow nearly a linear low.We not a reduction around 52.95 %in DIBL when reduce the channel doping from $10^9 \mathrm{nm}^{-1}$ to$2.5\ 10^8 \mathrm{nm}^{-1}$.In the same figure we plot also the variation of the DIBL against the influence of the temperature.Decreasing in the temperature results in decreasing in the DIBL the low value is obtained at 77 K.From our simulation, changing in the channel doping the DIBL can be obtained but with the

doping varying from 2.5 $10^8 nm^{-1}$ to 4 $10^8 nm^{-1}$ at 300 K and 400 K we can not calculate the DIBL because the program diverges.

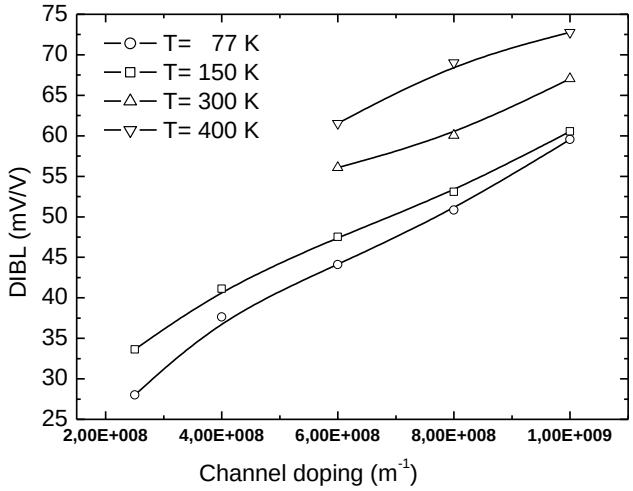

Figure 8. The DIBL variations with the channel doping at different temperatures.

5. CONCLUSION

In our work we have studied the DIBL effect on the performance of nanoscale CNTFET, using the non-equilibirium Green's function (NEGF) formalism. Among key transistor parameters; gate length, nanotubes diameter, oxide thickness, gate dielectric permittivity and channel doping, It is found that the DIBL effect decreases with decreasing oxide thickness, nanotubes diameter and channel doping, also we have found the DIBL effect reduces when the temperature varying from 400K down to 77K. In addition, as the gate length and gate dielectric permittivity increase the DIBL effect decreases.

REFERENCES

[1] A. Javey, *et al*., "High perfoeance n-type carbon nanotube field-effect transistor with chemically doped contacts," *Nano Lett*., vol. 5, pp. 345, 2005.
[2] A. L. Louarn, *et al.*, "Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube field-effct transistor," *Appl. Phys. Lett.*, vol. 90, pp. 233108, 2007.
[3] M. Rahmani, *et al.*, "Trilayer Graphene Nanoribbon Field Effect Transistor Analytical Model," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 12(4), pp. 2530-2535, 2014.
[4] S. M. Z. Iqbal, *et al*., "Fabrication of CNT NanoStrands as a Schottky Transistor Platform," *International Journal of Nano Devices, Sensors and Systems (IJ-Nano)*, vol/issue: 2(2), 2013.
[5] A. Javey, *et al*., "High dielectrics for advanced carbon-nanotube transistor and logic gates," *Nat. Mater*., vol/issue: 1(4), pp. 241-246, 2002.
[6] S. J. Wind, *et al*., "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett*., vol/issue: 80(20), pp. 3817-3819, 2002.
[7] M. S. Dresselhaus, *et al*., "Carbon Nanotubes: Synthesis, Structure, Properties, and Applications," *Berlin, Germany: Springer-Verlag*, 2001.
[8] Z. Yao, *et al*., "High-field electrical transport in single-wall carbon nanotubes," *Phys. Rev. Lett*., vol. 84, pp. 2941–2944, 2000.
[9] M. S. Fuhrer, *et al*., "High-mobility nanotube transistor memory," *Nano. Lett*., vol 2, pp. 755–759, 2002.
[10] H. Zhou, *et al*., "Numerical Study of DIBL effect in Carbon Nanotube-FETs," *IEEE NANO Organizers*, vol. 752, 2009
[11] R. T. Weitz, "Highly Reliable Carbon Nanotube Transistors with Patterned Gates and Molecular Gate Dielectric," *Nano Letter*, 2000.
[12] G. Fiori, *et al*., "A Threen-Dimensional Simulation Study of the Performancd of Carbon Nanotunbe Field-Effect Transistors with Doped Reservoirs and Realistic Geometry," *IEEE Trans. Electron Devices*, vol. 53, 2006.
[13] http:// www.itrs.net/links/2010itrs.
[14] J. H. Lee, *et al*., "Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-AL2O3 gate dielectric," *In. IEDM. Tech. Dig*., pp. 645-648, 2008.

[15] J. Guo, *et al*., "Towards multiscale modeling of carbon nanotube transistor," *Int. J. Mult. Comp. Eng*., vol. 2, pp. 257-276, 2004.
[16] S. O. Koswatta, *et al*., "Towards Multiscale Modeling of Carbon Nanotube Transistors," *IEEE IEDM Tech. Digest*, pp. 518, 2005.
[17] S. Datta, "Nanoscale device modeling: the Green's function method," *Superlatt Microstruct.*, vol. 28, pp. 253, 2000.
[18] A. Svizhenko, *et al*., "Two-dimensional quantum mechanical modeling of nanotransistors," *J. Appl. Phys*., vol/issue: 91(4), pp. 2343–2355, 2001.
[19] J. Clifford, *et al*., "Electrostatics of partially gated carbon nanotube FETs," *IEEE Transactions on Nanotechnology*, vol/issue: 3(2), pp. 281–286. 2004.
[20] J. Guo, *et al*., "Atomistic simulation of carbon nanotube field-effect transistors using non-equilibrium Green's function formalism," *J. Comput. Elect.*, vol/issue: 3(3–4), pp. 373–7, 2005.
[21] A. A. Orouji, *et al*., "Novel attributes and design considerations of source and drain regions in carbon nanotube transistors," *J. Physica E*, vol. 42, pp.1456-1462, 2010.

BIOGRAPHIES OF AUTHORS

KHIAL AICHA was born in Oum El Bouaghi, Algeria on 1987. She received the License physic degree from University of Oum El Bouaghi, Algeria. Master's degree in the physics of semiconductors and electromagnetic compatibility. She is research interests include MOSFETs and Carbone Nanotube Field Effect Transistors (CNTFETs).

RECHEM DJAMIL was born in Constantine, Algeria on 1972. He received the graduate electronic engineering, Master's degree in electronics components and graduation of doctorate in electronic degrees from the institute of electronics at Constantine University, Algeria. He is presently a teacher in the department of science and technology, Faculty of science and technology, university Larbi Ben M'hidi, Oum El Bouaghi, Algeria. His research interests focus on the modeling of nanoscale and quantum-effecttransistors MOSFETs, Double gate MOSFETs, Carbone Nanotube Field Effect Transistors (CNTFETs) and synthesis and fabrication of nanostructures such as chemical/gas sensors.

CHERIFA AZIZI was born in Sigus, Oum El Bouaghi, Algeria, on 1951. She received the License en-science degree in physic from University of Constantine, Algeria in 1973, and the Magister and Doctorate degrees in solid-stat physics Paul Sabatier University, Toulouse, France in 1976 and 1981, respectively. She worked in the Physics Department, University of Constantine, Algeria in 1981 to 2006. She was Head of the physics department, university of Constantine, Algeria from in 1982 – 1986, and she received the professor degree in 1984. CherifaAzizi is currently is a Professor and a dean with the Faculty of Sciences, University of Oum El Bouaghi, Algeria. She is research interests include microwave and millimeter-wave measurements, small-signal modeling of active devices, and microwave and millimeter-wave circuit design.

ZAABAT MOURAD was born in Constantine, Algeria on 1964. He received the Diploma of Higher Studies D.E.S. Physics Option Electronics. And Diploma of Advanced Studies in Physics Energy DEA option Photovoltaic's, Master's degree in electronics components and graduation of doctorate Physics status option Photovoltaic mention: Very Honorable Faculty of Science, University of Constantine. He is presently a Professor, Faculty of Exact Sciences and Natural Sciences and Life Department of Material Science, University Larbi Ben Me HidiOum el Bouaghi; and Director of Laboratory DEVICES ACTIFS AND MATERIALS since 2011.