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A Fuzzy Logic Control Strategy for Buck PFC Converter Based 4- Switch VSI Fed BLDC Motor Drive

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ABSTRACT

In this paper, a new Buck PFC dc–dc converter topology along with fuzzy logic control for a permanent magnet (PM) brushless dc motor (PMBLDCM) has been proposed. The proposed buck-PFC converter topology is on single stage power factor correction converter. A concept of dc link voltage control which is proportional to speed of the PMBLDCM is used in this paper. The stator currents of the PMBLDCM during step change in the reference speed are controlled within the specified limits by an addition of a rate limiter in the reference dc link voltage. The effectives of the proposed control strategy of PMBLDCM drive is validated through simulation results.

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1. INTRODUCTION

Efficiency and cost are the major concerns in the development of low-power motor drives targeting household applications such as fans, water pumps, blowers, mixers, etc [1],[2]. The use of the brushless direct current (BLDC) motor in these applications is becoming very common due to features of high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not limited to house hold applications, but these are suitable for other applications such as medical equipment, transportation, HVAC, motion control, and many industrial tools [3],[4]. The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutator assembly [5],[6]. Power quality problems have become important issues to be considered due to the recommended limits of harmonics in supply current by various international power quality standards such as the International Electro technical Commission (IEC)61000-3-2 [7],[8]. Hence, a diode bridge rectifier followed by a power factor corrected (PFC) converter is utilized for improving the power quality at ac mains. Many topologies of the single-stage PFC converter are reported in the literature and gained importance because of high efficiency as compared to two-stage PFC converters due to low component count and a single switch for dc link voltage control and PFC operation [9],[10].

In similar stage power conversion, the single phase AC supply through diode bridge rectifier followed by DC link capacitor is used to drive the BLDC motor [11]. The capacitor draws high pulsed current with a peak greater than fundamental input AC mains current due to the uncontrolled charging of capacitor [12],[13]. The Back EMF waveform of BLDC motor is trapezoidal in shape. And the stator current waveforms are rectangular in shape. Hysteresis current control is employed to maintain the actual motor

currents close to rectangular reference value [14],[15]. In the speed control loop PI controller normally used to make the motor to run at desired speed. For effective control of speed, PI controller replaced by fuzzy controller .The Fuzzy control controller over comes the limitation of PI controller.

In this paper, a fuzzy control scheme for Buck PFC Converter based Four switch VSI Fed BLDC Motor Drive has been proposed and detail are discussed in section 2.PI and Fuzzy controller details are presented in section 2.1 and section 2.2, section 4 elaborates the simulation of the proposed control strategy of drive system and results are illustrated with the help of graphical representation of performance characteristics for different operating conditions.

2. BUCK PFC CONVERTER FOR FOUR SWITCH VSI FED PMBLDCM DRIVE

The Figure 1 shows the Buck PFC converter for four switch VSI fed BLDC motor drive system. The control scheme employs hysteresis current control techniques to produce gating pulses for VSI switches. The proposed control scheme is low cost and switching losses are also less and also reduced torque ripple, voltage stress and fast dynamic response. The variable DC output of bridge rectifier is fed to Buck –PFC converter. The output of the Buck-PFC converter is given to two leg VSI inverter which drives BLDC motor. The power factor correction control scheme is based on the principle of current multiplier approach. This involves the presence of current loop inside speed control loop, in case of continuous conduction of the converter. The control loop starts with processing of speed obtained by comparing the actual, speed with the desired reference speed. The error is fed to the PI / Fuzzy controller to obtain the reference torque and compared with actual torque of BLDC motor, to produces resultant torque error which is multiplied with suitable constant and amplified in order to provide input to reference current block. The reference current is compared with phase a current which in hysteresis current controller and the hysteresis current controller generates pluses for operation of two leg inverter, a rate limiter is introduced, which limits the current within specified limits.

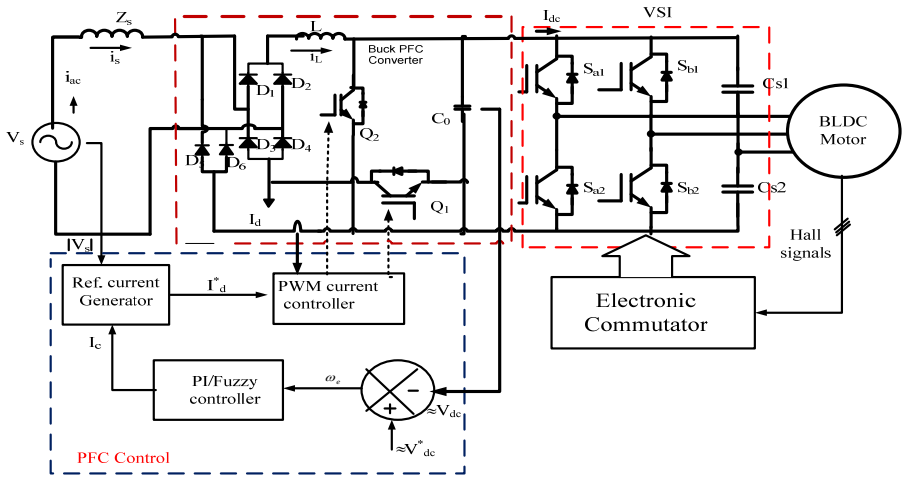


Figure 1. Buck PFC Converter for VSI Fed PMBLDCM Drive

2.1. Proportional- Integral (PI) Control

PI is a combination of integral and proportional terms which reduces the steady state and increases the response time of speed control.PID controller is modified by eliminating the derivative terms and the resulting controller is PI controller shown in Figure 2.

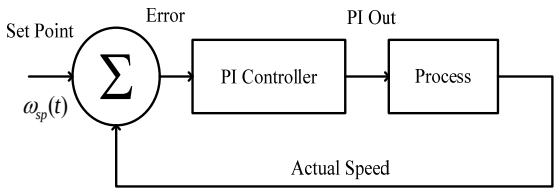


Figure 2. Block diagram of Proportional- Integral (PI) Control

Coming to the working of the PI controller the K_p and K_i values are the respective proportional and integral values of the controller are firstly given assumed values of K_p and K_i respectively. These values are been tuned to the desire values such that the error is minimum and this estimation is done by the error between the output and the set value (desired value).

2.2. Fuzzy Controller

Figure 3 fuzzy logical controller is an advanced controlled using multi valued logical. It is works on the principle of rule based system. It involves two processes namely fuzzification and defuzzication. Fuzzication involves the process of transforming a constant value into linguistic variable while defuzzication deals with hienstic variable conversion to constant value. In other words defuzzication is the inverse process of fuzzication of each input in graphical form. Bell shaped fuzzy member ship functions are used in the proposed work. The inputs to the fuzzy logic controller are speed error and rule of change of speed error and output is reference torque.

Figure 4 show simulink diagram implementation of Fuzzy logic controller (FLC). The rule base system is incorporated is simulink block of fuzzy logic controller. The member ship function considered here are triangular shape. The following are various linguistic terms for the FLC:

- Negative Big (NB)
- Negative Medium(NS)
- Zero (Z)
- Positive Medium (PM)
- Positive Big (PB)

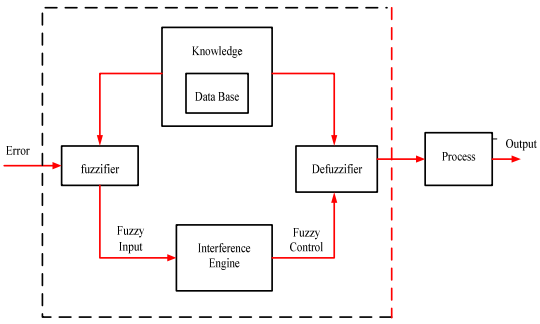


Figure 3. Block diagram of fuzzy logic controller

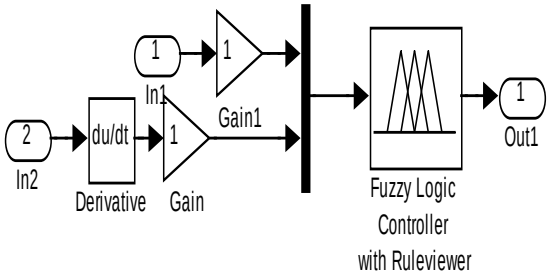


Figure 4. Simulink diagram of fuzzy logical control

After assigning the input, output ranges to define fuzzy sets, mapping of each of the possible seven input fuzzy values of speed deviation, active power deviation to the seven output fuzzy values is done through a rule base. The input and output membership functions are shown in Figure 5 and Figure 6 respectively.

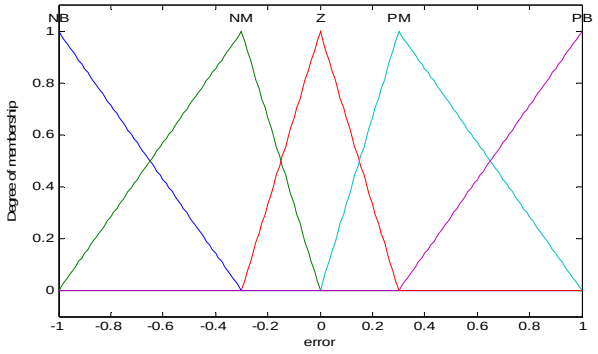


Figure 5. Membership functions for input error

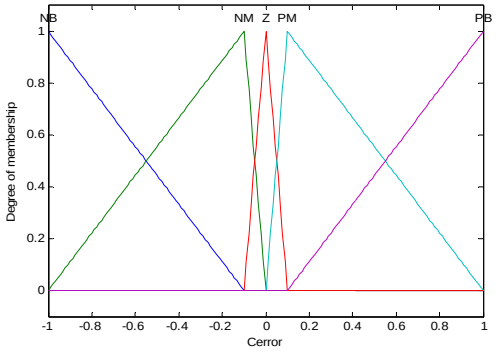


Figure 6. Membership functions for change in 'cerror'

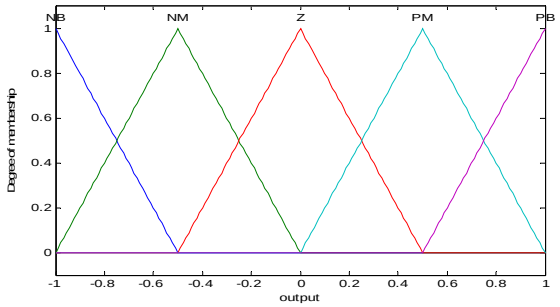


Figure 7. shows the membership function of output variable

Table 1. Rule base for Fuzzy Controller for 4- switch three phase VSI fed Fuzzy speed control drive PMBLDC motor

Error/cerror	NB	NM	ZO	PM	PB
NB	NB	NB	NB	NM	Z
NM	NB	NB	NM	Z	PM
ZO	NB	NM	Z	PM	PB
PM	NM	Z	PM	PB	PB
PB	Z	PM	PB	PB	PB

Rules base:

1. If error in NB and cerror is NB, output is NB
2. If error is NB and c error is NM, output is NB
3. If error is NB and cerror is Z ,output is NB
4. If error is NB and cerror is PM ,output NM
5. If error is NB and cerror is PB, output Z.Similarly the remaining other rules are written in Similar fashion which are tabulated in Table 1.

2.3. Modes of operations of proposed BUCK PFC converter

In this section, the proposed converter operates in CRM will be analyzed in detail. To simplify the analysis, the transitions between the switches and the output diode *Do* are omitted. After that, there still exist eight operation stages in a line period. Figure8. show the equivalent circuits of the stages.

2.3.1. Positive Buck-Boost Operation Mode

At the point when the information voltage Vac is in positive half cycle and the greatness of Vac is littler than Vo, the proposed converter works in buck-help mode. Amid this mode, switch Q_1 keeps OFF and switch Q_2 continues exchanging. There are two stages when the proposed converter works under these modes

Mode 1:

When switch Q_2 is ON the proposed converter works in mode-1. The equal circuit of this stage is indicated in Figure 8(a). The inductor L is charged by V_{ac} through D_1 and D_6, and ill builds amid this stage.

Mode 2:

When switch Q_2 is OFF the proposed converter works in mode-2. The comparable circuit of this stage is demonstrated in Figure 8(b). The inductor L is released by Vo through Do, and il declines amid this stage.

2.3.2. Positive Buck Operation Mode

At the point when the information voltage V_{ac} is in positive half cycle and the greatness is bigger than V_o, the proposed converter works in buck mode. Amid this mode, switch Q_2 keeps OFF and switch Q_1 continues exchanging. There are two stages when the proposed converter works under this modes.

Mode 3:

When switch Q_1 is ON, the proposed converter works in mode- 3. The proportional circuit of this stage is demonstrated in Figure 8(c). The inductor L is charged by $V_{ac}-V_o$ through D_1 and D_4, and il builds amid this stage.

Mode 4:

When switch Q_1 is OFF, the proposed converter works in mode- 3. The equal circuit of this stage is same as that of mode- 2, as indicated in Figure 8(b). The inductor L is released by V_o through D_o, and il declines amid this stage. At the point when the data voltage V_{ac} is in negative half cycle, there likewise exist two operation modes of negative buck-help operation mode and negative buck operation mode of the proposed converter. The negative operation methods can likewise be divided into four operation stages characterized as stages, and the proportionate circuits incorporate.

Figure 8(b), (d), and (e). The negative half cycle operation methodologies of the proposed converter are like those of the positive half cycle. For effort lessees, the negative operation procedures are not portrayed in point of interest here. An enhanced COT control is requested the proposed buck PFC converter to compel it that works in CRM, as indicated in Figure 9.

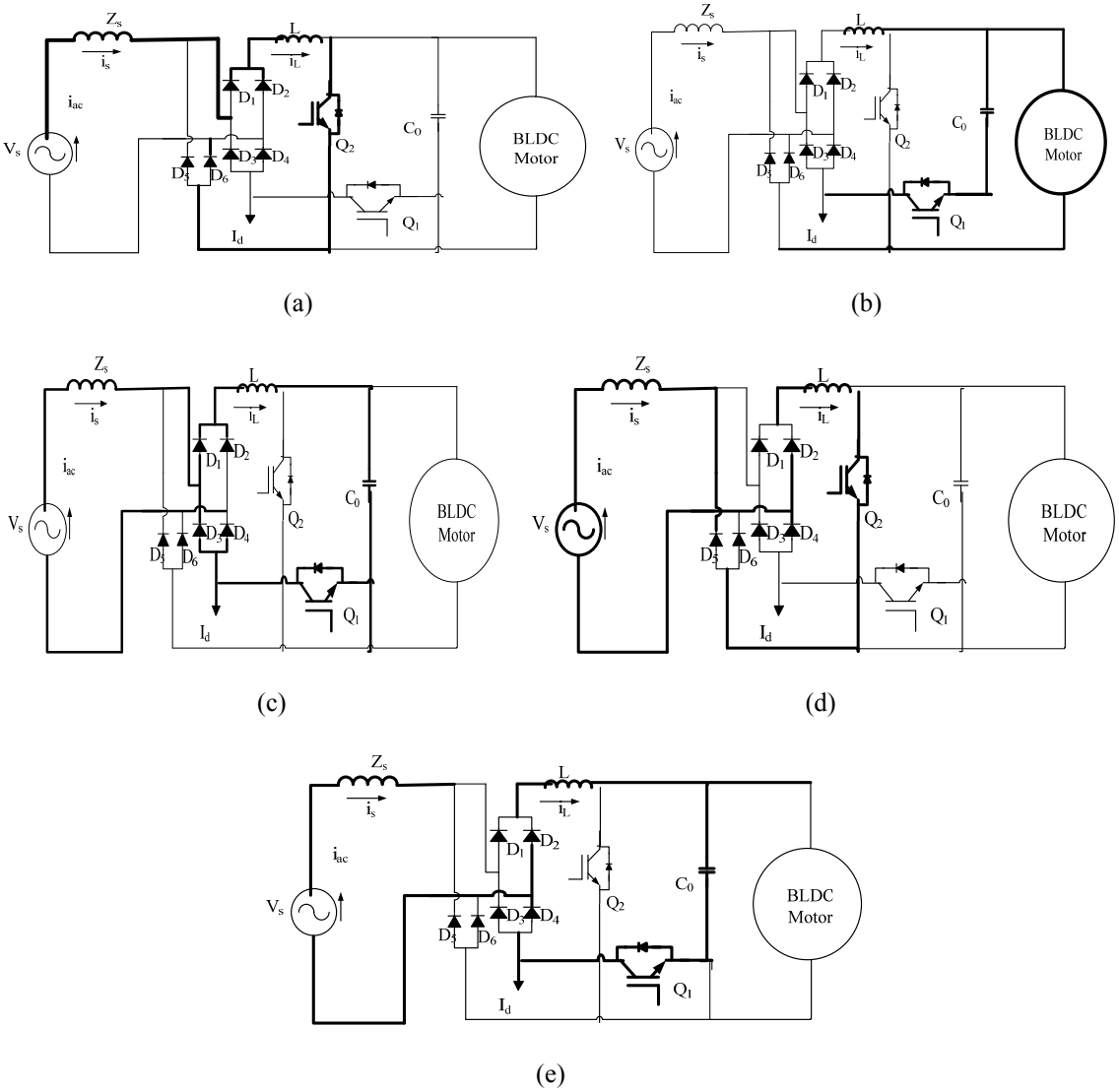


Figure 8. Operation of the proposed converter in different modes

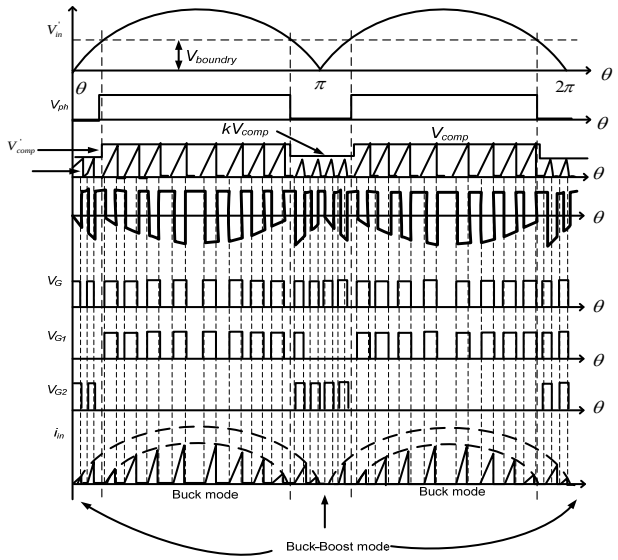


Figure 9. Key waveforms in the improved COT control diagram

The yield voltage is caught with a level-movement circuit framed by a high-voltage transistor Q_2 and the resistors Ra_1~Ra_3. Some key waveforms are indicated in Figure 9. As demonstrated in Figure 9, the control indicator V_{ph} used to control the converter either in buck mode or buck-help mode is attained by contrasting the distinguished V_{in} sign V_{in} and a voltage reference $V_{boundry}$. Typically, $V_{boundry}$ is situated to reflect the yield voltage V_o with the same proportion as that V_{in} reflects V_{in}. V_{ph} is high rationale when V_{in} is higher than $V_{boundry}$ and is low rationale when V_{in} is lower than $V_{boundry}$. The located yield sign VFB is sent to the negative data of the lapse speaker U_f. The slip in the middle of VFB and the set reference V_{ref} is increased by the recompense organizes Cf and an opened up mistake sign V_{comp} is accomplished. The dc voltage sign V_{comp} connected to control the conduction period T_{ON} is attained from V_{comp} through a control systems framed by resistors R_1 and R_2 and switch S_1. Switch S_1 is controlled by the control indicator V_{ph}. The proposed converter works in buck mode when S_1 is OFF and works in buck support mode when S_1 is ON. V_{comp} is a step capacity controlled by V_{ph},.

The zero-intersection purpose of the inductor current il is discovered by the helper slowing down the inductor L. This inductor current zero-crossing location indicator VZCD might be connected in both buck and buck-support modes. At the point when the inductor current il tumbles to zero, the yield voltage assistant slowing down begins to fall. When VZCD tumbles to zero, the yield of comparator UC_2 hops from low level to abnormal state. This level move sets the driving sign from low level to abnormal state. As indicated by the previously stated dissection, the climbing incline of V_{saw} is steady because of the consistent current source I1 charging amid the entire line period. Accordingly, the ON-time (T_{ON}) of the switches is dictated by V_{comp} relatively. More diminutive estimation of k prompts littler T_{ON} and more modest crest estimations of il when the proposed converter is working in buck-help mode. As indicated in Figure.9 the driving signs V_{g1} and V_{g2} are controlled by V_{ph} for the distinctive operation modes on the other hand. Diverse coefficient k brings about the distinctive PF amendment execution and the general productivity.

2.4. Harmonics Analysis

As per the control plan demonstrated in, the normal data current iac in the half line cycle could be communicated in

$$i_{ac}(\theta) = \begin{cases} \frac{I_{P1}(\theta) \times V_g}{2\sqrt{2}V_{ac}\sin\theta} & \theta_0 \leq \theta \leq \pi - \theta_0 \\ \frac{I_{P2}(\theta) \times V_g}{2\sqrt{2}V_{ac}\sin\theta} & (0 \leq \theta < \theta_0) \text{ and } (\pi - \theta_0 < \theta \leq \pi) \end{cases} \quad (1)$$

Where θ_0 is the limit edge between buck-support mode and buck mode

$$\theta_0 = \arcsin \frac{V_{boundry}}{V_{in}}$$

Also $i_{p1}(\theta)$ and $i_{p2}(\theta)$ are the crest estimations of il under buck mode and buck-buck mode, individually

$$i_{p1}(\theta)=\frac{\sqrt{2}V_{ph}\sin\theta-V_b}{L}\times T_{ON}$$

$$i_{p2}(\theta)=\frac{\sqrt{2}V_{ph}\sin\theta}{L}\times k\times T_{ON} \quad (2)$$

2.5. PMBLDC Motor

The windings of a BLDC Motor modelled as a series combination of R L and speed depends on the voltage source, which is known as the back EMF The BLDCM has three phases and those phase voltages are given by the equations. A PMBLDC Motor has three stator phase windings connected in a stator manner. Figure 10 shows the equivalent circuit of a PM BLDC Motor.

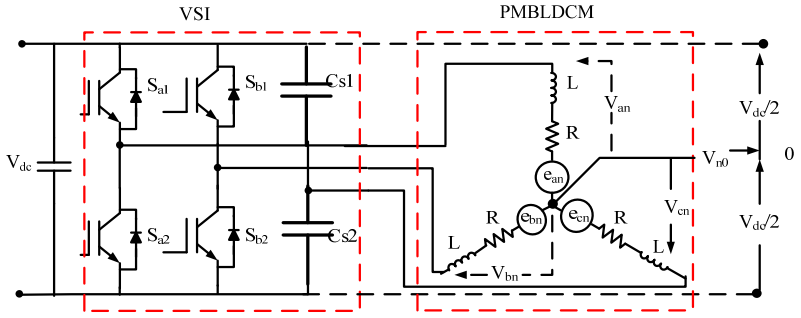


Figure 10. Equivalent circuit of a VSI-fed PMBLDC Motor

$$V_{ao}=\mathrm{Ri}_a+L\frac{di_a}{dt}+e_a+V_{no} \quad (3)$$

$$V_{bo}=\mathrm{Ri}_b+L\frac{di_b}{dt}+e_b+V_{no} \quad (4)$$

$$V_{co}=\mathrm{Ri}_c+L\frac{di_c}{dt}+e_c+V_{no} \quad (5)$$

Table 2. VSI switching sequence based on the Hall Effect sensor signal

H_a	H_b	H_c	E_a	E_b	E_c	S_1	S_2	S_3	S_4	S_5	S_6
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	-1	+1	0	0	0	1	1	0
0	1	0	-1	+1	0	0	1	1	0	0	0
0	1	1	-1	0	+1	0	1	0	0	1	0
1	0	0	+1	0	-1	1	0	0	0	0	1
1	0	1	+1	-1	0	1	0	0	1	0	0
1	1	0	0	+1	-1	0	0	1	0	0	1
1	1	1	0	0	0	0	0	0	0	0	0

Equation (1) & (2) & (3) Where
V_A Voltage of phase =A,V_B Voltage of phase= B,
V_c Voltage of phase =C, I_A Current of phase =A,I_B Current of phase =B,
I_C Current of phase =C,= Stator resistance ,
e_a= Phase "A" stator flux linkages, e_b= Phase "B" stator flux linkages ,e_c= Phase "C" stator flux linkages
e_a= Phase "A" back EMF e_b=Phase"B"back EMF , e_c = Phase "C" back EMF
The shape of the currents should in Rectangular waveform and must be in phase with the corresponding phase back EMF in Table-2. If the self and mutual inductance around the air gap are consider to be constant, then there will be a direct relation between the applied source voltage to the phase terminals (V) and the

induced back EMF (E) is given by equation(3) and the electromagnetic torque (Te) in N.M is given by equation (4).

$$W_e(\mathrm{n}) = \mathrm{W_r}(n)^* - W_r(n) \tag{6}$$

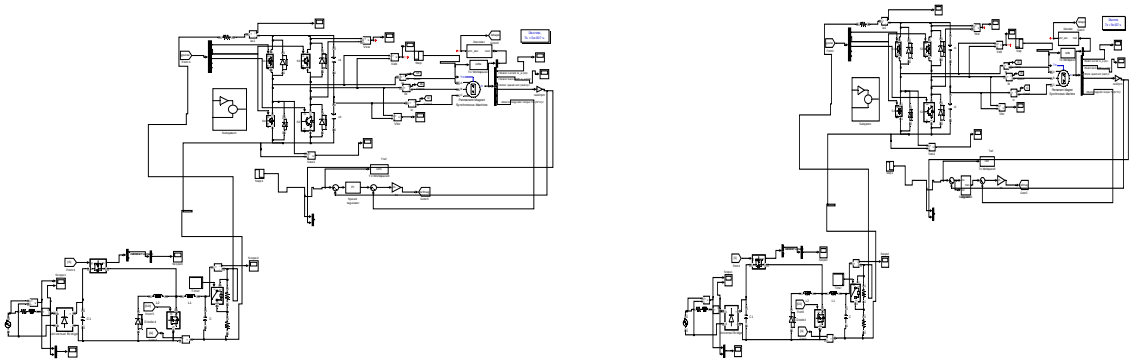
The new value of torque reference is given by

$$T(\mathrm{n}) = \mathrm{T}_{(\mathrm{n-1})} + K_p W_e(\mathrm{n}) - \mathrm{W_e}(\mathrm{n}-1) + K_1 W_e(\mathrm{n}) \tag{7}$$

where We=Rotor mechanical speed.

3. RESULTS AND DISCUSSION

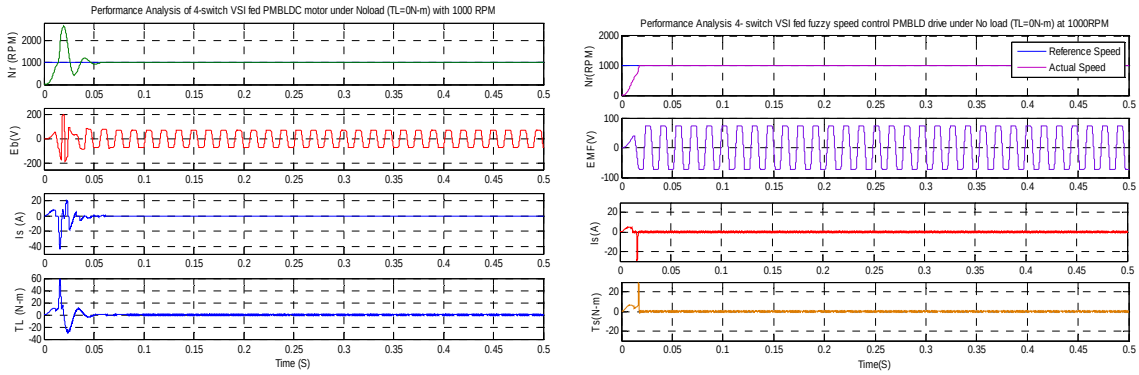
3.1. Buck PFC converter with 4-switch three phase VSI fed speed control of PI and Fuzzy logical control PMBLDC motor drive



(a) Speed control of PI (b) Speed control of Fuzzy logical control

Figure 11. Simulink diagram for speed control of Buck PFC converter six switch 4- switch three phase VSI fed PMBLDC Motor employing PI and Fuzzy control

3.2. No load condition

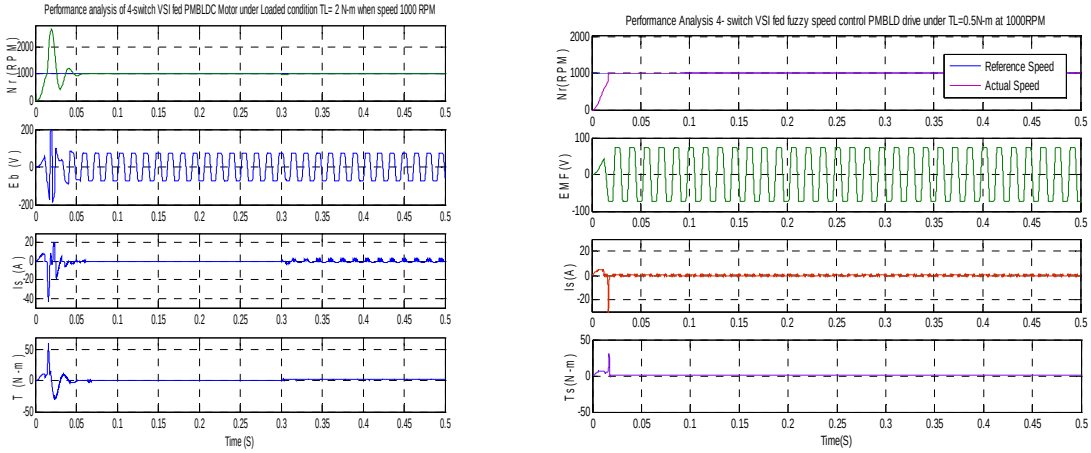


(a) Motor performance waves response with PI Controller (b) Motor performance waves response with Fuzzy Controller

Figure 12. Performance characteristics of Buck PFC converter with **4- switch** VSI fed PMBLDC Motor are shown for a speed of 1000 RPM at No load (TL = 0 N-m)

Figure 12 shows the back EMF stator current and torques initially exhibit some fluctuations but slowly settle down to steady state value. With fuzzy logic controller, the wave shapes of the performance measures are smoothened with no negative peaks or variations .In the whole in case of No load condition, fuzzy logical control of 4-switch VSI fed PMBLDC motor drive exhibits superior performance compared to its counterparts.

3.3. Application of Load



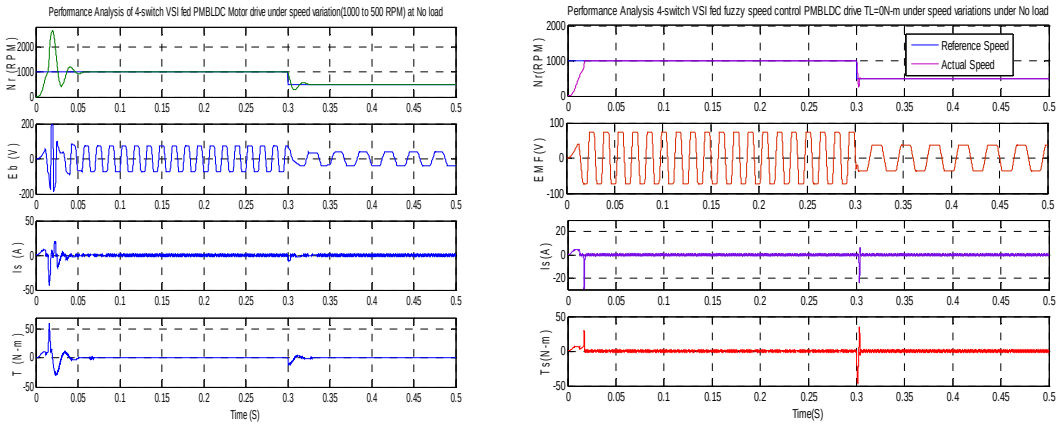
(a) Motor performance waves response with PI Controller

(b) Motor performance waves response with Fuzzy Controller

Figure 13. Performance characteristics of Buck PFC converter with **4-switch** VSI fed PMBLDC Motor are shown for a speed of 1000 RPM under load condition at 0.3secs (TL = 0.5 N-m)

Figure 13 with PI control in case of 4-witch cases the fluctuations are maximum at starting and gradually reduced with PI control. With the fuzzy control, the smooth control is observed with les deviations onnegative side. Summarizing the above, we have for laded condition, 4-switch VSI fed PMBLDC motor employing Fuzzy control exhibits better performance compared to reset of the configuration.

3.4. Dynamic response at No load condition



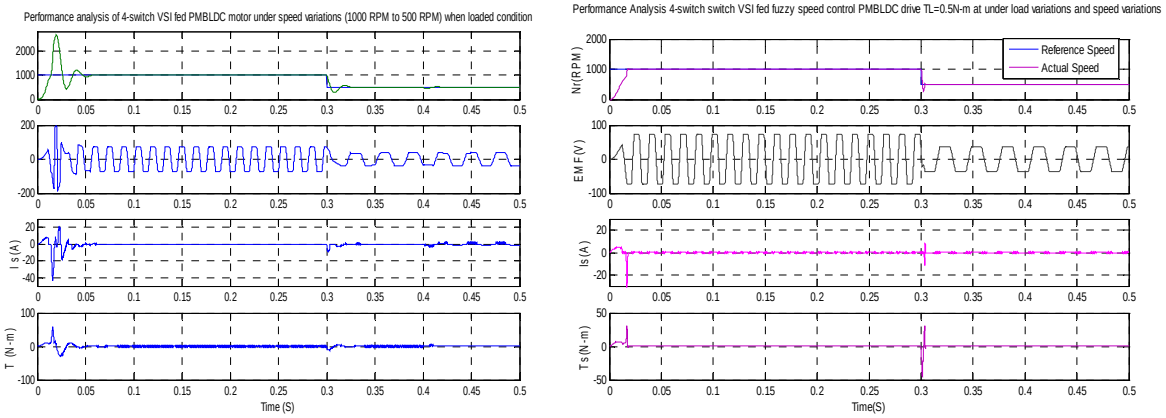
(a) Motor performance waves response with PI Controller

(b) Motor performance waves response with Fuzzy Controller

Figure 14. Performance characteristics of Buck PFC converter with **4-switch** VSI fed PMBLDC Motor are shown for a speed change of 1000 RPM to 500 RPM at 0.25 secs at No load (TL = 0 N-m)

Figure 14 shows with PI control, in case of 4-switch configuration, during dynamic response ,the fluctuation in current and torque are more, where as using Fuzzy control, the fluctuations are minimized and the wave shapes are improved. With PI control in case of 4-switch configuration the fluctuation during dynamic response are reduced. Further using fuzzy logical control, 4-switch configuration exhibits significantly better performance when compared PI control and also 4-switch based configuration with Fuzzy and PI controllers.

3.5. Dynamic response Application of Load



(a) Motor performance waves response with PI Controller

(b) Motor performance waves response with Fuzzy Controller

Figure 15.Performance characteristics of Buck PFC converter with **4- switch** VSI fed PMBLDC Motor are shown for a speed change of 1000 RPM to 500 RPM at 0.3secs under loaded condition (TL = 0.5 N-m)

Figure 15 shows, in case of with 4-switch configuration PI control during dynamic performance under loaded condition, the fluctuation in stator current and torque are maximum among all configuration with Fuzzy control, the deviation are reduced. In case of 4-switch configuration with PI control the fluctuation in the performance measures are lesses. When compared 4-switch configuration. Further with deployment of Fuzzy logical, the deviation is further mitigated and fine control of speed is achieved. In other words, 4-switch configuration with Fuzzy control ideal for efficient and smooth speed control.

4. CONCLUSION

In this paper, an improved buck power factor of PMBLDC motor with 4 switch VSI fed PMBLDC motor was proposed. The performance evaluation of the proposed control strategy has been analyzed under different operating conditions. The effectiveness of the proposed control scheme is that there is minimization of fluctuation in stator current and output torque.

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