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A New Instrumentation Amplifier Architecture Based on Differential Difference Amplifier for Biological Signal Processing

Zainul Abidin[1], Koichi Tanno[2], Shota Mago[3], and Hiroki Tamura[4]
[1]Department of Materials and Informatics, University of Miyazaki, Japan
[2,3]Department of Electrical and System Engineering, University of Miyazaki, Japan
[4]Department of Environmental Robotics, University of Miyazaki, Japan

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ABSTRACT

In this paper, a new Instrumentation Amplifier (IA) architecture for biological signal processing is proposed. First stage of the proposed IA architecture consists of fully balance differential difference amplifier and three resistors. Its second stage was designed by using differential difference amplifier and two resistors. The second stage has smaller number of resistors than that of conventional one. The IA architectures are simulated and compared by using 1P 2M 0.6-μm CMOS process. From HSPICE simulation result, lower common-mode voltage can be achieved by the proposed IA architecture. Average common-mode gain (A_c) of the proposed IA architecture is 31.26 dB lower than that of conventional one under $\pm 3\%$ resistor mismatches condition. Therefore, the A_c of the proposed IA architecture is more insensitive to resistor mismatches and suitable for biological signal processing.

Corresponding Author:
Koichi Tanno
Department of Electrical and Systems Engineering
Institute of Education and Research for Engineering, University of Miyazaki
1-1, Gakuen Kibanadai Nishi, Miyazaki, 889-2192, Japan
tanno@cc.miyazaki-u.ac.jp

1. INTRODUCTION

Biological signals processing by using wearable device is useful for health care system. Sensing of biological signals is a very challenging research. The biological signals, such as Electroencephalogram (EEG), Electrooculogram (EOG), Electrocardiogram (ECG), Electromyogram (EMG), and Axon Action Potential (AAP) have amplitudes in the order of μV to mV and frequencies span from DC to a few kHz, as shown in Fig.1 [1]-[3].

In order to detect and process the very weak and low frequency signals, design of analog front-end has to meet strict performance parameters. IA is often used in sensor interface. Three operational amplifiers (op-amps) based IA architecture is often employed to achieve high signal-to-noise ratio in first block of sensor interface. In the case of biological signals sensing, the IA architecture needs low A_c and it can be achieved by satisfying well-matched condition of resistors network [4]-[10]. However, in actual fabricated chips, resistors are often not well-matched and it deteriorates the A_c.

In reference [3], an IA architecture based on Fully Balanced Differential Difference Amplifier (FBDDA) which its A_c is low and insensitive to resistor mismatches was presented. In this paper, it is called as conventional IA architecture. With same number of resistors (7 resistors including gain-setting resistor), two op-amps in first stage of the 3 op-amps based IA architecture were replaced by using FBDDA. Large common-mode input voltage and limitation of circuit design of the FBDDA (in the first stage) produce some amount of common-mode voltage. Under the resistor mismatches condition, common-mode voltage reduction by the second stage is necessary. This paper focuses on reduction of remaining common-mode voltage of first stage by new design of second stage. Furthermore, a new IA architecture based on Differential Difference Amplifier (DDA) with smaller number of resistors, lower A_c

and more insensitive to resistor mismatches is presented.

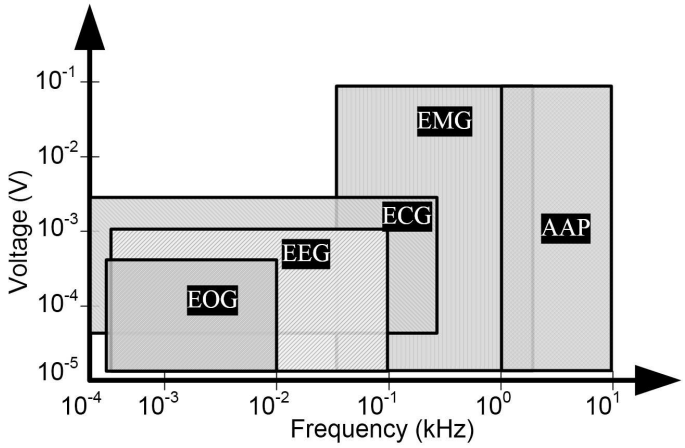

Figure 1. Voltage and frequency ranges of some biological signals

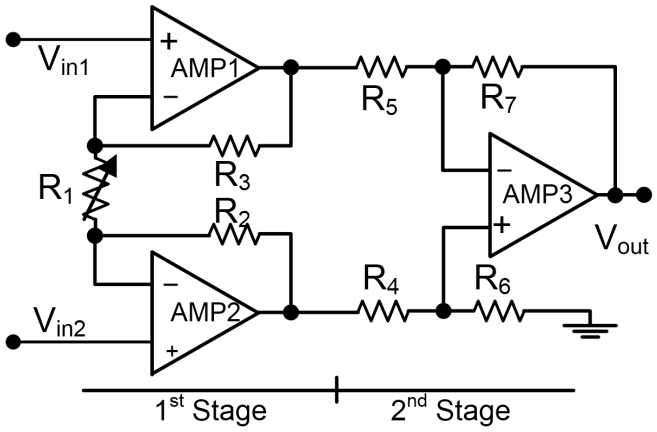

Figure 2. Three op-amps based IA architecture

2. PROBLEM OF CONVENTIONAL INSTRUMENTATION AMPLIFIER ARCHITECTURE

In many text books and literatures, under the condition of well-matched resistors network ($R_2 = R_3$, $R_4 = R_5$, and $R_6 = R_7$), derivation of output voltage of the 3 op-amp based IA architecture shown in Fig.2 (V_{out}), can be determined by

$$V_{out} = \frac{R_7}{R_5}\left(2\frac{R_3}{R_1}+1\right)(V_{in2}-V_{in1}) \tag{1}$$

Defining V_{in1} and V_{in2} as $v_{cm} - v_{dm}$ and $v_{cm} + v_{dm}$, respectively (v_{cm} and v_{dm} are common-mode voltage and differential input, respectively). Representing resistor mismatch of R_i as $R_{i+1}\,(1+\Delta_{i+1}) \mid i \in \{2,4,6\}$, where Δ_{i+1} is mismatch rate of R_{i+1}, the V_{out} becomes [3]

$$V_{out} = \frac{R_7}{R_5}\left\{2\frac{R_3}{R_1}(1+\alpha+\Delta_3\alpha)+1+\alpha\right\}v_{dm} + \frac{R_7}{R_5}(\alpha-1)\,v_{cm} \tag{2}$$

where α is coefficient defined as follows

$$\alpha = \frac{R_5+R_7}{\frac{R_5(1+\Delta_5)}{1+\Delta_7}+R_7} \tag{3}$$

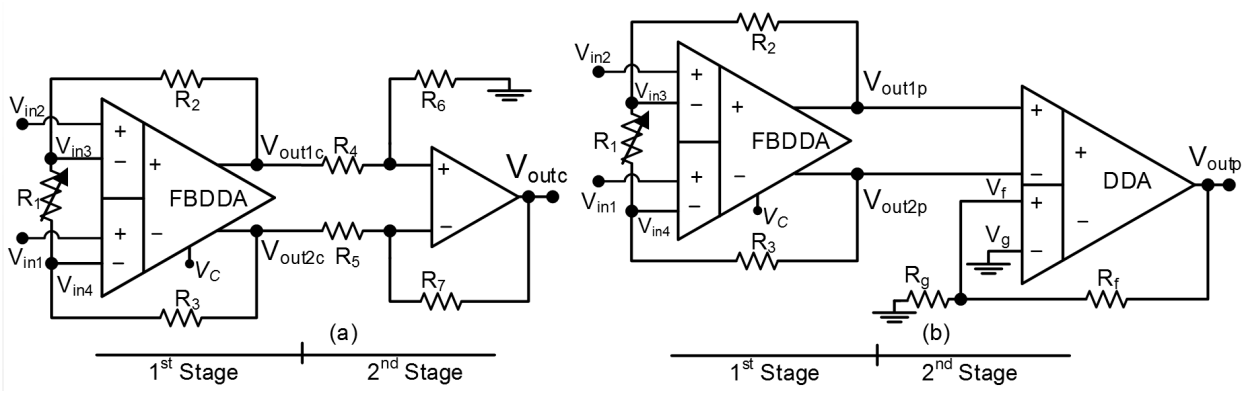

Figure 3. IA architectures: (a) Conventional (b) Proposed

Eq. 2 indicates that the V_{out} contains v_{cm}. The α is caused by resistor mismatches of second stage. Therefore, gain of second stage is often set to 0 dB to avoid deterioration of the A_c. In this way, the A_c of the 3 op-amps based IA architecture is sensitive to the resistor mismatches [3].

In order to overcome this problem, we proposed IA architecture shown in Fig. 3a [3]. The number of resistors in the conventional IA architecture is as same as that in the Fig. 2. First stage of the conventional IA architecture which is modified from [11] was designed by using FBDDA, 2 negative feedback resistors, and gain-setting resistor. The FBDDA consists of 2 stages fully differential gain stage and Common-Mode Feed Back (CMFB) circuit as shown in Fig. 4. Since an ideal amplifier responds only to differential voltage, A_c is zero in ideal case. Therefore, in ideal condition, the output voltages of FBDDA ($V_{out1c,2c}$) can be determined by [11]

$$V_{out1c,2c} = \pm A\{(V_{in2} - V_{in3}) - (V_{in1} - V_{in4})\} \tag{4}$$

where A is the amplification of FBDDA. Using (4) and the defined V_{in1} and V_{in2}, under the same manner of resistor mismatch condition, output voltages of the first stage ($V_{out1c,2c}$) become as follow.

$$V_{out1c} = \left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\} v_{dm} \tag{5}$$

$$V_{out2c} = -\left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\} v_{dm} \tag{6}$$

While, its second stage is op-amp based subtractor. Final output (V_{outc}) of the conventional IA architecture can be derived as follows.

$$V_{outc} = \frac{R_7}{R_5}\left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\}(1+\alpha)\, v_{dm} \tag{7}$$

From the above derivation, v_{cm} can be theoretically rejected since passing first stage and lower A_c can be achieved even though there are resistor mismatches. Therefore, we can set the gain of the second stage larger than 0 dB (offset voltage must be considered).

In actual condition, nonideality must be considered. Limitations in practical circuit design and device mismatches produce some amount of v_{cm}, especially FBDDA [12]. Transistor mismatch often occurs due to channel width and length (W/L). Furthermore, mismatch of W/L value will affect to mismatch of transconductance (g_m) as mentioned in this derivation result [13, 14].

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{8}$$

$$= \sqrt{\left(2\mu C_{ox}\frac{W}{L}\right) \mid I_{ds} \mid (1+\lambda V_{ds})} \tag{9}$$

$$\cong \sqrt{\left(2\mu C_{ox}\frac{W}{L}\right) \mid I_{ds} \mid} \tag{10}$$

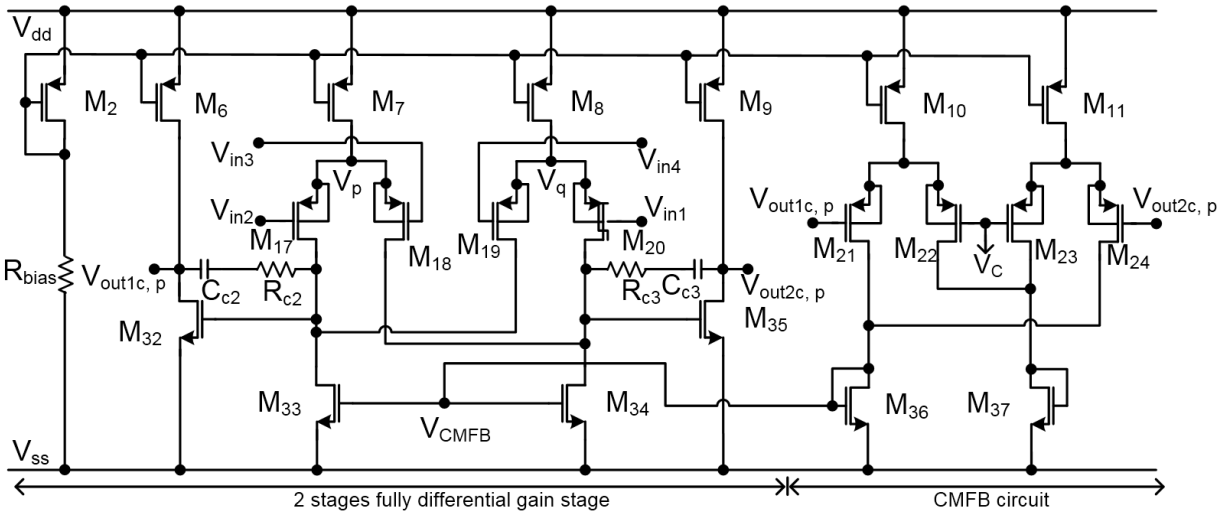

Figure 4. Circuit schematic of FBDDA

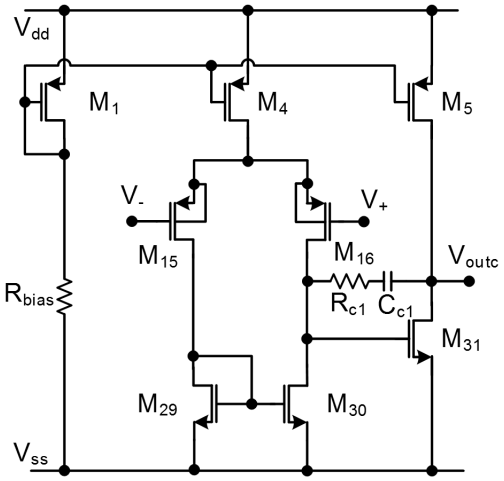

Figure 5. Circuit schematic of op-amp

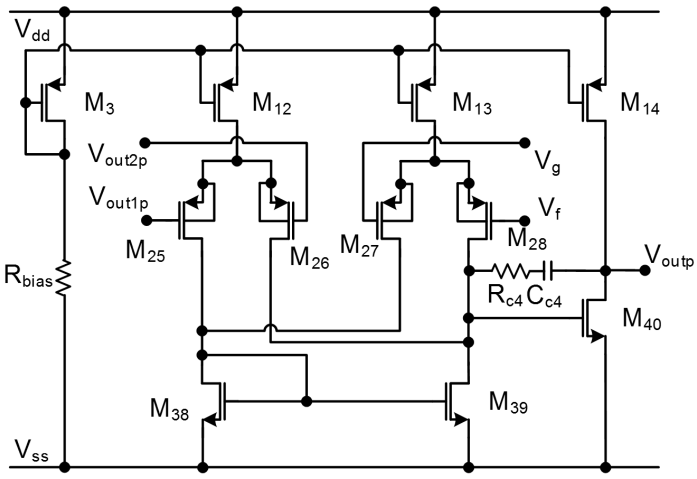

Figure 6. Circuit schematic of DDA

Since the FBDDA main component is cross-coupled amplifier (see Fig. 4), transistor mismatch of cross-coupled amplifier is analyzed. In order to analyze the effect of transconductance mismatch of transistors M_{17}, M_{18}, M_{19}, and M_{20} (see Fig. 4), the cross-coupled amplifier can be simplified by replacing transistors M_7 and M_8 with R_{ss} and transistors M_{33} and M_{34} with R_d. Supplying the inputs with v_{cm}, the common-mode gain of the cross-coupled amplifier (A_{ccr}) can be derived as follows.

$$\begin{aligned} A_{ccr} &= \frac{V_{out2c,p} - V_{out1c,p}}{v_{cm}} \\ &= \frac{\{(g_{m17} + g_{m18} - g_{m19} - g_{m20})\, v_{cm} - (g_{m17} - g_{m18})\, V_p - (g_{m19} - g_{m20})\, V_q\}\, R_d}{v_{cm}} \\ &= \left\{ (g_{m17} + g_{m18} - g_{m19} - g_{m20}) - \frac{(g_{m17}^2 + g_{m18}^2)\, R_{ss}}{(g_{m17} + g_{m18})\, R_{ss} + 1} \right. \\ &\left. - \frac{(g_{m19}^2 + g_{m20}^2)\, R_{ss}}{(g_{m19} + g_{m20})\, R_{ss} + 1} \right\} R_d \end{aligned} \tag{11}$$

Since A_c of FBDDA (A_{cFBDDA}) is not infinite from (11), some amount of v_{cm} may appear in $V_{out1c,2c}$. Because

of gain or resistor mismatches of second stage, the v_{cm} may appear and be amplified in V_{outc}. Finally, this condition deteriorates the A_c of the IA architecture. Next, we discuss about new design of second stage in the proposed IA architecture.

3. PROPOSED INSTRUMENTATION AMPLIFIER ARCHITECTURE

Proposed IA architecture is shown in Fig. 3b. The proposed IA architecture consists of 2 stages. First stage is as same as that of the conventional one. It has the same output voltages ($V_{out1p,2p}$) as (5) and (6), respectively. Second stage consists of Differential Difference Amplifier (DDA) and two resistors which are independent each other. The DDA is 4 inputs single output amplifier. In ideal condition, the relationship can be defined as follows.

$$V_{outp} = A\{(V_{out1p} - V_{out2p}) - (V_f - V_g)\} \tag{12}$$

Implementing DDA for second stage may reduce the remaining v_{cm} of first stage (in $V_{out1p,2p}$ of Fig. 3b) because V_{outp} shown in (12) has component of subtraction ($V_{out1p} - V_{out2p}$) which is independent of resistor mismatch. Furthermore, regarding resistors used in the second stage, number of resistors of the proposed IA architecture is smaller than that of the conventional one. Using (12) and referring Eqs.(5) and (6), the output of the second stage (V_{outp}) under the resistor mismatch condition can be derived as follows.

$$V_{outp} = 2\left(1 + \frac{R_f}{R_g}\right)\left\{\frac{R_3}{R_1}(2 + \Delta_3) + 1\right\} v_{dm} \tag{13}$$

From Eq. (13), even though A_{cFBDDA} is finite, gain of second stage is more than 0 dB, and resistor mismatch of second stage occurs, the v_{cm} can be drastically reduced compared with conventional one.

As mentioned in Chapter 2, in IA shown in Fig. 2, resistor mismatches of second stage cause high A_c (see Eq. (2)). Therefore, implementing 2 independent resistors (R_f and R_g), the second stage of the proposed IA architecture can be set to higher gain to get higher differential gain with smaller effect to the A_c. Furthermore, new design of second stage makes the proposed IA architecture has lower A_c and more insensitive to resistor mismatches than the conventional one.

4. SIMULATION RESULT

In this chapter, the IA architectures were evaluated using 1P 2M 0.6-μm CMOS process. In order to compare the performance of the IA architectures, the transistor level circuit of 3 kinds amplifier were realized. The op-amp in second stage of conventional IA architecture was realized by widely used op-amp circuit shown in Fig. 5 [13, 15]. The DDA was realized by circuit schematic shown in Fig. 6. It consists of 2 stages fully differential gain stage and phase compensation circuits (R_{c4}, C_{c4}) with single output. Fig. 4 shows the employed FBDDA, which is modified from the reference [11]. The FBDDA is developed from DDA by adding CMFB circuit and phase compensation circuits (R_{c2} and C_{c2}) because of its differential output. In the CMFB circuit, V_c is set to 0 V.

Table 1. Simulation Condition

Items	Value
CMOS process	1P 2M 0.6-μm CMOS
V_{dd} [V]	2.5
V_{ss} [V]	−2.5
V_c [V]	0
R_{bias} [kΩ]	295
$M_{1,3}$ [μm/μm]	1.3/2, *M* = 2
M_{4-14} [μm/μm]	1.3/2, *M* = 4
M_{15-28} [μm/μm]	16.1/3, *M* = 2
M_{29-40} [μm/μm]	3.3/2, *M* = 2
R_{c1-4} [kΩ]	9
C_{c1-4} [pF]	0.5

Note: *M* means the number of parallel connection

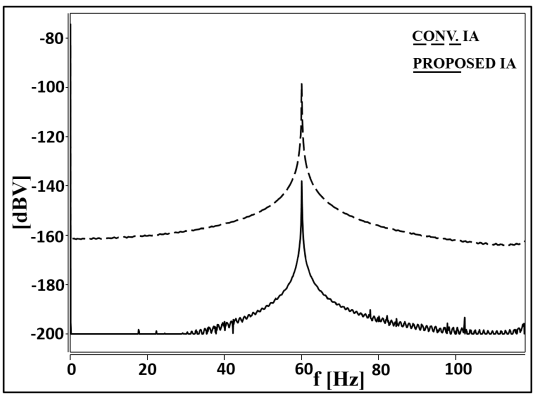

Figure 7. FFT results of V_{outc} and V_{outp}

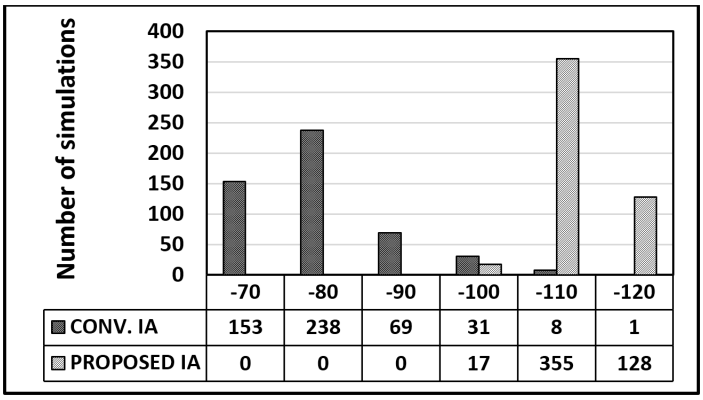

Figure 8. Histogram of A_c (dB) based on Monte Carlo analysis

Table 2. Summary of the Simulation Results

Parameters	Conventional IA	Proposed IA
	AC analysis	
Differential gain [dB]	54.15	54.15
-3 dB gain bandwidth [kHz]	301.34	398.46
Power cons. [μW]	843.79	992.52
	Monte Carlo analysis	
Ave. *Ac* [dB]	-85.53	-116.79
	Noise performance (PV)	
Input ref. noise [μV/$\sqrt{Hz}$]	89.68	89.68
Output ref. noise [mV/$\sqrt{Hz}$]	41.41	45.78

Note: PV = Peak Value

In order to evaluate the A_c, the V_{in1} and V_{in2} were supplied by v_{cm} which is represented by sine wave signal with amplitude of 50 mV and frequency of 60 Hz. The resistors network of both IA architectures (see Fig. 3) was designed as $R_1 = 10$ kΩ, $R_2 = R_3 = R_6 = R_7 = 250$ kΩ, $R_4 = R_5 = 25$ kΩ, $R_f = 9$ kΩ, and $R_g = 1$ kΩ. We set same gain for both stages and the ideal total differential gain of both IA architectures is 54.15 dB.

The IA architectures were simulated using HSPICE. The detailed simulation condition is shown in Table 1. Representing worst case of resistor mismatches condition ($\pm 3\%$), HSPICE simulation was done under the mismatch rates $\Delta_3 = \Delta_7 = 3\%$ and $\Delta_5 = -3\%$. The resistors R_2 and R_6 become 257.5 kΩ and R_4 becomes 24.25 kΩ. Fig. 7 shows the FFT simulation result of V_{outc} and V_{outp}. At frequency 60 Hz, the v_{cm} of the conventional and proposed IA architectures reach -98.66 dBV and -137.34 dBV, respectively. The proposed IA architecture has 38.68 dBV lower v_{cm} than the conventional one.

Monte Carlo simulation was done by 500 times to get data of A_c with deviation of resistor mismatch $\pm 3\%$ was randomly given to all resistors of both IA architectures. Fig. 8 shows histogram of A_c. Average A_c of the proposed and conventional IA architectures are -116.79 dB and -85.53 dB, respectively. The average A_c of the proposed IA architecture is lower than that of the conventional one. Lastly, the simulated performance of the IA architectures are listed in Table 2.

5. CONCLUSION

In this paper, a new IA architecture based on DDA has been presented. Resistor mismatches effect to common-mode gain of IA architectures has been identified and compared in theoretical analysis and HSPICE simulation. With same differential gain and smaller number of resistors, new design of second stage makes the proposed IA architecture has lower common-mode gain. Its ability to achieve lower common-mode gain under resistor mismatches condition makes it more suitable as a part of integrated circuit for biological signal processing. This design was submitted for fabrication. Actual chip evaluation and development of low common-mode DDA and its transistor mismatch effect are considered as future work.

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BIOGRAPHIES OF AUTHORS

Zainul Abidin was born in 1986. He received the B. Eng. from University of Brawijaya and M. Eng. from University of Miyazaki in 2008 and 2011, respectively, and is currently working for University of Brawijaya and toward the PhD degree in Department of Materials and Informatics at University of Miyazaki. He has been involved with design of analog integrated circuit since Master Degree. His current research interest includes analog circuit for biological signal processing. He is affiliated with IEEE and IEICE as student member.

Koichi Tanno was born in Miyazaki, Japan, on April 22, 1967. He received B. E. and M. E. degrees from the Faculty of Engineering, University of Miyazaki, Miyazaki, Japan, in 1990 and 1992, respectively, and Dr. Eng. degree from Graduate School of Science and Technology, Kumamoto University, Kumamoto, Japan, in 1999. From 1992 to 1993, he joined the Microelectronics Products Development Laboratory, Hitachi, Ltd., Yokohama, Japan. He was engaged in research on low-voltage and low-power equalizer for read channel LSI of hard disk drives. In 1994, he joined University of Miyazaki, where he is currently a Professor in the Department of Electrical and Systems Engineering. His main research interests are in analog integrated circuit design and multiple-valued logic circuit design. Dr. Tanno is a member of IEEE and the Executive Subcommittee of the IEEE Computer Society Technical Committee on Multiple-Valued Logic.

Shota Mago was born in 1992. He received the B.Eng from University of Miyazaki in 2015, and is currently studying to get master degree of Electrical and Electronic Engineering at University of Miyazaki. His current research is Analog CMOS Integrated Circuits.

Hiroki Tamura received the B.E and M.E degree from Miyazaki University in 1998 and 2000, respectively. From 2000 to 2001, He was an Engineer in Asahi Kasei Corporation, Japan. In 2001, He joined Toyama University, Toyama, Japan, where He was a Technical Official in Department of Intellectual Information Systems. In 2006, He joined Miyazaki University, Miyazaki, Japan, where He was an Assistant Professor in Department of Electrical and Electronic Engineering. In 2012, He is currently a Professor in the Department of Environmental Robotics. His main research interests are Neural Networks and Optimization Problems. In recent years, He has the interest in Biomedical Signal Processing using Soft Computing.