❒ 754

Fabrication and Analysis of Amorphous Silicon TFT

Srikanth G[1], Yadhuraj SR[2], Subramanyam TK[3], Satheesh Babu Gandla[4], Uma BV[5]

[1,5]Departement of Electronics and communication Engineering, R V College of Engineering, Bengaluru, India
[2,3,4]Inter Disciplinary Research Center, R V College of Engineering, Bengaluru, India

Article Info	ABSTRACT
	The display technology and large area electronics got momentum with the introduction of TFT devices. TFTs can be made using different semiconducting materials or organic conducting materials as the active layer. Each one of them differs in their performance depending on the material used for the active layer. In this paper, fabrication of amorphous silicon TFT using PECVD is carried out. Simulation of the a-Si: H TFT is also carried out with the dimensions similar to that of the masks used for the fabrication. The I_d-V_d plot for both the simulation and fabrication is obtained and studied.

Corresponding Author:

Srikanth G,
Departement of Electronics and Communication Engineering,
R V College of Engineering,
Mysore Road, Bengaluru, India 560059.
Email: srikanthg2007@rediffmail.com

1. INTRODUCTION

Thin film transistor (TFT) devices have revolutionised the display technology. It is a three terminal device with gate terminal insulated from that of the source and drain terminals. TFTs were conceptualised as early as 1925, but their application gained momentum with the demonstration of hydrogenated amorphous silicon (a-Si: H) TFT in 1979 with silicon nitride as the dielectric [1]. Such a device can be fabricated at a lower cost, less fabrication time and less number of steps. They are efficiently being used in the display applications and have found its way to almost every household, as a part of TV sets, cell phone displays, as displays for tablets and many more. One of the most significant advantages of a TFT is that it can be fabricated on flexible substrates and at lower temperatures, and has therefore attracted much attention of researches and industries since its first successful demonstration [2].

The operation of the TFT is much similar to that of MOSFETs; however, the current carrying capability of the former is not as good as that of the latter. The conduction channel in a TFT is formed in the accumulation regime, while that of a MOSFET is formed in the inversion regime. The source and drain are symmetric in both these devices, that is, either of them can be used as a source or a drain depending on the voltage applied to them. The voltage at the gate when above a certain threshold will create a conducting channel between the source and the drain, and when there is a potential drop between source and drain, current starts flowing between them.

Many structures of TFTs are available. Based on the position of the gate and contacts, they are classified as:
a. Top gate top contact
b. Top gate bottom contact
c. Bottom gate top contact
d. Bottom gate bottom contact

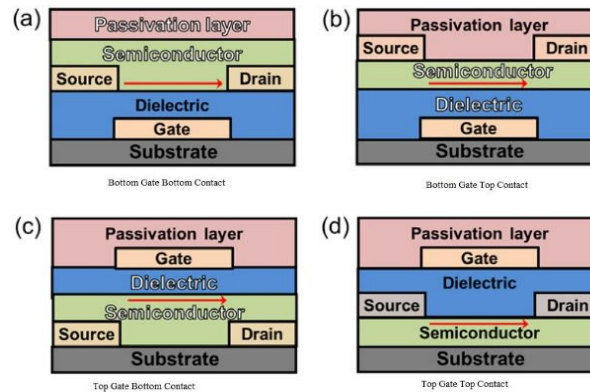The different structures are as shown in Figure 1.

Figure 1. Structure of TFTs

In this paper we report the simulation and fabrication of bottom gate top contact amorphous silicon TFT. The simulation of a-Si: H TFT is done with the dimensions similar to that used for the masks. The I_d-V_d plot from the fabrication and simulation are obtained and studied. The simulation is carried out using Silvaco Atlas tool. The fabrication is carried out using the PECVD (Plasma Enhanced Chemical Vapour Deposition), sputtering and thermal evaporation facilities available at R V college of Engineering, Bengaluru, India. The I_d-V_d plot of the device is obtained using the Agilent BL1500 analyser.

The rest of the paper is organised as follows. The second section provides a description of the fabrication process and the third section provides a description of the simulation. The fourth section provides a comparison of the results obtained which is followed by the concluding section.

2.   FABRICATION

The fabricated device has a bottom gate top contact structure. Float glass is used as the substrate material. Amorphous silicon is used for the active material. Silicon Nitride is used for the gate dielectric and aluminium is used for the contacts.The dimensions of the mask are listed in Table 1. The masks are as shown in Figure 2. Note that with the given mask set, four TFT devices can be fabricated on a single substrate.

Table 1. Dimensions of the Mask

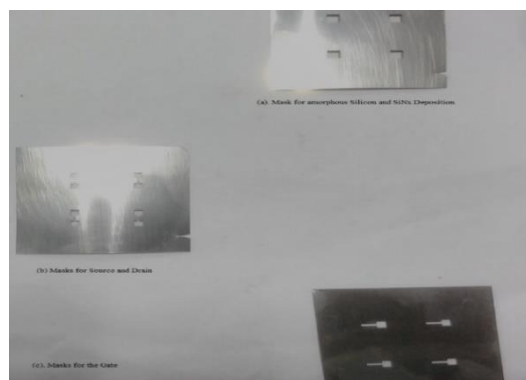| Layer	Dimension
Amorphous Silicon	Square of 3 mm
Gate	A Strip with a width of 250 μm
Distance between source and drain	100 μm

Figure 2. Masks used for the TFT

The masks are made of steel and approximately 1mm in thickness. The mask of Figure 2a is used for the deposition of a-Si: H and SiN$_x$, the mask of 2b is used for the deposition of source and drain while the one in Figure 2c is used for the deposition of gate.

Different processes are used for the deposition of different layers and are listed in Table 2. The deposition process for these layers is refined by carrying out deposition process multiple times and recording the outcome of the same.

Table 2. Processes used for the deposition each layer

Layer	Process
Amorphous Silicon	PECVD
Silicon Nitride	PECVD
Aluminium	Sputtering or Thermal evaporation

The amorphous silicon is deposited using the PECVD. The reactant gases are silane (SiH$_4$) and hydrogen (H$_2$) along with phosphine (PH$_3$) which is used as the dopant. Silicon nitride deposition also uses the method of PECVD. The reactant gases are silane (SiH$_4$) and ammonia (NH$_3$). Aluminium is deposited using the thermal evaporation or sputtering and its resistance is measured which is about 1.2 ohm.

The fabrication process starts with the deposition of the gate over the glass substrate. A layer of SiN$_x$ is deposited over it. The a-Si: H is then deposited on top of the dielectric layer and finally the source and drain.

The thickness of the amorphous silicon is 62 nm and that of the silicon nitride is measured to be about 7.5 um. The snapshot of the fabricated TFT is as shown in Figure 3.
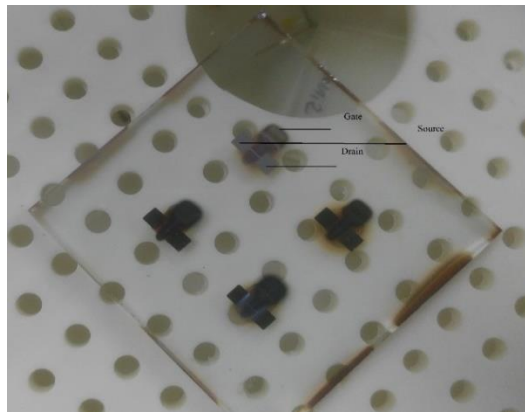

Figire 3. Fabricated TFT

As already mentioned using the given masks four TFTs can be fabricated on a single substrate. The Gate, Source and Drain contacts are marked in the figure.

3.   SIMULATION

The simulation is carried out using Silvaco Atlas tool. The dimensions of the TFT are chosen to be similar to that of the mask. The thicknesses of the TFT layers are measured after the fabrication of the TFT and the same is used for the simulation. Figure 4 shows the structure of the simulated TFT. The thickness of the source, drain and gate are chosen to be 0.05 um. The simulated TFT also has a bottom gate top contact structure. The channel length here is 100 um.

In the simulation, oxide layer is used for the substrate. And a passivation layer is also shown for the device.

During the fabrication it is often difficult to get the desired quality of deposition. An example of such a case is the decrease in the length of the channel due to spread in the deposited layer for source and drain (aluminium). A simulation is carried out with the channel length being 50 um to obtain the I$_d$-V$_d$ plot for this case. Figure 5 shows the structure of the simulated device with the channel length being 50 um.
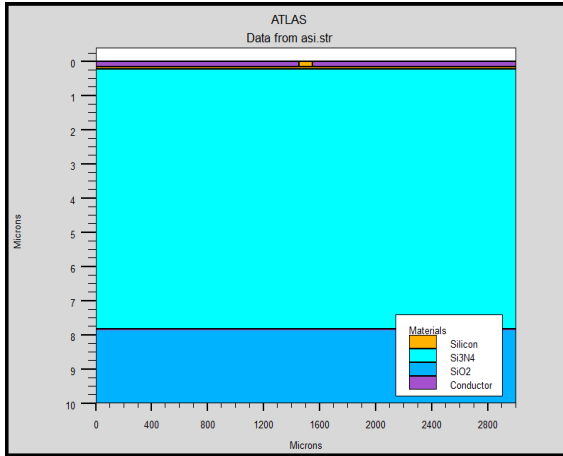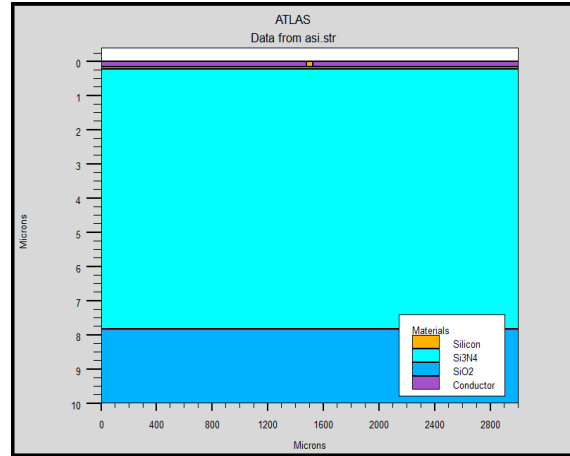
Figure 4. Structure of the Simulated TFT (100 um channel length)

Figure 5. Structure of the Simulated TFT (50 um channel length)

4. RESULTS AND DISCUSSION

The I_d-V_d study of the fabricated TFT is done using Agilent BL1500 series equipment. It is found that two of the devices had defects in fabrication and could not be tested for the I_d-V_d plot, while the I_d-V_d plot for the other two devices is shown in Figure 6a and 6b.
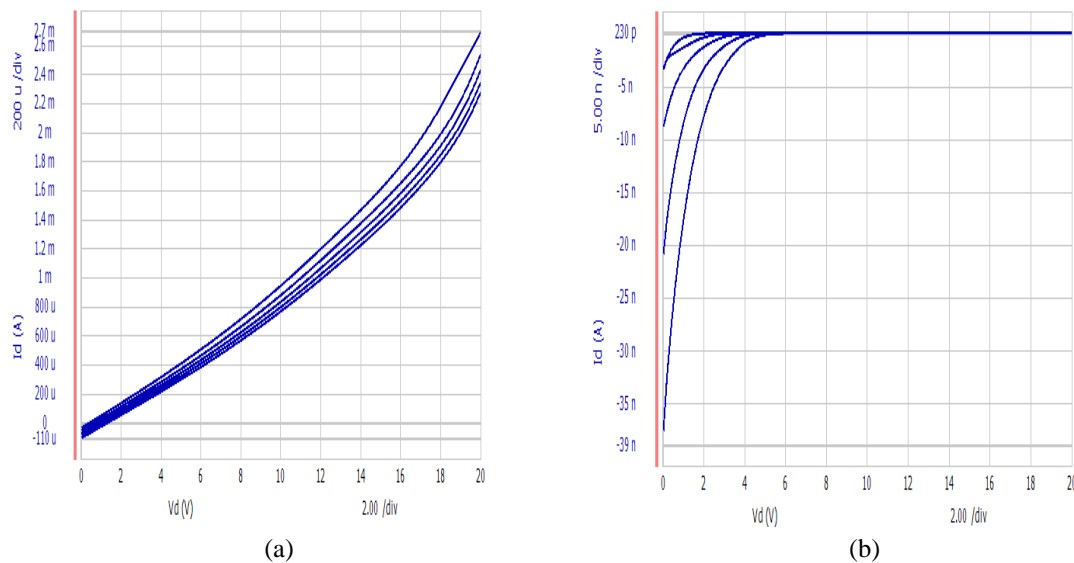

(a)   (b)

Figure 6. (a) I_d-V_d plot for the fabricated TFT showing a linear curve without saturation, (b) Id-V_d plot for the fabricated TFT showing saturation for a very low value of the current

Figure 6(a) shows a linear curve without any saturation, while the one in Figure 6(b) shows saturation for a very low value of the current. It is clear that in the first case the device characteristics is deteriorated, while in the second case the current is of very low value. This can happen because of the unwanted stress and the strain generated in the deposited layers. Such factors might lead to the creation of defect regions in the a-Si: H layer reducing its current carrying capability. A similar behaviour is also found if the source-drain distance is very small. Other factors that might result in such deterioration include the manual handling of the masks, and its misalignment.

The simulation results for the device are as shown in Figure 7(a) and 7(b).
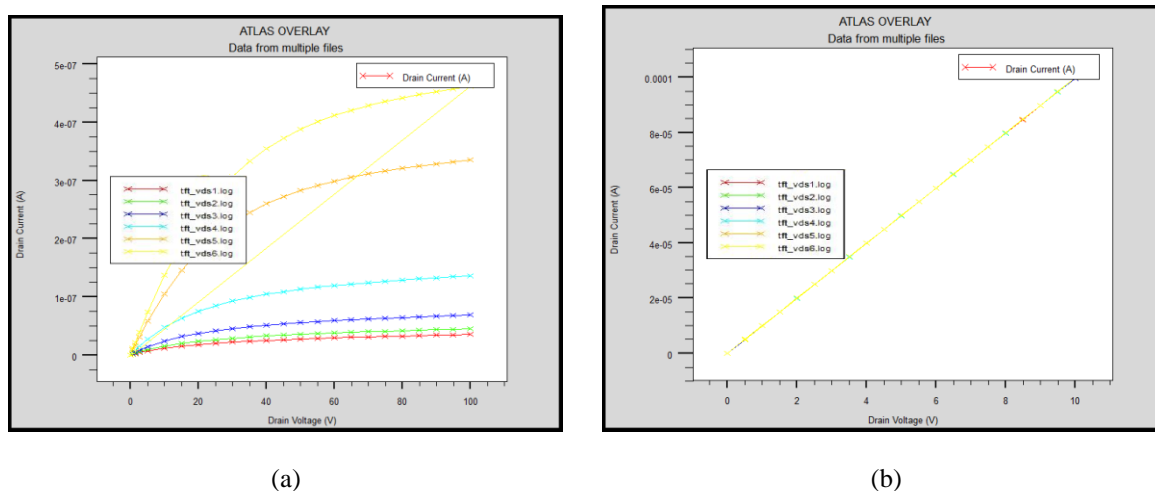
(a)   (b)

Figure 7. (a) I_d-V_d plot for the simulated TFT (Channel Length 100 um), (b) I_d-V_d plot for the simulated TFT (Channel Length 50 um)

It is found that the results from the simulation also show a deteriorating behaviour when the channel length is too short (shown in Figure 7(b)). While the desired dimensions are maintained, other factors like stress and strain in the layer in turn leading to defect generation can decrease the current carrying capability of the device. This throws some light on the behaviour of the saturation current in the simulation and fabrication results mentioned in this section.

5. CONCLUSION

The fabrication of the amorphous silicon TFT is carried out in the facility available at R V College of Engineering, Bangalore, and simulation of TFT using Silvaco Atlas. The I_d -V_d characteristics for both the fabricated and simulated TFT are obtained and studied. The reasons for deterioration of the drain current is due to stress and the strain in the deposited layers, which in the case of the amorphous silicon can create defects and reduce its current carrying capability, very short channel length. It could also be due to the misalignment of the masks or due to the errors inherent with human handling of the masks.

A good yield, a best performance device and the repeatability of process with desired characteristics are the primary goals of any fabrication process. Further work is being carried out in order to improve the deposition process and to fabricate more efficient TFTs with a good yield.

REFERENCES

[1] Yue Kuo, "Thin Film Transistor Technology—Past, Present, and Future", the Electrochemical Society Interface, Spring, 2013.
[2] M. Hatano, H. Hamamura, M. Matsumura, Y. Toyota, M. Tai, M. Ohkura, and T. Miyazawa, ECS Trans., 3(8), 35 (2006).
[3] L.J. Chen, Y.C. Wu, J.H. Chiang, M.F. Hung, C.W. Chang, and P.W. Su, "Comprehensive study of pi-gate nanowires poly-Si TFT non-volatile memory with an HfO2 charge trapping layer", *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 260–265, Mar. 2011.
[4] B. Y. Tsui, C. P. Lin, C. F. Huang, and Y. H. Xiao, "0.1 μm poly-Si thin film transistors for system-on-panel (SoP) applications," in *IEDM Tech.Dig.*, 2005, pp. 911–914.
[5] C.W. Tang, S.A. Van Slyke, Appl. Phys. Lett. 51 (1987) 913.
[6] H. Aziz, Z. Popovic, S. Xie, A.M. Hor, N.X. Hu, C. Tripp, G. Xu, Appl. Phys. Lett. 72 (7) (1998) 756.
[7] S.F. Lim, L. Ke, W. Wang, S.J. Chua, Appl. Phys. Lett. 78 (15) (2001) 2116.
[8] A. Cuevas, F. Chen, J. Tan, H. Mäckel, S. Winderbaum and K. Roth, 4th WCPEC, Waikoloa, 1148 (2006).
[9] H. Mäckel and R. Lüdemann, J. Appl. Phys. 92, 2602 (2002).