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A **New Proposal for OFCC-based Instrumentation Amplifier**

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ABSTRACT

This contribution puts forward a new voltage mode instrumentation amplifier (VMIA) based on operational floating current conveyor (OFCC). It presents high impedance at input terminals and provides output at low impedance making the proposal ideal for voltage mode operation. The proposed VMIA architecture has two stages - the first stage comprises of two OFCCs to sense input voltages and coverts the voltage difference to current while the second stage has single OFCC that converts the current to voltage. In addition it employs two resistors to provide gain and imposes no condition on the values of resistors. The behavior of the proposed structure is also analyzed for OFCC non idealities namely finite transimpedance and tracking error. The proposal is verified through SPICE simulations using CMOS based schematic of OFCC. Experimental results, by bread boarding it using commercially available IC AD844, are also included.

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1. INTRODUCTION

Design and development of analog signal processing and generating circuits using current mode (CM) building blocks has been mainstay for past few years. Current conveyor and its variants, being versatile CM building blocks, have been used extensively for these applications. The operational floating current conveyor (OFCC) [1] is a variant of current conveyor with attractive features of both high and low impedance at input and output ports which make it suitable for sensing both currents and voltage and providing the sensed variable in form of current and voltage. The OFCC has been used to develop variable gain amplifier [1], basic amplifier circuits (voltage, current, transimpedance and transconductance) [2-4], filters [5-10], instrumentation amplifier [11], [12], readout circuits [13], logarithmic amplifier [14], rectifier [15], and wheatstone bridge [16] in recent past.

This papers aims at presenting an instrumentation amplifier (IA) which is inevitably used in areas pertaining to industrial process control [17], automotive transducers [18], bio-potential acquisition systems [19-20] and linear position sensing [21], to suppress unwanted common mode noise and to amplify differential signals. In general, the IA structures are classified according to the active block used for realization or on the basis of type of input/output it processes/provides. Taking the later classification into consideration, the available IA may be viewed as voltage mode IA (VMIA), current mode IA (CMIA), transimpedance mode IA (TIMIA) and transadmittance mode IA (TAMIA). The available VMIAs [11], [12], [22-41] employ various active blocks and are compared on the basis of number and type of active block, numbers of resistors/capacitors, input and output impedance, as shown in Table 1.

The findings are placed in Table 1 and following points are noted:

a. The structures presented in [30], [31] use large number of active blocks while those reported in [12 Figure 4(a)], [22-24], [27], [39] employ many passive components.

b. The input impedance of all VMIAs is high while the output impedance of [11], [32-36], [38-41] is not appropriate therefore an additional active block would be needed to access the output.
c. Though the active block count is less than or equal to three in [32-35], [38-41], but an additional active block is needed to access output.
d. The VMIA [12 Figure 5(a)] uses three number of active blocks and resistors each and presents output at proper impedance level.
e. Both VM and CM active blocks are employed in [29-31], [36], [37] therefore the bandwidth is governed by VM block.
f. Component matching is needed in [12], [22-24], [27-31] for proper operation.

Table 1. Characteristics of Available VMIA Circuits

Ref. No.	Active Block Used	Resistors/ CapacitorsUsed	Input impedance	Output impedance
[11]	2 OFCC	4	High	High
[12 Figure 4(a)]	4OFCC	10	High	Low
[12 Figure 5(a)]	3OFCC	3	High	Low
[22]	2 opamps	5	High	Low
[22]	3 opamps	7	High	Low
[22]	4 opamps	6	High	Low
[23]	3 opamps	7	High	Low
[24]	3 opamps	7	High	Low
[25]	3 opamps	2	High	Low
[26]	4 opamps	6	High	Low
[27]	3 opamps	7	High	Low
[28]	5 opamps	5	High	Low
[29]	2 CCII+, 1 opamp	3	High	Low
[30]	6CCII+, 1opamp	3	High	Low
[31]	6CCII+, 1opamp	3, 1 capacitor	High	Low
[32]	2 CCII+	3	High	High
[33]	3 CCII+	2	High	High
[34]	2 CCII+	2	High	High
[35]	2 CCII+	2	High	High
[36]	2CC, 2opamps	2	High	High
[37]	3 opamps, 2 cm*, 1 cs**	2, 1 capacitor	High	Low
[38]	3 CCCII	Nil	High	High
[39]	2 OC	6	High	High
[40]	2CCCII	1 active resistor	High	High
[41]	2CCII	2	High	High

* current mirrors, ** current subtractor

It can be inferred from above discussion that the VMIA reported in [12 Figure 5(a)] uses least component count but requires component matching. The main motivation of this work is to present OFCC based VMIA that uses same active block count as [12 Figure 5(a)] and only two resistors without matching constraint.

The paper is detailed in four Sections. Section 2 describes OFCC port relationship and proposed OFCC based VMIA topology. This Section also includes the behavior of proposed topology in presence of non-idealities namely finite transimpedance gain and tracking errors. The verification of theoretical predictions is done both through simulations and experimentation. The corresponding results are put forward in Section 3. The findings of the paper are concluded in Section 4.

2. PROPOSED OFCC BASED VMIA

2.1. Operational Floating Current Conveyor (OFCC)

The OFCC has two inputs and two outputs and is represented by circuit symbol shown in Figure 1. The input ports Y and X (W and Z) is used respectively for sensing (providing) voltage and currents. The ports X and W have low impedance whereas ports Y and Z present high impedance.

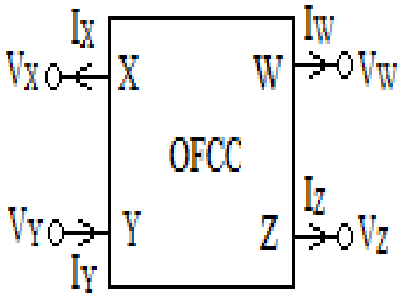


Figure 1. Electrical symbol of the OFCC

The OFCC operation is based on the port relationship of (1):

$$\begin{bmatrix} I_y \\ V_x \\ V_w \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_Z \end{bmatrix} \quad (1)$$

Here, the term Z_t represents open loop transimpedance and its value is very high, therefore feedback between W and X port is essential for developing any application. The frequency dependence of parameter Z_t in (1) is represented using single pole model and is approximated as $Z_t(s) = 1/sC_p$ at high frequencies where $C_p = Z_{to}\omega_{tc}$ (Z_{to} represents open loop transimpedance gain and ω_{tc} corresponds to its cut off frequency). The voltage and current transfers at X and Z ports have a multiplication factor of α and β. Ideal values of these factors are unity, however, in practice there is deviation from this value. The effect of non-ideal voltage and current transfers on circuit operation depends strongly on topology e. g. the performance of the circuit remains unaffected if the terminals whose behaviour is affected by non – ideal behaviour are not used in case of current terminal or corresponding voltage port is grounded.

2.2. Proposed Topology

The architecture of the proposed VMIA, as depicted in Figure 2, comprises of two stages. The first stage, comprises of two OFCCs and a current determining resistor R_1, provides current proportional to input voltage difference (V_{in1} - V_{in2}). A single OFCC ($OFCC_3$) and a resistor are used in second stage which converts the current output of first stage to voltage.

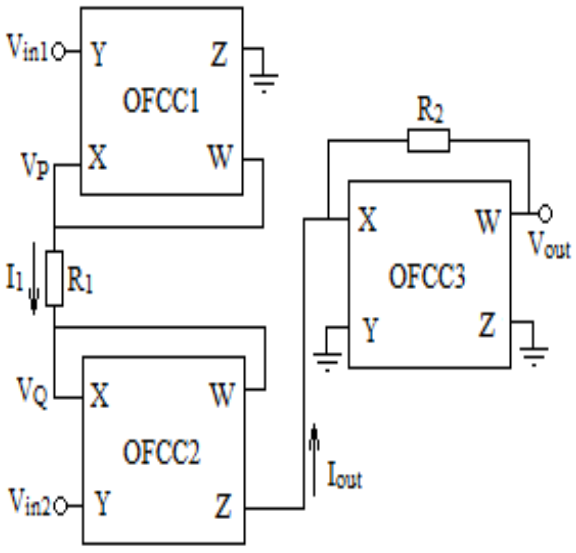


Figure 2. Proposed Instrumentation Amplifier

Using the port relationships of (1), voltages at nodes P and Q in Figure 2 are computed as

$$V_P = \beta_1 V_{in1} \quad (2)$$
$$V_Q = \beta_2 V_{in2} \quad (3)$$

which give current output (I_{out}) of the first stage as

$$I_{out} = \alpha \frac{(\beta_1 V_{in1} - \beta_2 V_{in2})}{R_1} \varepsilon_2(s) \quad (4)$$

where $\varepsilon_2(s) = \frac{1}{1+sC_{p2}R_1}$.

The third OFCC coverts I_{out} to output voltage (V_{out}). Routine analysis of the circuit gives V_{out} as

$$V_{out} = (R_2 \cdot I_{out})\varepsilon_3(s) \quad (5)$$

where $\varepsilon_3(s) = \frac{1}{1+sC_{p3}R_2}$.

Substituting I_{out} in Equation (5) yields

$$V_{out} = \frac{R_2}{R_1} \alpha.(\beta_1 V_{in1} - \beta_2 V_{in2}).\varepsilon_2(s).\varepsilon_3(s) \quad (6)$$

Representing $V_{in1} = V_{CM} + \Delta$ and $V_{in2} = V_{CM} - \Delta$, differential mode gain (A_d) and common mode gain (A_{CM}) are computed respectively as:

$$A_d = \frac{V_{out}}{2\Delta} = \frac{1}{2}\frac{R_2}{R_1} \alpha(\beta_1 + \beta_2)\, \varepsilon_2(s)\, \varepsilon_3(s) = \frac{1}{2}\frac{R_2}{R_1} \frac{\alpha(\beta_1+\beta_2)}{(1+sC_{p2}R_1)(1+sC_{p3}R_2)} \quad (7)$$

$$A_{CM} = \frac{V_{out}}{V_{cm}} = \frac{R_2}{R_1}\alpha(\beta_1 - \beta_2)\, \varepsilon_2(s)\, \varepsilon_3(s) = \frac{R_2}{R_1} \frac{\alpha(\beta_1-\beta_2)}{(1+sC_{p2}R_1)(1+sC_{p3}R_2)} \quad (8)$$

It is clear from Equation (8) that if the OFCCs are matched, the current output (I_{out}) would be zero for common mode input and would result in zero output voltage. There will be deviation from zero output if the OFCCs at input stage are not matched which are discussed in the following Section. Using Eqs. (7) and (8), the common mode rejection ratio (CMRR) is calculated as

$$CMRR = \frac{A_d}{A_{CM}} = \frac{(\beta_1+\beta_2)}{2(\beta_1-\beta_2)} \quad (9)$$

In practice, the values of β_1 and β_2 are close to unity, therefore the proposed topology can give a high value of CMRR. Considering $\alpha = 1$, $\beta_1 = \beta_2 = 1$ and frequencies much below $(1/(C_{p2}R_1), 1/(C_{p3}R_2))$, Equation (7) reduces to

$$A_d = \frac{V_{out}}{2\Delta} = \frac{R_2}{R_1} \quad (10)$$

It is clear from Equation (10) that no matching constraint is imposed on component values for obtaining differential gain. Comparing the proposed VMIA with available OFCC based VMIAs [12 Figure 5(a)] having similar input and output impedances, it is found that later uses equal resistors in first stage.

3. SIMULATION AND EXPERIMENTAL RESULTS

The proposal is examined through SPICE simulations wherein CMOS based schematic of OFCC of Figure 3 [1] is used. Model parameters of 0.5 μm technology from MOSIS (AGILENT) are used. The dimensions of various MOS transistors are given in Table 2. The supply voltages is taken as $V_{DD} = -V_{SS} = 1.5V$ while the bias voltages of $V_{B1} = -V_{B2} = 0.8V$ are considered. The passive components values are taken as $R_1 = 1$ kΩ and R_2 as 5 kΩ, 10 kΩ, 15 kΩ and 20 kΩ to obtain gain values of 14 dB, 20 dB, 23.5 dB and 26 dB respectively.

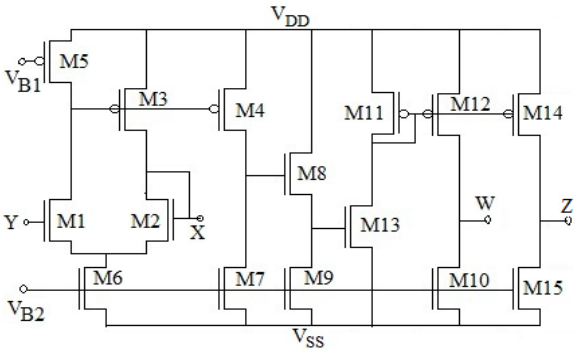


Figure 3. Internal Structure of OFCC [1]

Table 2 MOS transistors Dimensions of the OFCC Structure shown in Figure 3 [1]

MOS Transistor	$W(\mu m)/L(\mu m)$
$M1, M2$	50 / 1
$M3, M4, M11, M12, M14$	50 / 2.5
$M5, M7, M10, M15$	20 / 2.5
$M6, M8$	40 / 2.5
$M9, M13$	100 / 2.5

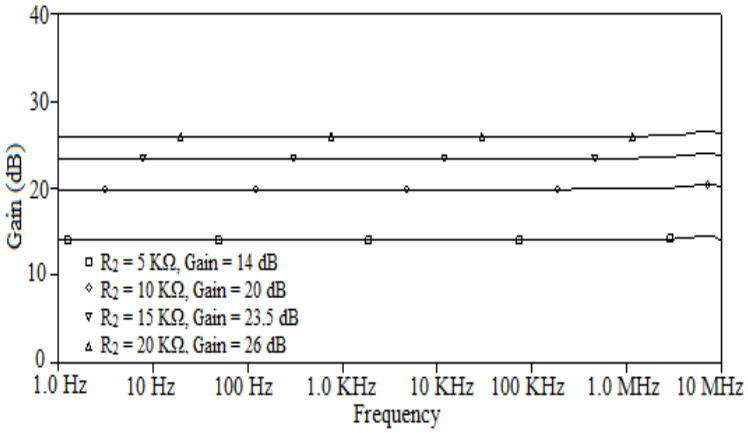


Figure 4. Gains of Proposed Topology with respect to Frequency

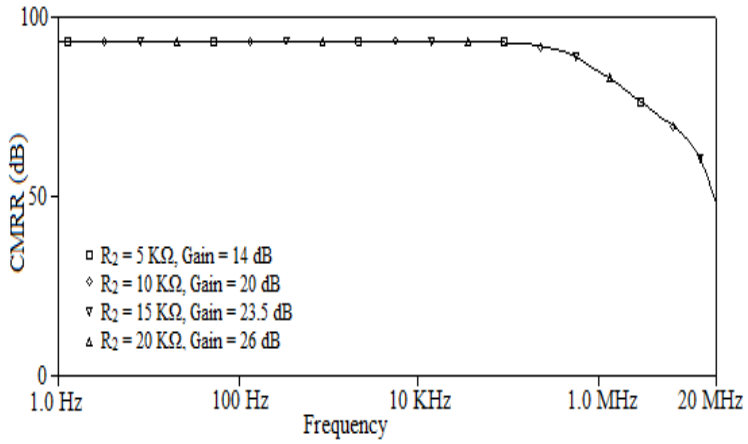


Figure 5. CMRRs of Proposed Topology with respect to Frequency

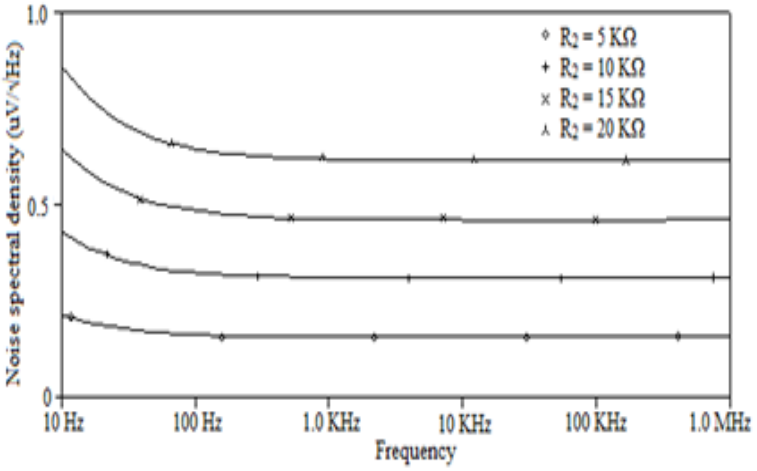


Figure 6. Noise Analysis of Proposed Topology with respect to Frequency

For validation of simulated observations the proposal is prototyped. The OFCC is realized with commercially available IC AD844AN [42] using the setup shown in Figure 7. Experimental observations are plotted for frequency response and CMRR as shown in Figure 8(a) and Figure 8(b) respectively. Output signal obtained through prototype for input signal at frequency of 100 kHz and 1 MHz is shown in Figure 9(a) and Figure 9(b) respectively for authentication. Figure 10(a) shows practical performance for sinusoidal, Figure 10(b) for square and Figure 10(c) for triangular input signals at frequency of 100 kHz each as a proof of the proposal.

Various performance parameters such as CMRR, its bandwidth and CMRR gain bandwidth product (GBP), are compared for available references along with proposed topology parameters and are listed in Table 3. As the IAs given in [11], [12], [22-41] and the proposed one have been tested for different differential gains and at different power supply voltages, it is not fair to compare these on the basis of gain and power consumption.

It is found that proposed VMIA outperforms in terms of both CMRR and its CMRR gain bandwidth product (GBP) as compared to OFCC based VM IA reported in [12 Figure 5 (a)]. As the data for CMRR bandwidth is not available for [22-26], [29-32], [34], [37], [39-41], the comparison of CMRR GBP for the proposed topology is best among all.

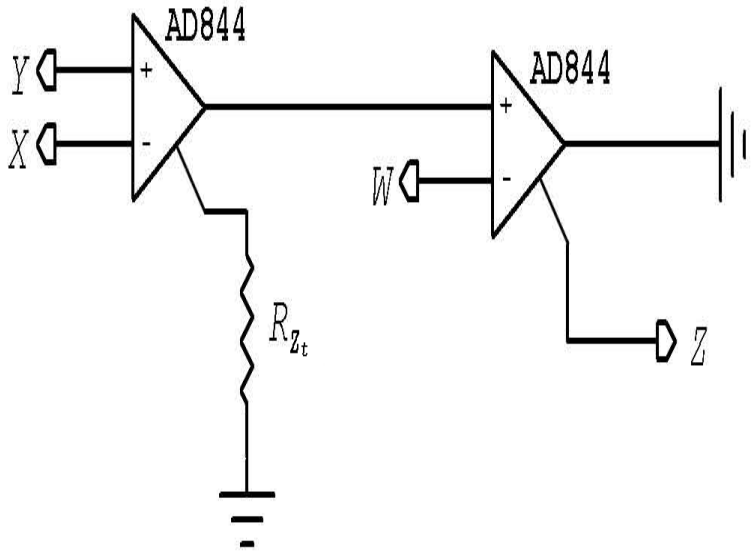
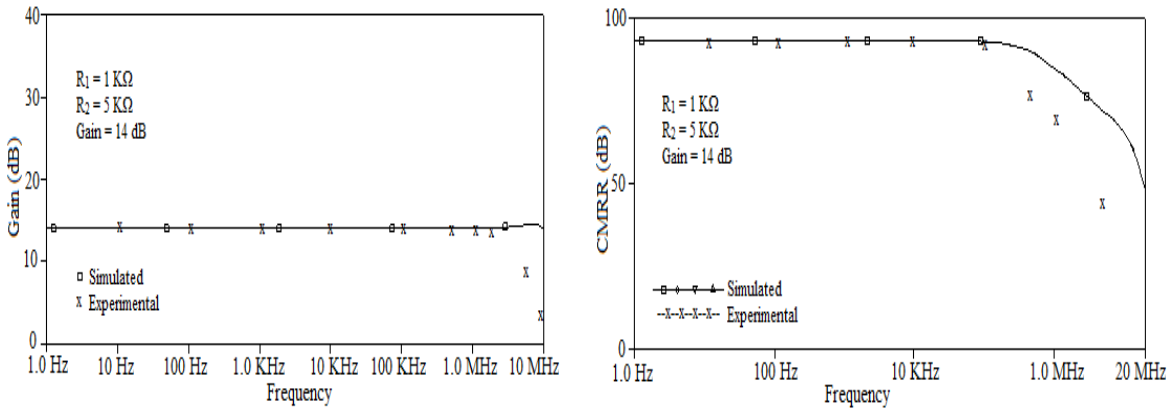
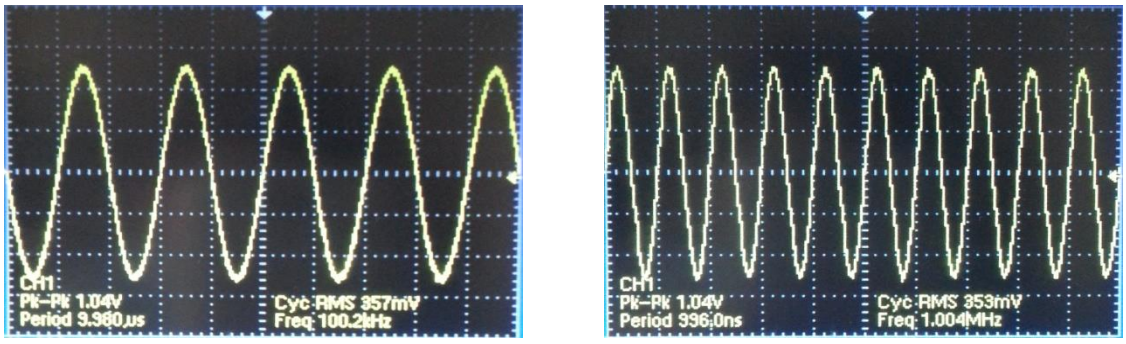


Figure 7. Realization of OFCC using AD844AN



(a) Frequency Response (b) CMRR

Figure 8. Simulated and Experimental Results. (a) Frequency Response and (b) CMRR



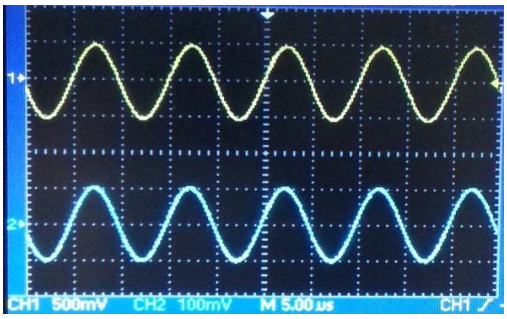
(a) (b)

Figure 9. Outputs (1.04 V each) Observed for Input (200 mV each) of (a) 100 kHz and (b) 1 MHz Frequency

Table 3. Performance Parameters of Available and Proposed IA Circuits

Ref. No.	Mode	CMRR (dB)	- 3dB frequency (CMRR)	Power Supply (Volts)	Experimental Results available
[11]	VM	76	185 kHz	NA	Yes
[12 Figure 4(a)]	VM	81	148 kHz	±1.5	NA
[12 Figure 5(a)]	VM	56	525 kHz	±1.5	NA
[22]	VM	70-90	NA	NA	NA
[23]	VM	NA	NA	NA	Yes
[24]	VM	NA	NA	NA	NA
[25]	VM	80	NA	NA	Yes
[26]	VM	>70 at 100 kHz	NA	NA	Yes
[27]	VM	62	65 kHz	3.3 (single)	NA
[28]	VM	> 60	Upto 200 kHz	NA	NA
[29]	VM	50	NA	NA	Yes
[30]	VM	145	NA	±1.5	NA
[31]	VM	149	NA	±1.5	NA
[32]	VM	100	NA	NA	Yes
[33]	VM	95	65 kHz	NA	Yes
[34]	VM	>70 at100 kHz	NA	NA	NA
[35]	VM	95	2 kHz	NA	Yes
[36]	VM	55	10 kHz	NA	Yes
[37]	VM	130	NA	±2.5	Yes
[38]	VM	147	35 kHz	±2.5	NA
[39]	VM	120	NA	NA	Yes
[40]	VM	142	NA	±3.3	NA
[41]	VM	NA	NA	NA	Yes
Proposed	VM	93.11	423.69 kHz	±1.5	Yes

NA: Not available



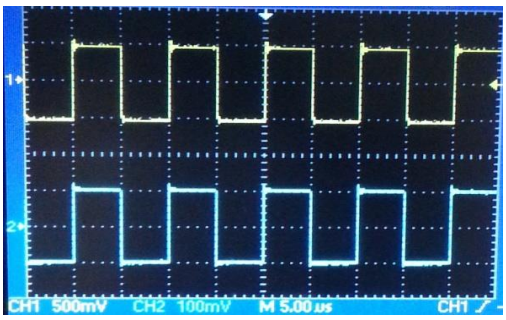
Ch1:

V_{out} = 1.04 V (p-p), 100 kHz
R_1 = 1kΩ, R_2 = 5kΩ (gain = 14 dB).

Ch2:

V_{in} = 200 mV (p-p), 100 kHz
Sinusoidal

(a) Sinusoidal



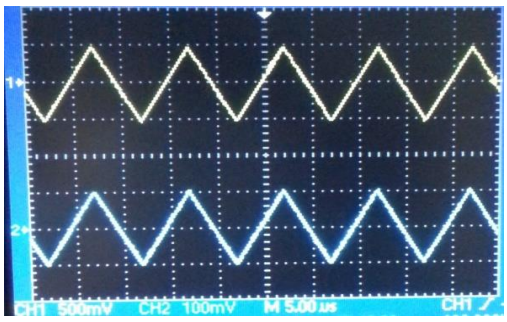
Ch1:

V_{out} = 1.04 V (p-p), 100 kHz
R_1 = 1kΩ, R_2 = 5kΩ (gain = 14 dB).

Ch2:

V_{in} = 200 mV (p-p), 100 kHz
Square

(b) Square



Ch1:

V_{out} = 1.04 V (p-p), 100 KHz
R_1 = 1kΩ, R_2 = 5kΩ (gain = 14 dB).

Ch2:

V_{in} = 200 mV (p-p), 100 kHz
Triangle

(c) Triangle

Figure 10. Experimental Results of the Proposed IA for (a) Sinusoidal (b) Square (c) Triangular Input

4. CONCLUSION

An OFCC based VMIA is proposed in this work that uses three OFCCs and two resistors. The input and output impedances of the proposal are high and low respectively therefore the structure can be used to sense signal from voltage sensor and interface output with system processing voltage signal. Effect of non idealities on behavior of proposal is included. Workability of the proposal is verified through SPICE simulations and experimentations. Comparison of the proposed VMIA with its available counterparts shows that it has highest CMRR GBP and has lowest component count.

REFERENCES

[1] H. M. Hassan and A. M. Soliman, "Novel CMOS realizations of Operational Floating Current Conveyor and applications," *Journal of Circuits Syst. Comput.*, vol/issue: 14(6), pp. 1113–1143, 2005.
[2] C. Toumazou, *et al.*, "Operational floating conveyor," *Electron. Lett.*, vol/issue: 27(8), pp. 651-652, 1991.
[3] A. A. Khan, *et al.*, "Operational floating current conveyor: Characteristics, Modeling and applications," *in IEEE Instrumentation and Measurement Technology Conference, Hamamatsu, Japan*, pp. 788–791, 1994.
[4] Y. H. Ghallab, *et al.*, "Operational floating current conveyor: Characteristics, Modeling and Experimental results," *in Eleventh International Conference on Microelectronics, Kuwait*, pp. 59–62, 1999.
[5] Y. H. Ghallab and W. Badawy, "The Operational Floating Current Conveyor and its applications," *Journal of*

Circuits Syst. Comput., vol/issue: 15(3), pp. 351–372, 2006.
[6] N. Pandey, *et al.*, "Single input four output current mode filter using operational floating current conveyor," *Journal of Active Passive Electronic Components*, pp. 1-8, 2013.
[7] N. Pandey, *et al.*, "Operational floating current conveyor based single input multiple output transadmittance mode filter," *Arabian Journal of Sci. Eng*., vol. 39, pp. 7991-8000, 2014.
[8] Y. H. Ghallab, *et al.*, "A novel universal voltage mode filter with three inputs and single output using only two operational floating current conveyor," *in Proceedings of the 12th International Conference on Microelectronics, Tehran*, pp. 95-98, 2000.
[9] Y. H. Ghallab, *et al.*, "A new second-order active universal filter with single input and three outputs using operational floating current conveyor," *in Proceedings of the 14th International Conference on Microelectronics, Lebanon*, pp. 42–45, 2002.
[10] T. Parveen, "OFC based high input impedance first order and multifunctional biquadratic filter Sections with grounded components and their higher order applications," *Technia- International Journal of Comp. Sci. Commun. Tech*., vol/issue: 4(1), pp. 710-713, 2011.
[11] Y. H. Ghallab, *et al.*, "A Novel Current-Mode Instrumentation Amplifier Based on Operational Floating Current Conveyor," *IEEE Trans. Instrum. Meas*., vol/issue: 54(5), pp. 1941-1949, 2005.
[12] N. Pandey, *et al.*, "Generalized operational floating current conveyor based instrumentation amplifier," *IET Circuits Devices Syst*., vol/issue: 10(3), pp. 209-219, 2016.
[13] Y. H. Ghallab and W. Badawy, "A New Differential PH Sensor Current Mode Readout circuit using only two Operational Floating Current Conveyor," *in Proceedings of IEEE International workshop on Biomedical Circuits & Systems*, pp. 13-16, 2004.
[14] N. Pandey, *et al.*, "OFCC based Logarithmic Amplifier," *in International Conference on Signal Processing and Integrated Networks, Noida, India*, pp. 522-525, 2014.
[15] N. Pandey, *et al.*, "Current-mode rectifier configuration based on OFCC," *in International Conference on Signal Propagation and Computer Technology, Ajmer, India*, pp. 533 – 536, 2014.
[16] Y. H. Ghallab and W. Badawy, "A New Design of a Current-mode Wheatstone Bridge Using Operational Floating Current Conveyor," *in International Conference on MEMS, NANO and Smart Systems, Cairo*, pp. 41-44, 2006.
[17] B. D. Miller and R. L. Sample, "Instrumentation amplifier IC designed for oxygen sensor interface requirements," *IEEE Journal of Solid State Circ.*, vol/issue: 16(6), pp. 677-681, 1981.
[18] V. Schaffer, *et al.*, "A 36 V programmable instrumentation amplifier with sub-20 V offset and CMRR in excess of 120 dB at all gain settings," *IEEE Journal of Solid State Circ.*, vol/issue: 44(7), pp. 2036-2046, 2009.
[19] M. Rahal and A. Demosthenous, "A synchronous chopping demodulator and implementation for high frequency inductive position sensors," *IEEE Trans. Instrum. Meas.*, vol/issue: 58(10), pp. 3693-3701, 2009.
[20] M. S. J. Steyaert, *et al.*, "A micropower low noise monolithic instrumentation amplifier for medical purposes," *IEEE Journal of Solid State Circ.*, vol/issue: 22(6), pp. 1163-1168, 1987.
[21] R. Martins, *et al.*, "A CMOS IC for portable EEG acquisition systems," *IEEE Trans. Instrum. Meas.*, vol/issue: 47(5), pp. 1191-1196, 1998.
[22] J. Szynowski, "CMRR analysis of instrumentation amplifiers," *Electron. Lett*, vol/issue: 19(14), pp. 547-549, 1983.
[23] R. P. Areny and J. G. Webster, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol/issue: 40(4), pp. 669-676, 1991.
[24] R. P. Areny and J. G. Webster, "Common mode rejection ratio for cascaded differential amplifier stages," *IEEE Trans. Instrum. Meas.*, vol/issue: 40(4), pp. 677-681, 1991.
[25] C. Toumazou and F. J. Lidgey, "Novel current mode instrumentation amplifier," *Electron. Lett*, vol/issue: 25(3), pp. 228-230, 1989.
[26] Q. S. Zhu, *et al.*, "High CMRR, second generation current mode instrumentation amplifiers," *in IEEE International Symposium on Circuits and Systems, Chicago*, vol. 2, pp. 1326-1328, 1993.
[27] M. Y. Ren, *et al.*, "Design of CMOS instrumentation amplifier," *in: International Workshop on Information and Electronics Engineering, Harbin, China*, vol. 29, pp. 4035-4039, 2012.
[28] Q. S. Zhu, *et al.*, "Improved wide-band, high CMRR instrumentation amplifier," *Clinical Physics and Physiological Meas.*, vol/issue: 13(A), pp. 51-55, 1992.
[29] K. Koli and K. A. I. Halonen, "CMRR enhancement techniques for current mode instrumentation amplifiers," *IEEE Trans. Circuits Syst.*, vol/issue: 47(5), pp. 622-632, 2000.
[30] B. Babaei and S. Mirzakuchaki, "High CMRR, low power and wideband current mode instrumentation amplifier," *in 24th Norchip Conference, Linkoping, Sweden*, pp. 121-124, 2006.
[31] B. Babaei and S. Mirzakuchaki, "High CMRR and low THD current mode instrumentation amplifier using current inversion technique," *in 25th Norchip Conference, Aalborg, Denmark*, pp. 1-4, 2007.
[32] B. Wilson, "Universal conveyor instrumentation amplifier," *Electron. Lett.*, vol/issue: 25(7), pp. 470-471, 1989.
[33] A. A. Khan, *et al.*, "An improved current mode instrumentation amplifier with bandwidth independent of gain," *IEEE Trans. Instrum. Meas.*, vol/issue: 44(4), pp. 887-891, 1995.
[34] C. Galanis and I. Haritantis, "An improved current mode instrumentation amplifier," *in Proceedings of Third IEEE International Conference on Electronics, Circuits, and Systems, Rodos*, vol. 1, pp. 65-68, 1996.
[35] S. J. Azhari and H. Fazlalipoor, "A novel current mode instrumentation amplifier (CMIA) topology," *IEEE Trans. Instrum. Meas.*, vol/issue: 49(6), pp. 1272-1277, 2000.
[36] S. J. G. Gift, "An enhanced current mode instrumentation amplifier," *IEEE Trans. Instrum. Meas.*, vol/issue: 50(1), pp. 85-88, 2001.

[37] C. A. Prior, *et al.*, "Design of an integrated low power high CMRR instrumentation amplifier for biomedical applications," *Analog Integrated Circuit Signal Process.*, vol. 57, pp. 11-17, 2008.
[38] S. Maheshwari, "High CMRR wide bandwidth instrumentation amplifier using current controlled conveyors," *International Journal of Electronics*, vol/issue: 89(12), pp. 889-896, 2002.
[39] S. J. G. Gift, *et al.*, "High performance current mode instrumentation amplifier circuit," *International Journal of Electronics*, vol/issue: 94(11), pp. 1015-1024, 2007.
[40] H. Ercan, *et al.*, "Voltage and current controlled high CMRR instrumentation amplifier using CMOS current conveyors," *Turkish Journal of Electr. Eng. Comput. Sci.*, vol/issue: 20(4), pp. 547-556, 2012.
[41] T. Kaulberg, "A CMOS Current-mode Operational Amplifier," *IEEE Journal of solid-state circ.*, vol/issue: 28(7), pp. 849-852, 1993.
[42] "Analog devices, 60 MHz, 2000 V/µs, Monolithic Op Amp," Analog Devices Incorporation, AD844 datasheet. http://www.farnell.com/datasheets/77786.pdf

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