

## Modeling and Structure Optimization of Tapped Transformer

Abdelhadi Namoune<sup>1</sup>, Azzedine Hamid<sup>2</sup>, Rachid Taleb<sup>3</sup>

<sup>1,2</sup>Electrical Engineering Department, University of Science and Technology of Oran-Mohamed Boudiaf  
Laboratoire d'Electronique de Puissance Appliquée (LEPA), Oran, Algeria

<sup>3</sup>Electrical Engineering Department, Hassiba Benbouali University  
Laboratoire Génie Electrique et Energies Renouvelables (LGEER), Chlef, Algeria

---

### Article Info

#### Article history:

Received Jun 1, 2016

Revised Aug 23, 2016

Accepted Dec 11, 2016

---

#### Keyword:

Geometrical parameters

High coupling coefficient

Quality factor

Tapped transformer

Technological parameters

---

### ABSTRACT

In this paper, a simplified circuit model of the tapped transformer structure has been presented to extract the Geometric and technology parameters and offer better physical understanding. Moreover, the structure of planar transformer has been optimized by using changing the width and space of the primary coil, so as to enlarge the quality factor  $Q$  and high coupling coefficient  $K$ . To verify the results obtained by using these models, we have compared them with the results obtained by employing the MATLAB simulator. Very good agreement has been recorded for the effective primary inductance value, whereas the effective primary quality factor value has shown a somewhat larger deviation than the inductance.

Copyright © 2017 Institute of Advanced Engineering and Science.  
All rights reserved.

---

### Corresponding Author:

Abdelhadi Namoune,  
Electrical Engineering Department,  
University of Science and Technology of Oran-Mohamed Boudiaf,  
Laboratoire d'Electronique de Puissance Appliquée (LEPA),  
Faculté de Génie Electrique, BP 1505 El-m'naouar, Oran, Algeria.  
Email: namoune.abdelhadi@gmail.com

---

## 1. INTRODUCTION

Transformers are exploited in *RFIC* (radio-frequency integrated circuit) functions in place of two inductors in disparity circuits to acquire superior  $Q$  (quality factor) while absorbing less expire region [1]. They are also utilized for solitary to differential signal translation, impedance matching, signal pairing and phase dividing. A transformer is shaped when two spiral coils, or inductors, magnetically combine due to their close proximity. This reasons the impedance levels, distincted as the ratio of the terminal voltage to the current flow, to modify between coils [2-4]. The transformer characteristics comprise the self-inductance, series resistance, mutual coupling coefficient, substrate capacitances, self resonating frequencies, symmetry and die region. Alike to inductor, the type of transformer structure influences these characteristics and is selected based on the application usage the transformer is intended for. The three ordinary transformer configurations are shown in Figure 1. Figure 1(a) illustrates a tapped structure consisting of an inner winding and an outer winding. Mutual combination between adjacent conductors contributes mostly to the self-inductance of every coil. The structure is not often useful as the mutual inductance is small due to very small coupling [5]. Figure 1(b) shows two spirals interwound in the equal plane. The interwound spirals guarantee electrical characteristics of primary and secondary are equal, including the similar number of turns. The transformer terminals are situated in opposite side's permitting easy access for layout [6]. Figure 1(c) shows two spirals stacked in divide metal planes. The advantage of the structure is an abridged generally region since it is implemented in different metal layers. The flux linkage between the two windings advances due to the close coupling. The coupling coefficient,  $K$ , can be as high as 0.9 for a stacked structure [7]. However, the use of separate metal planes consequences in an asymmetry between the primary and secondary coils

caused by the diverse thickness and metal characteristics of the planes. This layout is suitable for small frequency action as big capacitance between coils due to the overlap results in a low *SRF* (self resonating frequencies) [8].

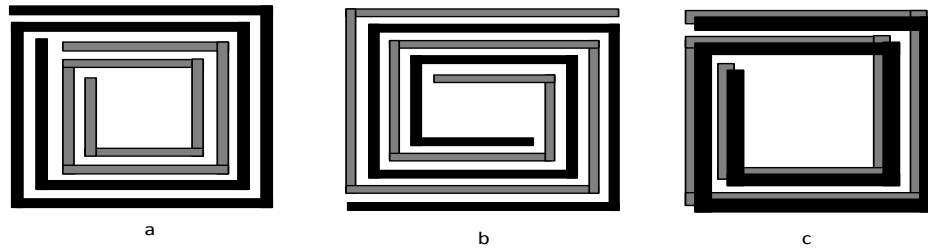


Figure 1. Transformers Physical Structures (a) Tapped (b) Interleaved (c) Stacked

An on-chip transformer model is needed for chip technologies. Modeling and design of on-chip inductors and transformers is presented in [9]. Each inductor is constructed with one metal spiral or winding. On-chip transformers, consisting of various windings, may be designed in different ways.

The tapped transformer design is chosen for various causes. This structure simply permits for any ratio of  $N_p: N_s$ , but in return, due to the large relative distance between windings of the two spirals it consequences in a awfully small coupling coefficient,  $K$ . Clearly, because of including straight relations between two spirals there is a superior possibility of circulating tall levels of noise between parts of the circuit that use magnetic coupling. On the other hand, due to low surface area between the two inductors, the resulted parasitic capacitance is extremely small which consequences in tall self resonance frequency [10]. The advantages are short port-to-port capacitance and tall  $L_p$  and  $L_s$  but have the disadvantages of organism asymmetric and have short coupling coefficient, approximately around 0.3 to 0.7 [11].

In this paper, square shaped tapped transformer has been studied. Section 2; extract the geometrical and technological parameters of the tapped transformer. Section 3, an equivalent-circuit model of tapped transformers is presented. In Section 4, the structure has been optimized by changing the geometrical and technological parameters of the tapped transformer, to enlarge the quality factor  $Q$  and high coupling coefficient  $K$ . Moreover, simulation results will be compared with calculation results. Finally, a conclusion is drawn in Section 5.

## 2. TAPPED TRANSFORMER

Figure 2 illustrate the cross Section view beside the thickness of a typical tapped transformer contrivance. The outer diameter  $OD$  is distinct as the outmost distance between two parallel segments. The inner diameter  $ID$  is distinct as the intimate distance between 2 parallel segments. The width is  $W$ , the spacing is  $S$ . The example device in Figure 2 has  $N_p=N_s = 2$  turns [12], [13].

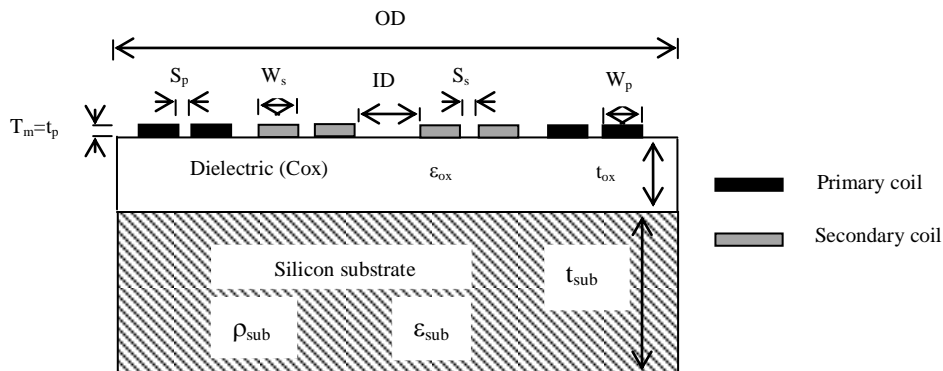


Figure 2. Cross Section View of a Tapped Transformer with the Definition of the Main Geometrical and Technological Parameters

The planned transformer model obtains into explanation an amount of geometrical parameters. They are abridged in Table 1 [14], [15].

Table 1. Geometrical Parameters of the Tapped Transformer

Symbol	Geometrical Parameters
$N_p$	Number of primary turns
$N_s$	Number of secondary turns
$l_p$	Wire length of the primary turns
$l_s$	Wire length of the secondary turns
$W_p$	Width of the metal conductor of the primary turns
$W_s$	Width of the metal conductor of the secondary turns
$t_p$	Thickness of the metal conductor of the primary turns
$t_s$	Thickness of the metal conductor of the secondary turns
$S_p$	Space between metal conductor of the primary turns
$S_s$	Space between metal conductor of the secondary turns
$ID$	Inner diameter of the transformer
$OD$	Outer diameter of the transformer

Technological parameters must be cautiously measured in the enlargement of the model so that it can be legal for an amount of different processes parameters [16], [17]. Table 2 presents a list of the technological parameters, which are considered in the planned model (see Figure 2).

Table 2. Technological Parameters of the Tapped Transformer

Symbol	Technological Parameters
$t_{ox}$	Distance between the substrate and the (primary, secondary) lower face
$t_{sub}$	Substrate thickness
$\epsilon_{ox}$	Equivalent relative permittivity of the dielectric between substrate and conductor
$\epsilon_{sub}$	Equivalent relative permittivity of the substrate
$\rho_{sub}$	Substrate resistivity

### 3. TRANSFORMER MODEL

A lossy transformer can be modeled with an inductor and a resistor in series for each coil representing the dominating series losses as shown in Figure 3. From the model, the characteristics of the tapped transformer can be illustrated [18]. The impedances of the primary and secondary coils are:

$$Z_{11} = R_p + j.\omega.L_p \quad (1)$$

$$Z_{22} = R_s + j.\omega.L_s \quad (2)$$

The inductances of the primary and secondary windings are:

$$L_p = \frac{\text{Im}(Z_{11})}{j.\omega} \quad (3)$$

$$L_s = \frac{\text{Im}(Z_{22})}{j.\omega} \quad (4)$$

The quality factors of the windings are:

$$Q_p = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \quad (5)$$

$$Q_s = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})} \quad (6)$$

To explanation for the inadequate coupling suitable to metal ohmic loss, substrate dissipation, parasitic capacitance and outflow, several parameters are defined [19]. The quality factor represents the power of the magnetic coupling and  $M$  is the mutual inductance between the primary and secondary coils as distinct in Equation 7. For a completely joined transformer, the quality factor is harmony. But in a characteristic process,  $K$  is between 0.3 and 0.9 for monolithic transformers [20]. The relation between coupling coefficient,  $K$ , and mutual inductance,  $M$ , is illustrated in Equation 8.

$$M = \frac{Z_{12}}{j.\omega} = \frac{Z_{21}}{j.\omega} \tag{7}$$

$$k = \frac{M}{\sqrt{L_p.L_s}} \tag{8}$$

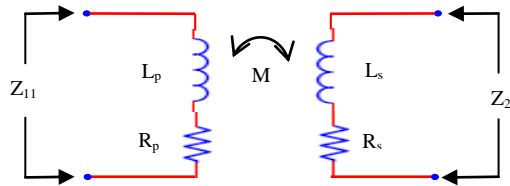


Figure 3. A Lossy Transformer Model

The model for a tapped transformer is exposed in Figure 4. This model comprises two  $\pi$  models, one for each coil. The  $\pi$  model contains the series inductance ( $L_s$ ), the series resistance ( $R_s$ ), the series capacitance ( $C_s$ ), the transformer to substrate capacitance ( $C_{ox}$ ), and the substrate resistance ( $R_{si}$ ) and capacitance ( $C_{si}$ ). The transformer model also includes the spiral-to-spiral capacitances ( $C_{ov}$ ) and the mutual inductance ( $M$ ). The substrate coupling elements  $R_{si}$  and  $C_{si}$  are neglected from the use of a patterned ground shield [21].

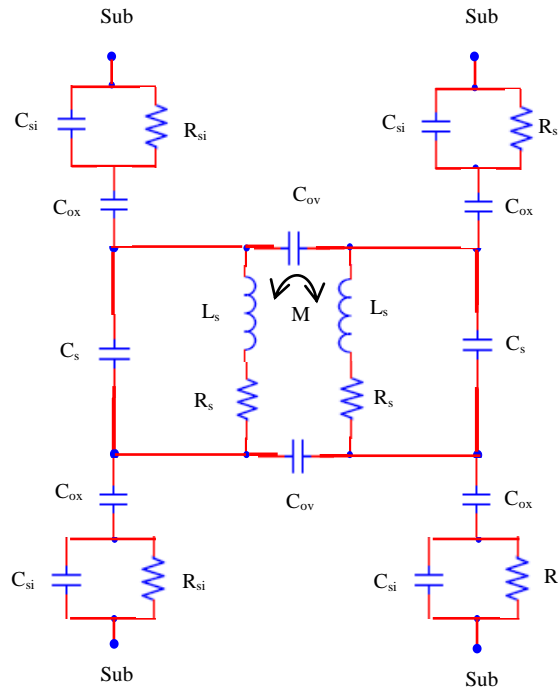


Figure 4. Physical Representation of Equivalent Circuit Model Parameters for Transformer [22]

#### 4. STRUCTURE OPTIMIZATION

##### 4.1. Space and Width of the Primary Coil of the Tapped Transformer

The width and the space between turn's lines of primary coil can influence the inductance and quality factor of tapped transformers. Figure 5 shows the space  $S_p$  and width  $W_p$  of a tapped transformer. When varying the width and space of primary coil, the inductance, quality factor and coupling coefficient will also be changed so as the parasitic capacitance.

For the tapped transformer, if the outer diameter and number of turns is fixed, equal summation of width  $W_p$  and space  $S_p$  leads to approximately the equal region of the tapped transformer, which is a thought in tapped transformer design. Also, the summation constant of width and space (primary coil) are optimized, together verify the performance of the tapped transformer.

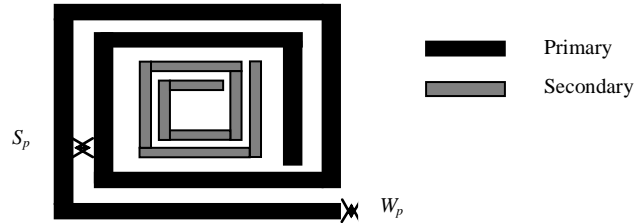


Figure 5. Tapped Transformer Structure (the Indication of width and Space of Primary Coil)

Four tapped transformer structures are considered by care the summation of width and space of the primary coil at  $25\mu\text{m}$ . The width and space of primary coil are  $9+16\mu\text{m}$ ,  $13+12\mu\text{m}$ ,  $17+8\mu\text{m}$ , and  $21+4\mu\text{m}$ , respectively. The number of turns ( $N_p$  and  $N_s$ ) of these four tapped transformers is fixed at 2 and  $OD$  outer diameter is  $250\mu\text{m}$ . Figure 6 shows the four structures of tapped transformer.

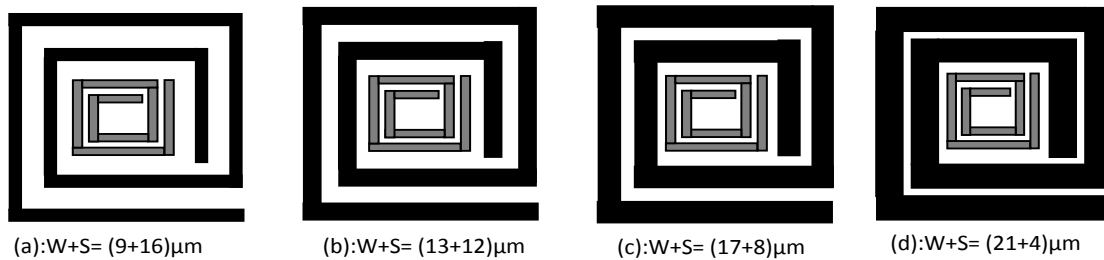


Figure 6. The Four Structure of Tapped Transformers with width Plus Space ( $W_p+S_p$ ) as: (a)  $9+16\mu\text{m}$ , (b)  $13+12\mu\text{m}$ , (c)  $17+8\mu\text{m}$ , (d)  $21+4\mu\text{m}$

Figure 7 shows the inductance  $L_p$  and quality factor  $Q_p$  of primary coil of these four structures. The value primary inductances of these four structures are approximately the equal. Above 5 GHz, the value primary inductances show divergence for the reason that of the diverse element parasitic. For the primary quality factor  $Q_p$ , it is obvious that the structure with the summation of width and space ( $W_p+S_p=17\mu\text{m}+8\mu\text{m}$ ) achieve the major quality factor.

Figure 8 shows the result for the highest value primary inductance can achieve for a square tapped transformer having the thickness of metal  $t_p$ , the widths of primary coil between 2 and  $20\mu\text{m}$  and ( $t_p/W_p$ ) ratios between 0.1 and 0.8 (characteristic device values for primary coil of tapped transformer). It must be renowned that tapped transformers, still although of easy realization, eat a lot of on-wafer region, and wary optimization to contain the top magnitude inductance and quality factor. This optimization must think a known primary inductance value, frequency of action and the technology parameter used to create the tapped transformers.

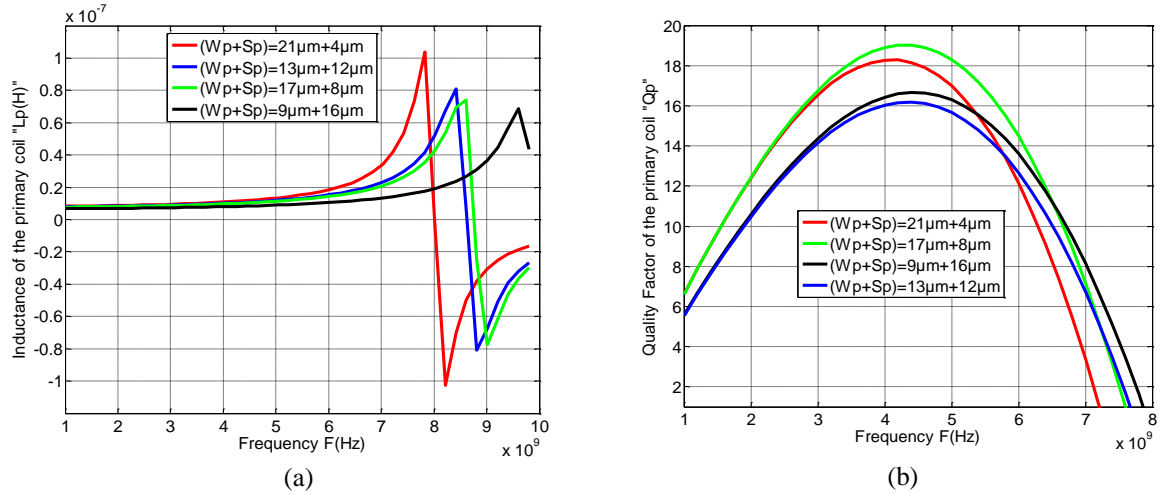


Figure 7. (a) Primary Inductance  $L_p$  and (b) Primary Quality Factor  $Q_p$  as a Function of Frequency of these Four Structures  $(W_p+S_p)$

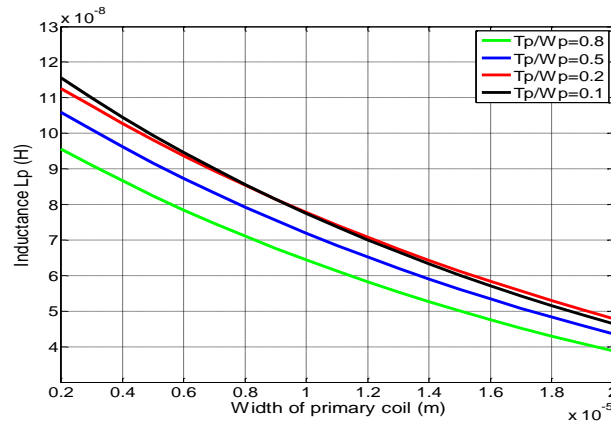


Figure 8. Results for the Primary Inductance of Tapped Transformer having the Width  $W_p$  between 2 and 20  $\mu\text{m}$  and the Thickness of Metal  $t_p$  defined by the  $t_p / W_p$  Ratios between 0.1 and 0.8

#### 4.2. Effect of Geometrical Parameters

To evaluate the inductance of the primary turn of a tapped transformer, we employ the experimental formula [23], [24]:

$$L_p = \frac{37,5 \cdot \mu_0 \cdot N_p^2 \cdot AD^2}{11 \cdot OD - 14 \cdot AD} \quad (9)$$

$$k = 1 - \left( \frac{OD \cdot (14,5 \cdot OD - 13 \cdot AD)}{37,5 \cdot N_p \cdot \sqrt{N_s} \cdot AD^2} \right) \quad (10)$$

where  $N_p$  is the number of primary turns,  $N_s$  is the number of secondary turns,  $OD$  is the outer diameter,  $ID$  is the inner diameter,  $W$  is the track width, and  $S$  is the line-to-line spacing.

In addition ( $W$  and  $S$ ), outer diameter ( $OD$ ) is another important geometrical parameter determining the coupling coefficient value and surface employ of the tapped transformer. Figure 9 shows how coupling coefficient  $K$  varies with changing outer diameter  $OD$  and number of turns of primary coil  $N_p$ . The spacing of primary coil  $S_p$  can be fixed to  $2\mu\text{m}$ , the width of primary coil  $W_p$  can be fixed to  $10\mu\text{m}$  and the frequency  $f$

can be fixed to 5 GHz. bigger outer diameter and augment number of turn  $N_p$  product in elevated coupling coefficient  $K$ .

In a tapped transformer, such as the one in design, the coupling coefficient between the primary and secondary coils is small. Figure 10 shows the coupling coefficient  $K$  as a function of number of turns  $N_p$  and different spacing  $S_p$ , different width  $W_p$  of the primary coil for a tapped transformer. For the unchanged space and width of the primary coil, there is a big development in coupling coefficient  $K$  as number of turn augments.

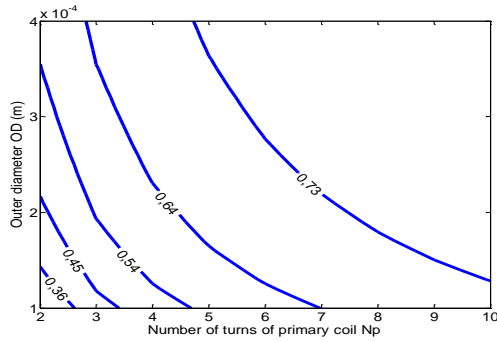


Figure 9. Outer Diameter  $OD$  Versus Number of Turns of Primary Coil  $N_p$  for a Tapped Transformer and a given Coupling Coefficient Value  $K$

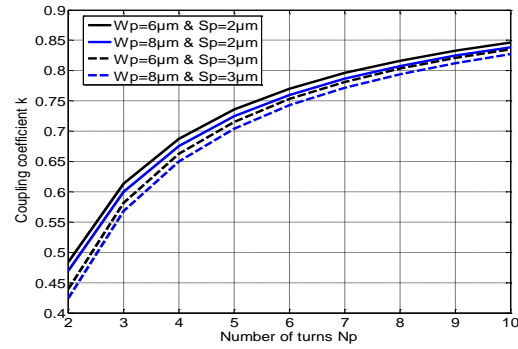


Figure 10. Coupling Coefficient  $K$  as a Function of Number of Turns  $N_p$  and different Metal Trace Width  $W_p$ , and Spacing  $S_p$  for a Tapped Transformer

### 4.3. Effect of Substrate Thickness and Substrate Resistivity

The influence of the substrate resistivity and the substrate thickness on the performance of a 5.2 nH nominal tapped transformer is analyzed. Two different substrate resistivities were simulated: low resistivity silicon ( $LR-Si$ ) at 0.4 W.cm and high resistivity silicon ( $HR-Si$ ) at 7 KW.cm. Two different substrate thicknesses were also simulated,  $T_{sub} = 300 \mu m$  and  $T_{sub} = 500 \mu m$ . The results are shown in Figure 11.

Increasing the thicknesses from 300 to 500  $\mu m$  does not augment significantly the primary quality factor, mostly since the resistance of the substrate is limited by the skin effect. The peak of the primary quality factors at 2.5 GHz and 5.5 GHz. On the additional hand, rising the resistivity of the substrate can augment the primary quality factor, signifying that at very elevated frequency the substrate connected losses are the controlling ones when employing thick substrate ( $T_{sub} > 200 \mu m$ ).

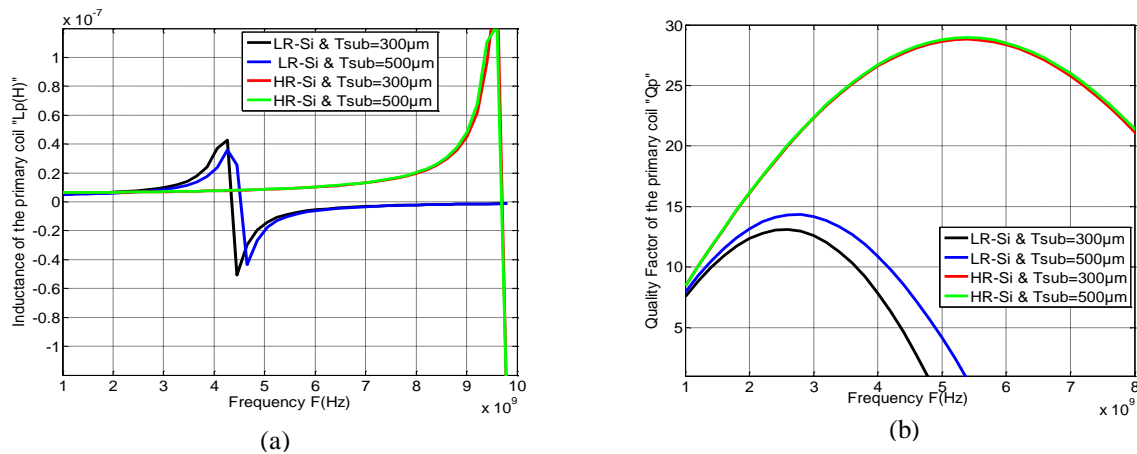


Figure 11. (a) Primary Inductance and (b) Primary Quality Factor as Function of the Frequency for different Substrate Resistivity ( $LR$  – Low Resistivity and  $HR$  – High Resistivity) and different Substrate Thicknesses ( $T_{sub}=300 \mu m$  and  $T_{sub}=500 \mu m$ ).

#### 4.4. Comparisons Between Calculation and Simulation Results

Figure 12 illustrate a comparison of the effective values of the primary inductance  $L_p$  and primary quality factor  $Q_p$  of tapped transformer taken by the calculation of the parameters physical model and by simulation results by MATLAB.

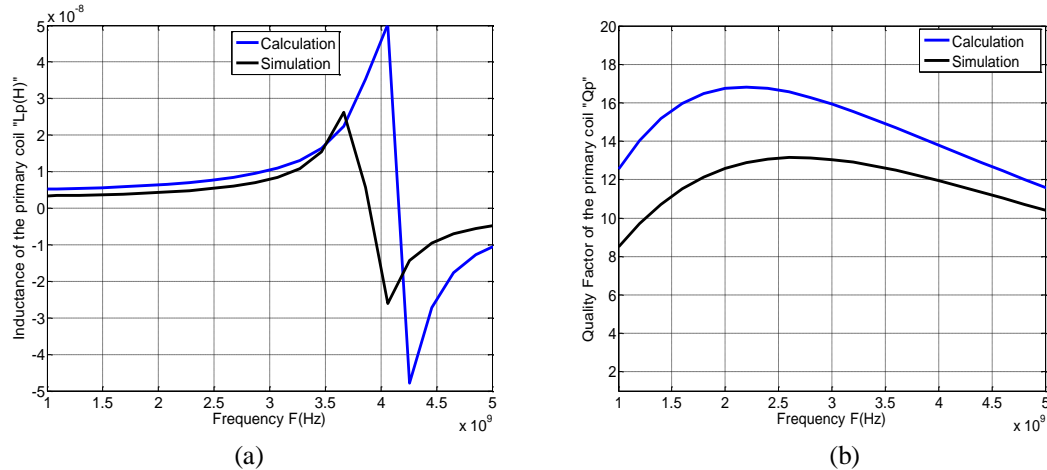


Figure 12. Comparison between Calculated and Simulated Results (a) Primary Inductance and (b) Primary Quality Factor of a Tapped Transformer

A good accord between the calculated and simulated primary inductance value was also achieved in the holder of tapped transformer. A vaguely bigger calculated inductance value was achieved compared with the simulated results. The calculated inductance value at 3 GHz frequency is 10.45 nH. The simulated inductance value at 3 GHz frequency is 7.96 nH.

The maximum primary quality factor value achieved by calculating the parameters of the equivalent model of tapped transformer was 16.82 and was achieved at 2.2 GHz frequency. The maximum primary quality factor value obtained by simulation was 13.15 and was obtained at 2.6 GHz frequency.

## 5. CONCLUSION

In this paper, an equivalent circuit model has been presented to study the tapped transformer. This model presents a great physical perception of the tapped transformer and can be utilized to remove the geometric and technology parameters. The correctness of the circuit model is defined by contrasting its consequence with MATLAB simulation result. Also, the physical structure of tapped transformer has been optimized to obtain improve performance. By contrasting the MATLAB simulation results of diverse structures, the quality factor of tapped transformer is optimized by using appropriate, outer diameter, inner diameter, width, space, substrate thickness and substrate resistivity. The preferred tapped transformer specifications recognized by the designer are transformed into suitable geometrical parameter without neglecting the process parameter.

## REFERENCES

- [1] Parashar K. K., "Design and Analysis of I-Slotted Rectangular Microstrip Patch Antenna for Wireless Application," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 4(1), pp. 31-36, 2014.
- [2] J. R. Long, "Monolithic Transformers for Silicon RF IC Design," *IEEE Journal Solid-State Circuits*, vol. 35, pp. 1368-1382, 2000.
- [3] S. I. Hong, *et al.*, "Robust Digital Predistortion in Saturation Region of Power Amplifiers," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 6(1), pp. 99-105, 2016.
- [4] B. Razzaghzadeh and M. Salimi, "Analysis of a Bidirectional DC-DC Converter with High Voltage Gain," *Bulletin of Electrical Engineering and Informatics*, vol/issue: 4(4), pp. 280-288, 2015.
- [5] Pan S. J, *et al.*, "Comparative Investigation on Various On-Chip Center-Tapped Interleaved Transformers," *International Journal RF and Microwave CAE*, vol. 14, pp. 424-432, 2004.



- [6] Hsu H. M., *et al.*, "Characterization of On-Chip Transformer Using Microwave Technique," *IEEE Transactions on Electron Devices*, vol/issue: 55(3), 2008.
- [7] Biondi T., *et al.*, "Analysis and Modeling of Layout Scaling in Silicon Integrated Stacked Transformers," *IEEE Transactions on Microwave Theory and Techniques*, vol/issue: 54(5), pp. 2203-2210, 2006.
- [8] W. Gao, *et al.*, "Scalable compact circuit model for differential spiral transformers in CMOS RFICs," *Transactions on Electron Devices*, vol/issue: 53(9), pp. 2187-2194, 2006.
- [9] O. E. Gharniti, *et al.*, "Modeling and Characterization of On-Chip Transformers for Silicon RFIC," *IEEE Transactions on Microwave Theory and Techniques*, vol/issue: 55(4), pp. 607-615, 2007.
- [10] Cho M. H., *et al.*, "Design and Analysis of On-Chip Tapered Transformers for Silicon Radio Frequency Integrated Circuits," *Japanese Journal of Applied Physics*, vol/issue: 44(2B), pp. 2166-2170, 2005.
- [11] J. Liu, *et al.*, "An Accurate Compact Model for On-Chip Vertically Coiled Transformers," *IEEE Electron Device Letters*, vol/issue: 34(4), pp. 484-486, 2013.
- [12] Y. Benhadda, *et al.*, "Thermal Behavior of an Integrated Square Spiral Micro Coil," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 14(2), pp. 250-265, 2015.
- [13] Aluigi L., *et al.*, "Midas Automated Approach to Design Microwave Integrated Inductors and Transformers on Silicon," *Radioengineering*, vol/issue: 22(3), pp. 714-723, 2013.
- [14] B. Leite, *et al.*, "An Analytical Broadband Model for Millimeter-Wave Transformers in Silicon Technologies," *IEEE Transactions on Electron Devices*, vol/issue: 59(3), 2012.
- [15] M. Derkaoui, *et al.*, "Design and Modeling of an Integrated MicroTransformer in a Flyback Converter," *TELKOMNIKA*, vol/issue: 11(4), pp. 669-682, 2013.
- [16] Z. Feng, *et al.*, "High-Performance Solenoidal RF Transformers on High-Resistivity Silicon Substrates for 3D Integrated Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol/issue: 60(7), pp. 2066-2072, 2012.
- [17] Zucchelli M., *et al.*, "Dickson Charge Pump Using Integrated Inductors in Complementary Metal–Oxide Semiconductor Ttechnology," *IET Power Electron*, vol/issue: 9(3), pp. 553-558, 2016.
- [18] Chen B., *et al.*, "A semi-analytical extraction method for transformer model," *14<sup>th</sup> International Symposium on Integrated Circuits (ISIC)*. Singapore, pp. 428-431, 2014.
- [19] C. H. Huang, *et al.*, "Optimum Design of Transformer-Type Marchand Balun Using Scalable Integrated Passive Device Technology," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol/issue: 2(8), pp. 1370-1377, 2012.
- [20] Choi Y. S. and Yoon J. B., "Experimental Analysis of the Effect of Metal Thickness on the Quality Factor in Integrated Spiral Inductors for RF ICs," *IEEE Electron Device Letters*, vol/issue: 25(29), pp. 76-79, 2004.
- [21] Chiou H. K., *et al.*, "A 2.6-GHz Fully Integrated CMOS Power Amplifier Using Power-Combining Transformer," *Microwave and Optical Technology Letters*, vol. 52, pp. 299–302, 2010.
- [22] Mayevskiy Y., *et al.*, "A New Compact Model for Monolithic Transformers in Silicon-Based RFICs," *IEEE Wireless Compon Lett.*, vol/issue: 15(6), pp. 419–421, 2005.
- [23] Leite B., *et al.*, "Shielding Structures for Millimeter-Wave Integrated Transformers," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 239-242, 2009.
- [24] M. Y. Bohsali and A. Niknejad, "Microwave Performance of Monolithic Silicon Passive Transformers," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 647-650, 2004.