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Low Common-Mode Gain Instrumentation Amplifier Architecture Insensitive to Resistor Mismatches

Zainul Abidin[1], Koichi Tanno[2], Shota Mago[3], and Hiroki Tamura[4]
[1]Department of Materials and Informatics, University of Miyazaki
[2,3]Department of Electrical and System Engineering, University of Miyazaki
[4]Department of Environmental Robotics, University of Miyazaki

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ABSTRACT

In this paper, an instrumentation amplifier architecture for biological signal is proposed. First stage of conventional instrumentation amplifier architecture was modified by using fully balanced differential difference amplifier and evaluated by using 1P 2M 0.6μm CMOS process. From HSPICE simulation result, lower common-mode voltage can be achieved by proposed instrumentation amplifier architecture. Actual fabrication was done and six chips were evaluated. From the evaluation result, average common-mode gain of proposed instrumentation amplifier architecture is 10.84 dB lower than that of conventional one without requiring well-matched resistors. Therefore, the proposed instrumentation amplifier architecture is suitable for biological signal processing.

Corresponding Author:
Zainul Abidin
Department of Materials and Informatics, University of Miyazaki
1-1, Gakuen Kibanadai Nishi, Miyazaki, 889-2192, Japan
zainulelektro@gmail.com

1. INTRODUCTION

Sensor interface has considerable interests in medical monitoring and health care systems. Design of the sensor interface circuit has to meet some stringent requirements of analog and digital blocks. Biological signals, such as Electroencephalogram (EEG), Electrooculogram (EOG), Electrocardiogram (ECG), and Electromyogram (EMG) are widely used for medical and health care applications and very weak and low frequency signals. The signals amplitude and frequency spans are in the order of μV to mV and from DC to a few kHz, respectively [1]-[4].

In order to acquire and process the biological signals, Instrumentation Amplifier (IA) is often used [5]. Conventional IA architecture shown in Fig. 1a is often employed to achieve high signal-to-noise ratio in first block of sensor interface [6], [7]. It consists of three operational amplifiers. In this kind of IA architecture, low common-mode gain (A_c) is necessary and can be achieved by satisfying well-matched condition of resistors network. However, in actual fabricated chips, resistor mismatch often happens and deteriorates the A_c [7]. In this paper, an IA architecture which its A_c is low and insensitive to resistor mismatches is presented.

2. PROBLEM OF CONVENTIONAL INSTRUMENTATION AMPLIFIER ARCHITECTURE

As mentioned in Chapter 1, the IA architecture shown in Fig.1a requires well-matched resistors ($R_2 = R_3$, $R_4 = R_5$, and $R_6 = R_7$) and the output voltage of conventional IA (V_{outc}) can be determined as follows

$$V_{outc} = \frac{R_7}{R_5}\left(2\frac{R_3}{R_1} + 1\right)(V_{in2} - V_{in1}) \quad (1)$$

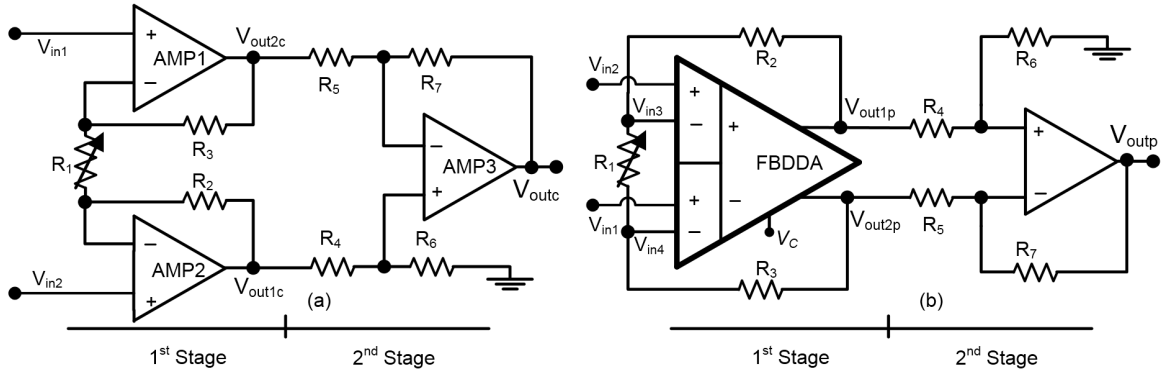


Figure 1. IA architectures: (a) Conventional (b) Proposed

The V_{in1} and V_{in2} are defined as $v_{cm} - v_{dm}$ and $v_{cm} + v_{dm}$, respectively (v_{cm} and v_{dm} are common-mode voltage and differential input, respectively). Defining resistor mismatch of R_i as $R_{i+1}\ (1 + \Delta_{i+1}) \mid i \in \{2, 4, 6\}$, where Δ_{i+1} is mismatch rate of R_{i+1},V_{out1c} and V_{out2c}, which are the output voltages of the first stage, can be given by

$$V_{out1c} = \left\{2\frac{R_3\,(1+\Delta_3)}{R_1} + 1\right\} v_{dm} + v_{cm} \tag{2}$$

$$V_{out2c} = -\left(2\frac{R_3}{R_1} + 1\right) v_{dm} + v_{cm} \tag{3}$$

Inputting the V_{out1c} and V_{out2c} to the second stage, which is the subtractor circuit, V_{outc} becomes

$$V_{outc} = \frac{R_7}{R_5}\left\{2\frac{R_3}{R_1}\,(1 + \alpha + \Delta_3\alpha) + 1 + \alpha\right\} v_{dm} + \frac{R_7}{R_5}\,(\alpha - 1)\,v_{cm} \tag{4}$$

where α is coefficient defined as follows

$$\alpha = \frac{R_5 + R_7}{\frac{R_5(1+\Delta_5)}{1+\Delta_7} + R_7} \tag{5}$$

From the above derivation, the v_{cm} cannot be rejected by the first stage. From Eq. 4, we can find the v_{cm} is amplified due to resistor mismatches of the second stage. Therefore, the resistor mismatches deteriorate the A_c. In this way, the A_c of the conventional IA architecture is sensitive to the resistor mismatches .

3. PROPOSED INSTRUMENTATION AMPLIFIER ARCHITECTURE

Fig. 1b shows the proposed IA architecture. The proposed IA architecture consists of 2 stages; first stage is Fully Balanced Differential Difference Amplifier (FBDDA) with 2 negative feedback resistors and gain-setting resistor modified from [8] and second stage is as same as the conventional one. The FBDDA consists of fully differential gain stage and Common-Mode Feed Back (CMFB) circuit and the output voltages of FBDDA ($V_{out1p,2p}$) can be determined by

$$V_{out1p,2p} = \pm A\{(V_{in2} - V_{in3}) - (V_{in1} - V_{in4})\} \tag{6}$$

where A is the amplification of FBDDA, and should be very large value. Next, theoretical analysis of the proposed IA architecture is presented using the same manner as Chapter 2.

Using (6) and the $V_{in1,2}$ defined in Chapter 2, under the condition of well-matched resistors, the output voltage of proposed IA architecture (V_{outp}) can be derived as same as Eq. 1 (V_{outc}). Otherwise, when resistor mismatches occur, the output voltages of the first stage (V_{out1p} and V_{out2p} shown in Fig. 1b) can be derived as

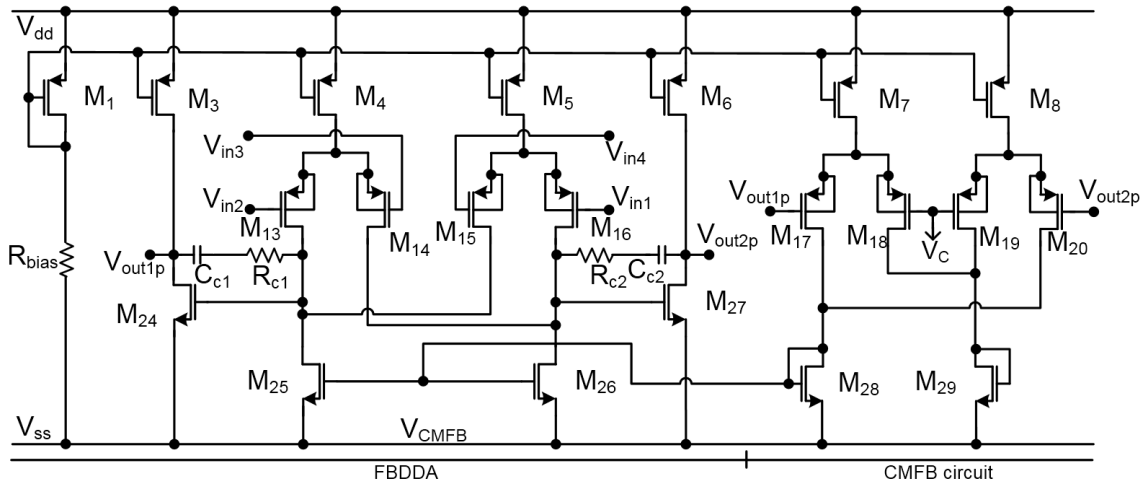


Figure 2. Circuit schematic of FBDDA with CMFB circuit

follow

$$V_{out1p} = \left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\} v_{dm} \quad (7)$$

$$V_{out2p} = -\left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\} v_{dm} \quad (8)$$

Therefore, V_{outp} in consideration of resistor mismatches can be given as follows.

$$V_{outp} = \frac{R_7}{R_5}\left\{\frac{R_3}{R_1}(2+\Delta_3)+1\right\}(1+\alpha)\, v_{dm} \quad (9)$$

From the above derivation, V_{out1p} and V_{out2p} keep the balance as shown in (7) and (8). Theoretically, v_{cm} is rejected perfectly by the first stage. It confirms that in the second stage, v_{cm} is also rejected perfectly as shown in Eq. 9 even the resistor mismatches occur. In this case, low A_c can be achieved by the proposed IA architecture.

Fig. 2 shows the employed FBDDA, which is modified from the reference [8]. The FBDDA consists of fully differential gain stage and common-mode feedback (CMFB) circuit. Two stages amplifier is employed for the fully differential gain stage, therefore, phase compensation circuits (R_{c2}, R_{c3}, C_{c2} and C_{c3}) are added. Furthermore, CMFB circuit is necessary because the FBDDA has differential output. In this design, V_c is set to 0 V. The operational amplifier employed in second stage, which is widely used, is shown in Fig. 3 [9], [10].

4. EVALUATION

In this chapter, simulation result and evaluation of actual fabricated chip are presented. The IA architectures were evaluated using 1P 2M 0.6-μm CMOS process. In order to compare the performance of the IA architectures, Fig. 3 was also employed for AMP1, AMP2, and AMP3 in the conventional IA architecture. In order to evaluate the A_c, the V_{in1} and V_{in2} were supplied by v_{cm} which is represented by sine wave signal with amplitude of 50 mV and frequency of 60 Hz. The resistors network was designed by $R_1 = 51$ kΩ and $R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = 250$ kΩ. Therefore, the ideal total differential gain is 20.7 dB.

4.1. Simulation result

The IA architectures were simulated using HSPICE. The detailed simulation condition is shown in Table 1. Representing resistor mismatches condition ($\pm 3\%$), HSPICE simulation was done under the mismatch rates Δ_5 and Δ_7 are estimated to -3% and 3%, respectively. The resistors R_4 and R_6 become 242.5 kΩ and 257.5 kΩ, respectively. Fig. 4a shows the FFT simulation result of V_{outc} and V_{outp}. At frequency 60Hz, the

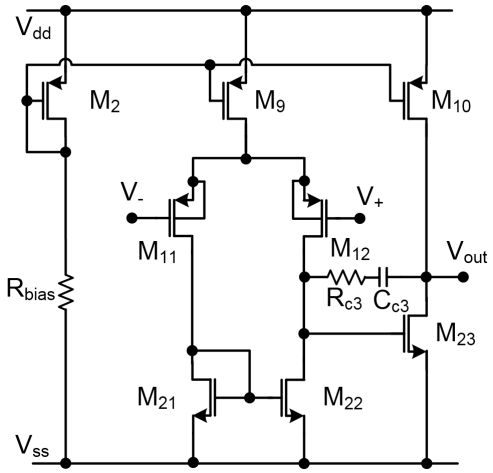


Figure 3. Circuit schematic of an operational amplifier

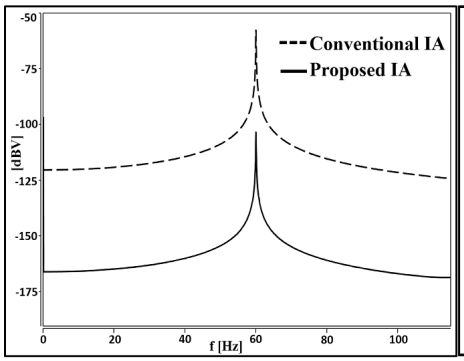
v_{cm} of the conventional and proposed IA architectures reach -57.9 dBV and -103.5 dBV, respectively. The proposed IA architecture has 45.6 dBV lower common-mode voltage than the conventional one.

Monte Carlo simulation was done by 500 times to get data of A_c with deviation of resistor mismatch $\pm 3\%$ ($R_1 \sim R_7$). Fig. 4b shows histogram of A_c. Average A_c of the proposed and conventional IA architectures are -90.6 dB and -44.9 dB, respectively. The average A_c of the proposed IA architecture is lower than that of the conventional one. Lastly, the simulated performance of the IA architectures are listed in Table 2.

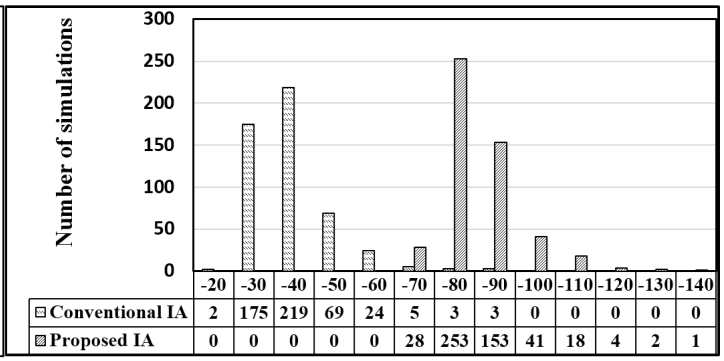
4.2. Chip evaluation

In order to confirm the actual performance, six chips of the IA architectures were fabricated. Fig. 5 shows the microphotograph of the fabricated chip. Due to the number of transistors used in FBDDA, the chip area of the proposed IA architecture is larger than that of the conventional one.

Six chips were evaluated by giving v_{cm} in the form of a sine wave with 100 mV_{p-p} and 60 Hz. Fig. 6 shows FFT measurement result of V_{outc} and V_{outp} of chip no. 3 (see Table 3). At the frequency of 60 Hz, the V_{outp} and V_{outc} reach -88 dBV and -74 dBV, respectively. It indicates that the v_{cm} of V_{outp} 14 dBV lower than that of V_{outc}. Regarding the given v_{cm} value, the A_c of the six chips are calculated and summarized in Table 3. Average A_c of the conventional and proposed IA architectures are -42.8 dB and -53.64 dB, respectively. From these results, under the condition of actual fabrication result (random resistor mismatches), the A_c of the proposed IA architecture is lower than that of the conventional one. The v_{cm} of proposed IA architecture is not perfectly rejected as mentioned in the theoretical analysis because transistor mismatch was



(a)



	-20	-30	-40	-50	-60	-70	-80	-90	-100	-110	-120	-130	-140
Conventional IA	2	175	219	69	24	5	3	3	0	0	0	0	0
Proposed IA	0	0	0	0	0	28	253	153	41	18	4	2	1

(b)

Figure 4. (a) FFT results of V_{outc} and V_{outp} (b) Histogram of A_c (dBV) based on Monte Carlo analysis

Table 1. Simulation Condition

Items	Value
CMOS process	1P 2M 0.6-μm CMOS
V_{dd} [V]	2.5
V_{ss} [V]	-2.5
V_c [V]	0
R_{bias} [kΩ]	295
$M_{1,2}$ [μm/μm]	1.3/2, M = 2
M_{3-10} [μm/μm]	1.3/2, M = 4
M_{11-20} [μm/μm]	16.1/3, M = 2
M_{21-29} [μm/μm]	3.3/2, M = 2
R_{c1-3} [kΩ]	9
C_{c1-4} [pF]	0.5

Note: M means the number of parallel connection

Table 2. Summary of the Simulation Results

Parameters	Conventional IA	Proposed IA
	AC analysis	
Differential gain [dB]	20.7	20.7
-3 dB gain bandwidth [KHz]	254.2	301.6
Power cons. [W]	596.3μ	843.8μ
	Monte Carlo analysis	
Ave. *Ac* [dB]	-44.9	-90.6
	Noise performance (PV)	
Input ref. noise [μV/$\sqrt{Hz}$]	90.4	93.5
Output ref. noise [μV/$\sqrt{Hz}$]	972.4	1000

Note: PV = Peak Value

not considered in this paper. Radiated power supply noise with frequency of 60 Hz is also actual problem.

5. CONCLUSION

In this paper, an IA architecture based on FBDDA has been presented. Resistor mismatch which degrades the performance of conventional IA architecture have been identified and compared in theoretical analysis, simulation and actual chip fabrication. Its ability to achieve low common-mode gain even the resistors are not well-matched makes it suitable as a part of integrated circuit for biological signal processing. As other performance parameters, transistor mismatch effect and offset voltage cancellation are considered as future work.

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REFERENCES

[1] Xiaodan Zou, Xiaoyuan Xu, Libin Yao, and Yong Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067-1077, Apr. 2009.

[2] Jos Hulzink, et al., "An Ultra Low Energy Biomedical Signal Processing System Operating at Near-Threshold". *IEEE Transactions On Biomedical Circuits And Systems*, vol. 5, no. 6, pp. 546-554, Dec. 2011.

[3] Chih-Jen Yen, Wen-Yaw Chung and Mely Chen Chi. "Micro-Power Low Offset Instrumentation Amplifier IC Design For Bio-Medical System Applications". *IEEE Transactions On Circuits And Systems-I: Regular*

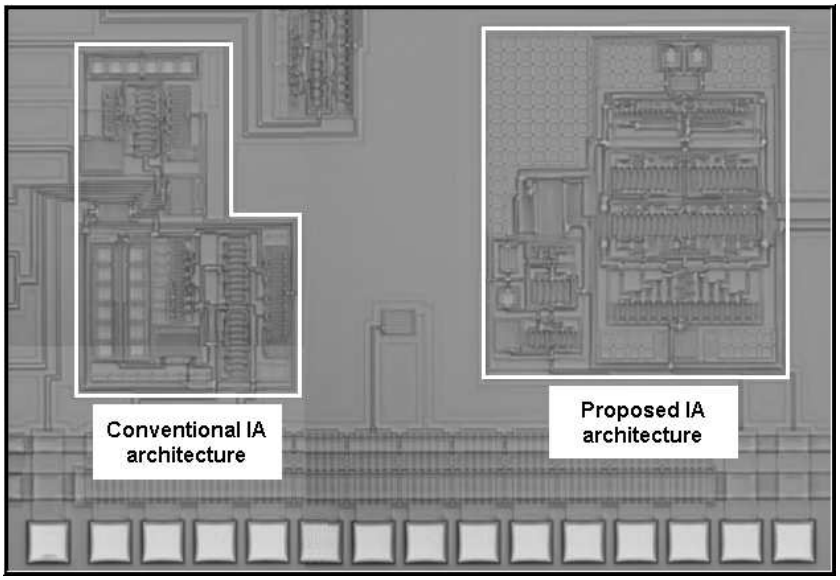


Figure 5. Microphotograph of the IA architectures

Table 3. A_c of the IA Architectures

Chip no.	Conventional (dB)	Proposed (dB)
1	-44.97	-50.97
2	-42.97	-56.97
3	-44.97	-58.97
4	-41.97	-54.97
5	-40.97	-50.97
6	-40.97	-48.97

Papers, vol. 51, no. 4, pp. 691-699, Apr. 2004.

[4] Akshay Goel and Gurmohan Singh, "A Novel Low Noise High Gain CMOS Instrumentation Amplifier for Biomedical Applications," *IAES International Journal of Electrical and Computer Engineering*, vol. 3, no. 4, pp. 516-523, Aug. 2013.

[5] N. V. Helleputte, et al., "A Multi-Parameter Signal-Acquisition SoC for Connected Personal Health Applications", *IEEE International Solid-State Circuits Conference*, pp. 314-315, Febr. 2014.

[6] J. Szynowski, "CMRR analysis of instrumentation amplifiers," *Electronics Letters*, vol. 19, no. 14, pp. 547-549, 1983.

[7] Hwang- Cherng Chow and Jia -Yu Wang, "High CMRR instrumentation amplifier for biomedical application," *Proc. IEEE International Symposium on Signal Processing and Its Applications*, pp. 1-4, Febr. 2007.

[8] A. Hussain and I. Mohammed, " A CMOS fully balanced differential difference amplifier and its applications," *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 48, No. 6, pp. 614-620, June 2001.

[9] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition. Oxford University Press, New York, 2002.

[10] N. Mukahar and S. H. Ruslan, "A 93.36 dB, 161 MHz CMOS Operational Transconductance Amplifier (OTA) for a 16 Bit Pipeline Analog-to-Digital Converter (ADC) ," *IAES International Journal of Electrical and Computer Engineering*, vol. 2, no. 1, pp. 106-111, Feb. 2012.

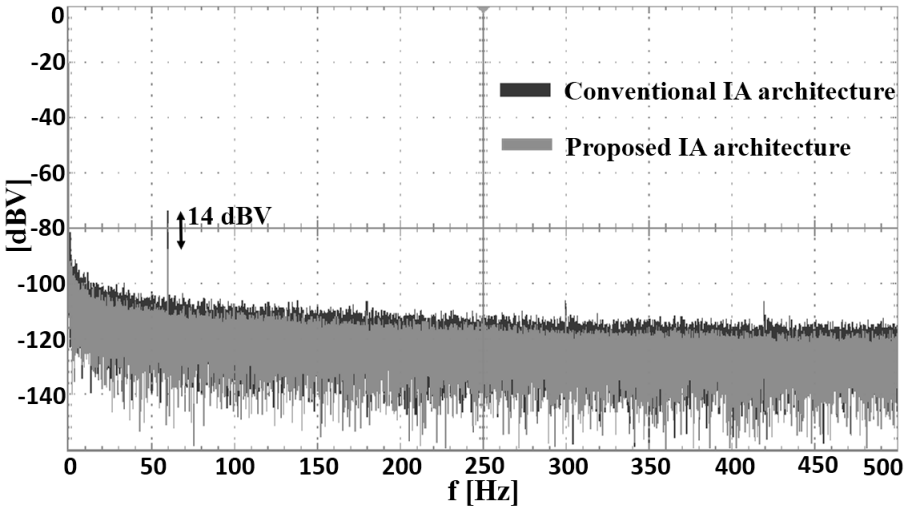
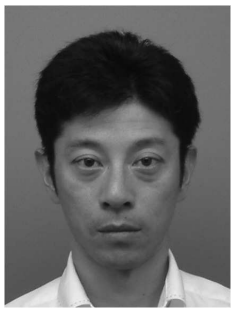


Figure 6. FFT measurement result of chip no. 3 (V_{outc} and V_{outp})

BIOGRAPHIES OF AUTHORS

Zainul Abidin was born in 1986. He received the B. Eng. from University of Brawijaya and M. Eng. from University of Miyazaki in 2008 and 2011, respectively, and is currently working for University of Brawijaya and toward the PhD degree in Department of Materials and Informatics at University of Miyazaki. He has been involved with design of analog integrated circuit since Master Degree. His current research interest includes analog circuit for biological signal processing. He is affiliated with IEEE as student member.



Koichi Tanno was born in Miyazaki, Japan, on April 22, 1967. He received B. E. and M. E. degrees from the Faculty of Engineering, University of Miyazaki, Miyazaki, Japan, in 1990 and 1992, respectively, and Dr. Eng. degree from Graduate School of Science and Technology, Kumamoto University, Kumamoto, Japan, in 1999. From 1992 to 1993, he joined the Microelectronics Products Development Laboratory, Hitachi, Ltd., Yokohama, Japan. He was engaged in research on low-voltage and low-power equalizer for read channel LSI of hard disk drives. In 1994, he joined University of Miyazaki, where he is currently a Professor in the Department of Electrical and Systems Engineering. His main research interests are in analog integrated circuit design and multiple-valued logic circuit design. Dr. Tanno is a member of IEEE and the Executive Subcommittee of the IEEE Computer Society Technical Committee on Multiple-Valued Logic.

Shota Mago was born in 1992. He received the B.Eng from University of Miyazaki in 2015, and is currently studying to get master degree of Electrical and Electronic Engineering at University of Miyazaki. His current research is Analog CMOS Integrated Circuits.

Hiroki Tamura received the B.E and M.E degree from Miyazaki University in 1998 and 2000, respectively. From 2000 to 2001, He was an Engineer in Asahi Kasei Corporation, Japan. In 2001, He joined Toyama University, Toyama, Japan, where He was a Technical Official in Department of Intellectual Information Systems. In 2006, He joined Miyazaki University, Miyazaki, Japan, where He was an Assistant Professor in Department of Electrical and Electronic Engineering. In 2012, He is currently an Associate Professor in the Department of Environmental Robotics. His main research interests are Neural Networks and Optimization Problems. In recent years, He has the interest in Biomedical Signal Processing using Soft Computing.