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Evaluation of Various Digital Controllers for Forward Converter with Active Clamp

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ABSTRACT

This research paper presents the design issues of digital Controllers for Forward Converter with Active Clamp circuit (ACFC). Brief review of Working Principle and mathematical modeling of the converter is first given. The importance of Digital Controllers for forward converter and design procedure is described in detail. And the validity of designed controllers and achievement of desired compensation is verified by the results of implemented digital controllers to Active clamp forward Converter (ACFC). Finally results are analyzed by applying disturbances at both Supply and Load ends of the converter. And the conclusions are made based on obtained results of Voltage Mode Controller (VMC) by comparing with the results of the Current Mode Controller (CMC).

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1. INTRODUCTION

With the continuous advancement of power electronic components such as power MOSFETs and MLCCs, a primary trend is moving towards high operating frequencies, which help in reducing the size and rating of magnetic components such as transformer and filter inductor. Also new design trends require power supplies with low voltages and high currents for Telecom Power Supply; Distributed Power supply Circuits etc. Forward converter is a promising topology for low and medium power applications where low voltages at high currents are required with higher efficiency [1-7]. Forward converter with active clamp is shown in Figure 1.

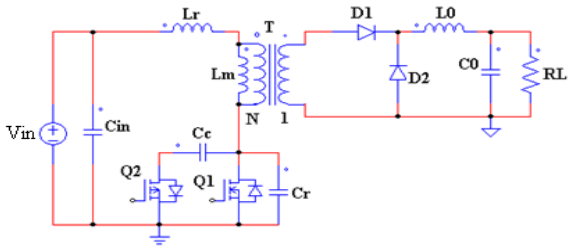

Figure 1. Forward Converter with Active Clamp

A Controller is required to get better performance from the converter. With the advance of microcontrollers/DSP, digital control is increasingly used in various applications of switch mode power converter systems. Digital control offers a number of advantages over analog control i.e high level of accuracy; it is easier to implement computational functions, more flexible in modifying the code for various applications, low cost and less sensitive to noise. The disadvantages, however, include sampling delay, limited computational power and control loop bandwidth. Nevertheless, as the price/performance ratio of digital processors continues to decline, digital controllers are becoming a viable and competitive option, especially in high end switching converter applications [8-9]. In [10], [15] some efforts have been made to improve the performance of the converter by designing analog controllers but no one is discussed regarding the design of digital controller for an ACFC eventhough it has more advantages.

The Main Objective of this Paper is to present design issues of digital controllers for isolated DC-DC Converter and to verify the validity of the designed controllers by applying disturbances. In Section 2, an outline of the Working Principle of the Converter is presented. Mathematical Modeling of the ACFC is presented in Section 3. Design procedure of the digital controllers for considered converter is presented in Section 4. In Section 5 Simulation Results and discussions are presented and finally, the conclusions are made about the designed controllers and is presented in Section 6.

2. PRINCIPLE OF OPERATION ACFC

The Brief review about the principle of operation [2] of the considered converter is presented by considering two states of the converter.

2.1. Power Transfer State

During this state power is transferred to secondary as the MOSFET, Q_1 is turned on at t_0, the current ramps up in the magnetizing inductor. The secondary diode D_1 conducts and D_2 is blocked as shown in Figure 2. The lump capacitor C_r is discharged and V_{DS} of Q_1 is almost zero. The leakage inductor is crossed by the reflected output inductor current which peaks to I_m plus Is/N as shown in Figure 2

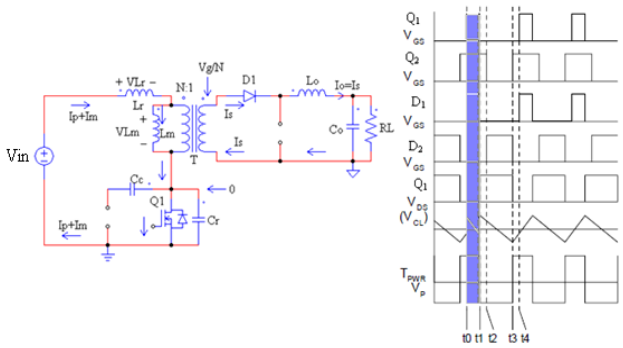

Figure 2. ACFC During on State of Main Mosfet

2.2. Active Clamp State

This is the active clamp state where the transformer primary is reset. Although the schematic of Figure 3 shows an immediate reversal of the primary current, the transition from positive to negative current flow is actually smooth and had really began during the previous state when the magnetizing current had reached its maximum positive peak value. On the primary side, Q_2 is now fully turned-on as the difference between the input V_{in} and the clamp capacitor voltage is now applied across the transformer primary. Q_2 is subject to minimal conduction loss as only the magnetizing current is flowing through the channel resistance. Conversely, on the secondary side, D_2 is carrying the full load current through its channel resistance and is experiencing high conduction loss.

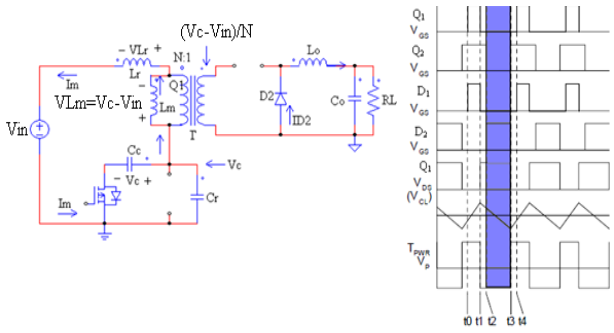

Figure 3. ACFC During off State of Main Mosfet

3. MATHEMATICAL MODELLING OF THE CONVERTER

To observe the behavior of the converter mathematical model of the converter is required. State space averaging is the most common technique to represent physical phenomena into mathematical form and is used here to model the ACFC. In deriving the state space model, the leakage inductance of the transformer $L_{r.}$ and the parasitic capacitance of the main switch, C_r are neglected [8-12]. It is assumed that the small letters denotes the time varying quantities, capital letters denote DC quantities and small letters with hat denotes small ac perturbations. Also, it is assumed that the converter is operating in continuous current mode. In continuous current mode (CCM) only two modes exist, i.e. when the power switches Q_1 is ON & Q_2 is OFF when switches Q_1 is OFF & Q_2 is ON and same has been shown in Figure 2 and in Figure 3. In order to examine the effect of load changes on the response of the converter, a current generator i_z is added in parallel with the load resistor. State Space Model of the converter is designed by considering the Magnetizing Current 'i_m', clamp capacitor voltage 'v_c', inductor current 'i' and the output voltage 'v' are the four elements of a state vector x, while the input vector u has v_{in} and i_z and by taking weighted average of two states of the converter. The state –space averaged model of the converter is

$$\dot{X} = Ax + Bu$$
$$Y = Cx \qquad \text{Where A= d } A_{ON} + (1\text{- d) } A_{OFF}\text{ ; B= d } B_{ON} + (1 - \text{d) } B_{OFF} \tag{1}$$

We now perturb and linearize the converter wave form this quiescent operating point: Each variable is written as a sum of steady state or DC component and small signal or AC component as

$$x = X + \hat{x}; u = U + \hat{u};\ d = D + \hat{d}$$
$$\text{Where} \hat{x} \ll X; \hat{u} \ll U; \hat{d} \ll D \tag{2}$$

Substituting Equation 2 in Equation 1 and neglecting the higher order terms, the Equation which relates small changes in variables i.

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + (A_{on} - A_{off})\hat{d}X + (B_{on} - B_{off})\hat{d}U$$
$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + E\hat{d} \quad Where\ E = (A_{on} - A_{off})X + (B_{on} - B_{off})U \tag{3}$$

From the above Equation (3), we obtain StateMatrices foe the considered converter are,

$$A = \begin{bmatrix} 0 & -\frac{(1-D)}{L_m} & 0 & 0 \\ \frac{(1-D)}{C_C} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_O} \\ 0 & 0 & \frac{1}{C_O} & \frac{1}{RC_O} \end{bmatrix}; B = \begin{bmatrix} \frac{1}{L_O} & 0 \\ 0 & 0 \\ \frac{D}{NL_O} & 0 \\ 0 & \frac{1}{C_O} \end{bmatrix}; E = \begin{bmatrix} \frac{V_g}{L_m} \\ 0 \\ \frac{V_g}{NL_O} \\ 0 \end{bmatrix}; C = [1\ 0\ 0\ 0] \tag{4}$$

4. CONTROLLER DESIGN

A controller is required to get desired performance of the converter. There are different types of the controllers available depends up on the sensing signals and, most commonly used controller is PI controller

because of its simplicity. But the main drawback of analog controller is total circuitry is need to be changed to replace a compensator and due to rapid development in the Micro controllers and DSPs, digital controllers are becoming a viable one because of in a single chip we are able to develop different types of controller as per the requirement [13-14]. Before designing a controller Performance of the converter is need to be observed by using parameters of the converter, Parameters of the converter are calculated by assuming required specifications. The designed parameters of the converter are shown in table1.

Table 1. Parameters of ACFC

Parameter	Symbol	Typical
Input Voltage	Vin	48V
Output Voltage	V_0	5V
Duty Cycle	D	0.35-0.7
Full Load Efficiency	η	90%
Output Load Current	I_0	20A
Switching Frequency	F_s	100KHz
Output Filter components	Lo & Co	8µH & 590µF
Magnetizing Inductance & Clamp capacitor	Lm & Cc	100µH& 100nF

From the frequency response it is observed that the converter having low phase margin10.7degree at 11.1 KHz. To improve phase margin to 60 degrees and to attain a crossover frequency of f_c=20 kHz a compensator is required. Different methods are available to design a controller for Switching Converter.

4.1. Continuous-Time Controller

From the frequency response of ACFC without compensator, it is observed that uncompensated loop gain has a magnitude at 20 KHz of approximately -10.6 dB. So to obtain unity gain at 20 kHz the compensator should have a gain of +10.6dB. To improve the phase margin a PD compensator is needed.
The dc gain is given by $T_{uo} = \frac{HV}{DV_m}$=4

$$f_p = 20KHz\sqrt{\frac{1+sin60}{1-sin60}} = 74.641kHz; f_z = 20KHz\sqrt{\frac{1-sin60}{1+sin60}} = 5.3589kHz \quad (5)$$

To obtain a compensator gain of 10.6 dB the low frequency compensator gain must be

$$G_{co} = (\frac{f_c}{f_o})^2 \frac{1}{T_{uo}}\sqrt{\frac{f_z}{f_p}} = 1.2797 \quad (6)$$

The transfer function of PD compensator is:

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_p})}{(1+\frac{s}{w_z})} = \frac{8.294e{-}5s{+}1.28}{9.771e{-}7s{+}1} \quad (7)$$

Even though the transient response of the system improves there is steady state error. The low frequency regulation can be further improved by addition of an inverted zero. By introducing the zero at 2000Hz which is one tenth of crossover frequency the steady state error can be reduced. The transfer function of PI compensator is$\frac{s+2000}{s}$. The total transfer function of the PID compensator is given according to the Equation

$$G_c(s) = \frac{8.294e{-}005s^2{+}3.552s{+}6773}{2.586e{-}6s^2{+}s} \quad (8)$$

By simulating the considered converter in the MATLAB Software it is observed that required phase margin and zero volt switching is achieved with the help of designed controller. Figure 4 Shows output voltage wave form of the converter with Continuous time PID Controller.

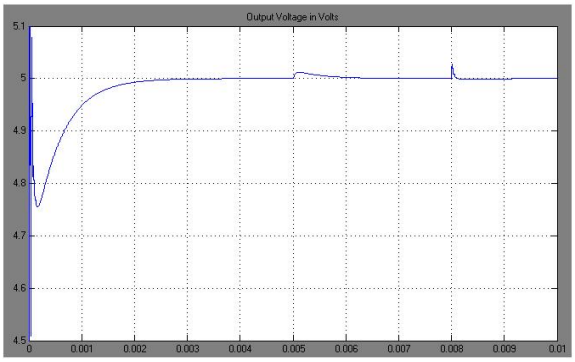

Figure 4. Output Voltage Waveform of ACFC with PID Compensator

4.2. Discrete-Time Controller

There are different methods available to design digital controllers for a switching converter. The available methods to design digital controllers are (i) Digital Redesign Method and (ii) Direct Digital design Method [8].

4.2.1. Digital Redesign Method

In this method, first controller is designed in continuous –time with the help generalized procedure and then designed controller is transformed into digital form to achieve to get desired performance from the converter. To tranform the continuous-time controller into digital form different techniques are available. Table 2 shows the transformation methods and associated Equations to discretize continuous time model into digital form.

Table 2. Discretization Methods

Discretization Method	Z- domain
Tustin Method	$z = \frac{1 + s\frac{Ts}{2}}{1 - s\frac{Ts}{2}}$
Zero Order Hold Method	u(t)=u[k] kTs≤k≤(k+1)ts
First Order Hold method	u(t)= u[k]+$\frac{t-kTs}{Ts}(u[k+1]-u[k]$
Matched Pole Zero Method	Z=e^{sT}

Tustin Method transforms the whole left half plane of the s-domain into the inside unit circle of z-domain. The ZOH device generates a continuous input signal u (t) by holding each sample value u [k] constant over one sample period. First-order hold (FOH) differs from ZOH by the underlying hold mechanism. To turn the input samples u [k] into u (t) a continuous input, FOH uses linear interpolation between samples. This method is generally more accurate than ZOH for systems driven by smooth inputs.Matched pole zero method preserves the pole zero location but there is an aliasing effect in this method. And this method gives almost similar results of Tustin approximation.With the help of above transformation methods, the designed continuous time controller (8) is transformed into digital form by considering the sampling frequency 5e-6 Hz and the obtained digital controllers are as follows,

$$\text{Tustin Method} = \frac{18.06z^2 - 32.6z + 14.57}{z^2 - 1.017z + 0.01691} \quad (9)$$

$$\text{Zero order hold Method} = \frac{32.07z^2 - 61.09z + 29.04}{z^2 - 1.145z + 0.01446} \quad (10)$$

$$\text{First order Hold Method} = \frac{16.18z^2 - 29.28z + 13.13}{z^2 - 1.145z + 0.01446} \quad (11)$$

$$\text{Matched Pole Zero Method} = \frac{15.98z^2 - 28.84z + 12.9}{z^2 - 1.145z + 0.01446} \quad (12)$$

With the help of above transfer functions of digital controllers, considered converter is simulated in MATLAB software. Figure 5 shows the Simulink model of ACFC with Discrete time controller and Figure 6 represents a variation of output waveform with different types of digital controllers.

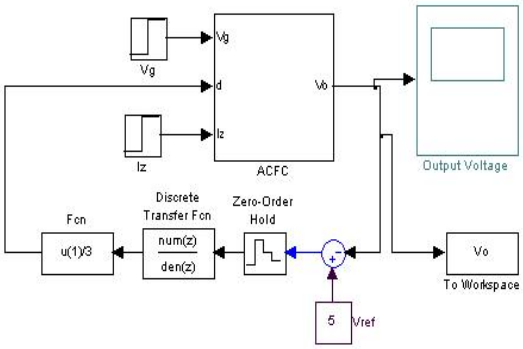

Figure 5. Simulink Model of ACFC with Discrete-time PID Compensator

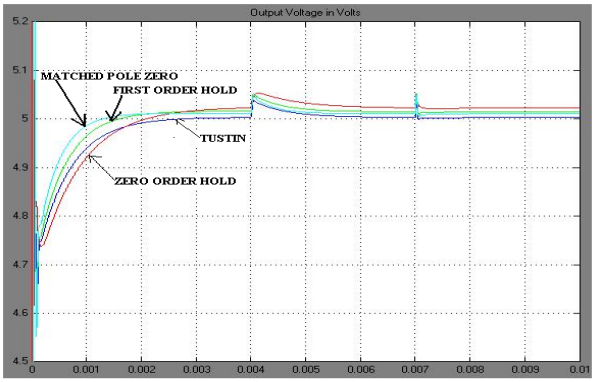

Figure 6. Variation of Output voltage waveform of ACFC with Discrete-time PID Compensators

4.2.2. Direct Digital Design Method

To design a digital controller by direct digital design method, first, it needs to transform continuous-time model of ACFC into Discrete time Model [14] and then need to design a digital controller directly in the digital domain by using matched pole zero method. With the help of matched pole-zero method continuous model of ACFC is transformed in to digital form.The Discrete-time Transfer functions of ACFC are shown in (13-18).

$$G_{vg}(z) = \frac{0.00027112(z+1)}{z^2 - 1.961z + 0.9667} \quad (13)$$

$$G_{ig}(z) = \frac{0.065(z-0.9667)}{z^2 - 1.961z + 0.9667} \quad (14)$$

$$G_{img}(z) = \frac{0.0489(z-1)}{z^2 - 1.208z + 1} \quad (15)$$

$$G_{vd}(z) = \frac{0.0312(z+1)}{z^2 - 1.961z + 0.9667} \quad (16)$$

$$G_{id}(z) = \frac{7.4967(z-0.9667)}{z^2 - 1.961z + 0.9667} \quad (17)$$

$$G_{imd}(z) = \frac{3.8263(z-1)}{z^2 - 0.71z + 1} \quad (18)$$

The designed discrete-time model of ACFC is very suitable to design the digital controller directly by using Root locus technique. From the root locus of converter, it is observed that the poles are located at 0.966+/-0.0896i.which are very nearer to the unit circle, it indicates that the system is very nearer to the conditional stability. Now by using pole placement technique a digital PID controller is designed to improve the stability limit and Phase margin of the converter by locating the zeros at Z=0.99,0.9717 and poles at Z=1,0.7214. Figure 7 represents the output voltage waveform of ACFC with digital controller designed by direct digital design method.The designed digital controller is represented by (19).

$$G_{imd}(z) = \frac{1.3424(z-0.99)(z-0.9717)}{(z-1)(z-0.7214)} \quad (19)$$

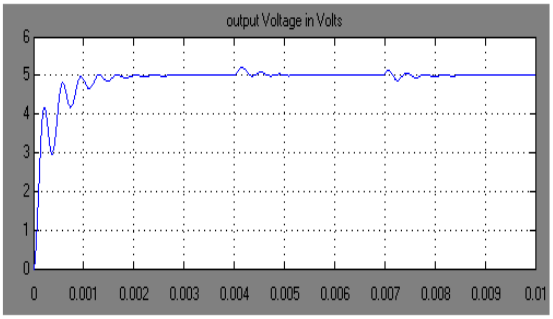

Figure 7. Output Voltage Waveform of ACFC with Direct Digital Design Compensator

4.3. Two-Loop Controller

From the above results, it is observed that we are able to get zero voltage regulation but again to improve performance of the converter two loop controllers are required [15-17]. Authors are presented a paper [15] to design a two loop controller for Forward Converter with the active clamp circuit. With the help of mathematical analysis presented in [15] and by using above discretizing methods a two loop controller is designed. And the corresponding Equations are as follows:

$$G_i(z) = \frac{0.4365z^2 + 0.02523Z - 0.4112}{Z^2 - 1.119Z + 0.119} \tag{20}$$

$$G_c(z) = \frac{-4.537e5\ Z + 4.402e5}{Z - 0.5073} \tag{21}$$

And by considering the slopes of sensed voltage and current signal duty cycle Equation is derived and in shown in Equation (22):

$$\hat{d} = \frac{1}{K}\left(\frac{\widehat{v_C}}{v_g} - \frac{\widehat{i_o}}{N} + \frac{DT}{2L_o}\widehat{v_o} + \left(\frac{1}{NL_o} + \frac{1}{L_m}\right)\frac{DT}{2}\widehat{v_g} - i_m D\right) \tag{22}$$

where $K = \left(\frac{M_1}{2} + M_o\right)T$

And the duty cycle Equation is split into different parts,

$$F_M = \frac{1}{K}; F_i = \frac{1}{N}; F_v = \frac{DT}{2L_o}; F_{im} = D; F_S = \left(\frac{1}{NL_o} + \frac{1}{L_m}\right)\frac{DT}{2} \tag{23}$$

Now with the help of complete small signal model block diagram of Active Clamp Forward Converter (ACFC) with Average Current Mode Control (ACMC) is shown in Figure 8. And is simulated in MATLAB software corresponding results are shown in Figure 9. It represents output voltage waveform of ACFC with Discrete –time two-loop controller.

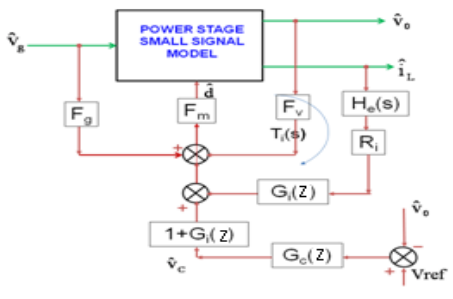

Figure 8. Block Digram Representation of ACFC with Two-Loop Controller

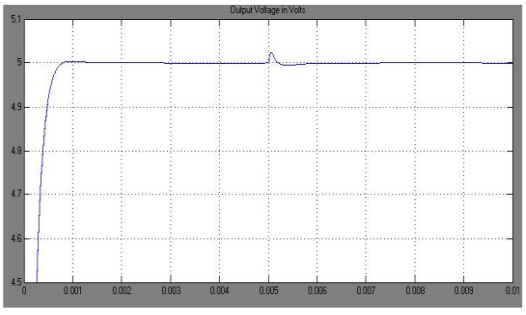

Figure 9. Output Voltage Waveform of ACFC with Two-Loop Controller

5. RESULTS AND DISCUSSION

From the obtained results, it is observed that the zero voltage regulation is achieved by the designed controllers. The comparative output wave forms of digital redesign method represent the Tustin method is giving the more accurate approximation for the continuous-time controllers and to design a digital controller by direct digital design method matched pole zero method is preferable. To analyze the performance of the designed controllers disturbance is applied at both ends of the converter. A line step change of 5V is applied and 50% of load step change is applied. By analyzing the performance and in implementation point of view as compared to continuous –time controller's digital controllers are preferable. As compared to the single loop controller, two loop controllers giving better performance. And it is observed that single loop controller has some drawbacks, i.e. any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slower response. The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation. Compensation is further complicated by the fact that the loop gain varies with input voltage. And the two loop controller has the advantages of simpler dynamics, robust wide bandwidth output voltage control, inherent protection against excessive switch currents on a cycle by cycle basis and transformer saturation problem is reduced/eliminated

6. CONCLUSION

This paper presents the step-by-step design procedure to design digital controllers for an Active Clamp Forward Converter (ACFC). By comparing the obtained results of the designed controllers bilinear transformation is recommended to design a discrete-time controller by a digital redesign method and the Pole zero matching method is preferred to design a digital controller by the direct digital design method. To get better performance from the converter two loop controller is designed and results are confirmed that as compared to single loop controller two-loop controller giving better performance. Finally Simulation results are presented for a 48V input ACFC. The validity of the designed digital controller is confirmed by the Simulation results by applying disturbances at load end as well as at the supply end.

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