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The Impact of Tunneling on the Subthreshold Swing in Sub-20 nm Asymmetric Double Gate MOSFETs

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ABSTRACT

This paper analyzes the subthreshold swing in asymmetric double gate MOSFETs with sub-20 nm channel lengths. The analysis of the carrier transport in the subthreshold region of these nano scaled MOSFET includes tunneling as an important additional mechanism to the thermionic emission. It is found that the subthreshold swing is increasing due to tunneling current and that the performance of nano scaled MOSFETs is degraded. The degradation of the subthreshold swing due to tunneling is quantified using analytical potential distribution and Wentzel–Kramers–Brillouin (WKB) approximation in this paper. This analytical approach is verified by two dimensional simulations. It is shown that the degradation of subthreshold swing increases with both reduction of channel length and increase of channel thickness. We also show that the subthreshold swing is increasing in case of different top and bottom gate oxide thicknesses.

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1. INTRODUCTION

Scaling down of silicon devices is continuing in the effort to improve the performance of integrated circuits, in particular related to operating speed and power consumption. The conventional MOSFET structure in CMOS integrated circuits is not suitable for nano-scaled channel lengths because of serious short channel effects (SCEs) such as the subthreshold swing (SS) degradation, the threshold voltage shift, and drain induced barrier lowering (DIBL). The multiple gate MOSFET, which has the several gates around channel to improve the controllability of carriers in channel [1, 2], was developed to solve these problems.

The double gate (DG) MOSFET, the simplest structure among the multiple gate MOSFETs, is of great importance [3, 4, 5]. In this paper, the subthreshold swing (SS) is investigated for sub-20 nm asymmetric DGMOSFETs, having different top and bottom gate structures. Because the tunneling current cannot be ignored in MOSFETs with sub-20 nm channel lengths, the thermionic and tunneling currents have to be included when analyzing the carrier transport. The study in this paper is focused on the degradation of SS due to tunneling current for sub-20 nm asymmetric DGMOSFETs. To obtain subthreshold swing model, we use the potential model of Ding et al., [6] and the tunneling probability derived from the Wentzel-Kramers-Brillouin (WKB) approximation.

Section 2 shows the potential distribution and subthreshold swing model of asymmetric DGMOSFET. Section 3 describes the channel-dimension-dependent subthreshold swing with the top and bottom oxide thicknesses as the relevant parameters. Section 4 presents our conclusions.

2. THE POTENTIAL DISTRIBUTION AND SUBTHRESHOLD SWING MODEL FOR ASYMMETRIC DOUBLE GATE MOSFET

Figure 1 shows the cross-sectional diagram of an asymmetric DGMOSFET. As can be seen from the labels in the Figure, the top (t_{ox1}) and the bottom (t_{ox2}) gate oxide thicknesses can have different values due to different fabrication steps. First, Poisson equation has to be solved.

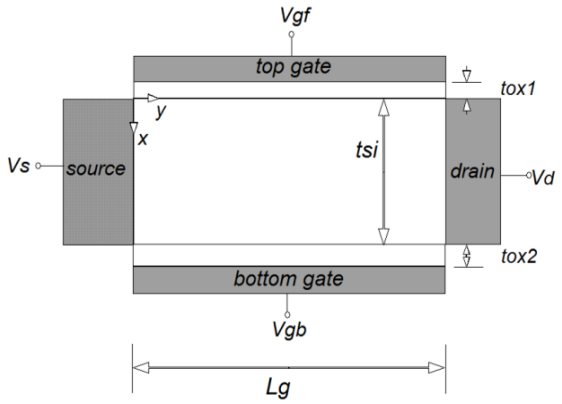


Figure 1. Schematic Cross-Sectional Diagram of Asymmetric DGMOSFET

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \tag{1}$$

In Equation (1) ε_{si} is the permittivity of silicon and N_a is the doping concentration in the channel. The boundary conditions of Ding et al. are used to solve Equation (1). The subthreshold swing model for the subthreshold current consists of thermionic and tunneling currents:

$$\mathrm{SS}=\left[\frac{\partial\log(I_{total})}{\partial V_{gf}}\right]^{-1}=\left[\frac{\ln(10)\times I_{total}}{\frac{\partial I_{ther}}{\partial V_{gf}}+\frac{\partial I_{tunn}}{\partial V_{gf}}}\right] \tag{2}$$

where I_{ther} is the thermionic current, I_{tunn} is the tunneling current, and I_{total} is the sum of thermionic and tunneling currents. We use the potential model of Ding et al. and the WKB approximation, to obtain the SS of sub-20 nm asymmetric DGMOSFET, to be expressed as Equation (2) in accordance with channel length and thickness with parameters of top and bottom oxide thicknesses.

The first derivative of the thermionic current for the top-gate voltage is

$$\begin{aligned}\frac{\partial I_{ther}}{\partial V_{gf}}&=\frac{\partial\left(\frac{qn_{min}(x)v_{th}t_{si}W}{6}\right)}{\partial V_{gf}}=\left(\frac{qv_{th}t_{si}W}{6}\right)\left(\frac{\partial n_{min}(x)}{\partial V_{gf}}\right)\\&=\left(\frac{qv_{th}t_{si}W}{6}\right)n_{min}(x)\left(\frac{1}{V_T}\right)\left(\frac{\partial\varphi_{min}(x)}{\partial V_{gf}}\right)\end{aligned} \tag{3}$$

The $n_{min}(x)$ is $(n_i^2/N_a)\exp(\varphi_{min}/V_T)$ by the Boltzmann distribution, where n_i is the intrinsic electron concentration, k is the Boltzmann constant, V_T is the thermal voltage, and φ_{min} is the minimum channel potential to be found from the condition $\partial\varphi/\partial y=0$ with $\varphi(x,y)$ derived from Equation (1). The effective current path x_{eff} [7] is substituted for x in Equation (3). The $\partial\varphi_{min}(x)/\partial V_{gs}$ is according to reference [6]. The first derivative of tunneling current for the top gate voltage is

$$\frac{\partial I_{tunn}}{\partial V_{gf}}=\left(\frac{qN_dt_{si}W}{6}\right)\left(\frac{2v_{tht}}{3}\frac{\partial T_t}{\partial V_{gf}}+\frac{v_{thl}}{3}\frac{\partial T_l}{\partial V_{gf}}\right) \tag{4}$$

$$T_{t,l}=exp\left[-2\int_{y_1}^{y_2}\left|\sqrt{\frac{2m_{t,l}[q\varphi(x_{eff},y)-E_{fm}]}{\left(h/2\pi\right)^2}}\right|dy\right] \tag{5}$$

T_t and T_l are the tunneling probability for electrons with transverse effective mass m_t and longitudinal m_l, respectively, derived from Equation (5), v_{tht} and v_{thl} are the transverse and longitudinal electron velocities, and N_d is the doping concentration in the source and drain. The y_1 and y_2 are points where the potential energy is equal to the Fermi level E_{fm} at end of the source and drain, and h is Planck constant. The SS of sub-20 nm asymmetric DGMOSFET, defined by Equation (2), is investigated with respect to the channel length and thickness, and the top and bottom oxide thicknesses as the parameters.

3. CHANNEL-DIMENSION-DEPENDENT SUBTHRESHOLD SWINGS OF ASYMMETRIC DGMOSFET

Figure 2 shows the variation of SSs as a function of channel length in the sub-20 nm region for t_{si}=1.5 nm, t_{ox1}=t_{ox2}=1.5 nm, N_a=$10^{16}cm^{-3}$, and V_{af}=V_{ab}=0.1 V. The SSs of the proposed model agree well with 2D numerical simulation [8], as shown in Figure 2. The degradation of SS is larger for shorter channels due to short-channel effects. Comparing SSs with and without tunneling current in the range of sub-10 nm, it can be seen that SSs with the tunneling current are larger than those without tunneling because tunneling current becomes more significant when the channel length is shorter. The SSs with and without tunnelling are similar for the channel lengths above 10 nm because the thermionic current is dominant in this region. The inset in Figure 2 shows the variation of potential energy as a function of channel length. Even though the reduction of the maximum of potential energy for smaller channel lengths causes an increase in thermionic current, we observe that the increase in tunneling current due to decreases width of the potential energy is dominant under 10 nm of channel length. Figure 2 shows the degradation of SSs by increase of subthreshold current in the subthreshold region due to the domination of tunneling current.

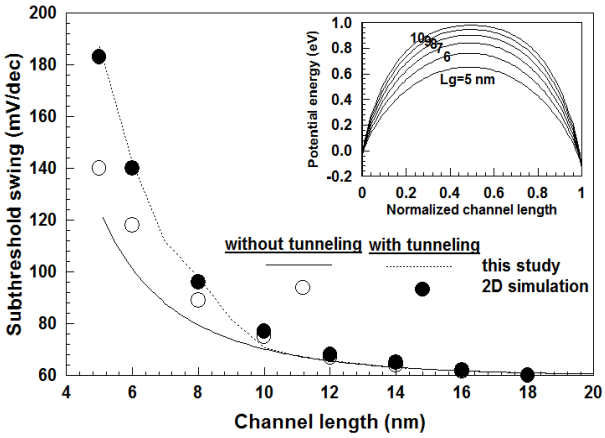


Figure 2. Comparison of SSs Obtained by 2D simulation [8] and this Study for Asymmetric DGMOSFETs

Asymmetric DGMOSFET can be fabricated with different top and bottom oxide thicknesses. Figure 3 shows SSs as a function of channel length in the case of equal and different thicknesses of the top and the bottom oxide. It can be seen that the asymmetric DGMOSFETs show larger SSs than those with the symmetric structure. It can also be seen in Figure 3 that SSs increase with increase of channel thickness, regardless of existence of tunneling current. The smaller channel thickness does not show a large difference for SSs between the symmetric and asymmetric structures, whereas a smaller channel length causes larger difference for SSs between symmetric and asymmetric DGMOSFET due to SCEs.

Figure 4 shows the contours of SSs for channel length and thickness with the top and bottom oxide thicknesses as the parameters. The SSs for the symmetric DGMOSFETs are smaller than those for asymmetric DGMOSFETs. The variation of SSs is significant in the case of SSs without tunneling current, but SSs of symmetric and asymmetric DGMOSFET is nearly equal regardless of the inclusion of tunneling current for channel lengths above 10 nm. The SSs increase in the region of small channel lengths. As can be seen in Figure 4a, it appears that SSs for small channel lengths can be reduced by a reduction in channel thickness. However, this is only the case if the tunnelling current is not included in the calculation. Figure 4b shows that the inclusion of tunnelling current leads to SS values that are almost independent of the channel thickness when the channel lengths are very small. Furthermore, there is no longer a difference between SSs

in the cases of symmetric and assymetric DGMOSFETs. These effects are due to the dominance of tunnelling current at very small channel lengths.

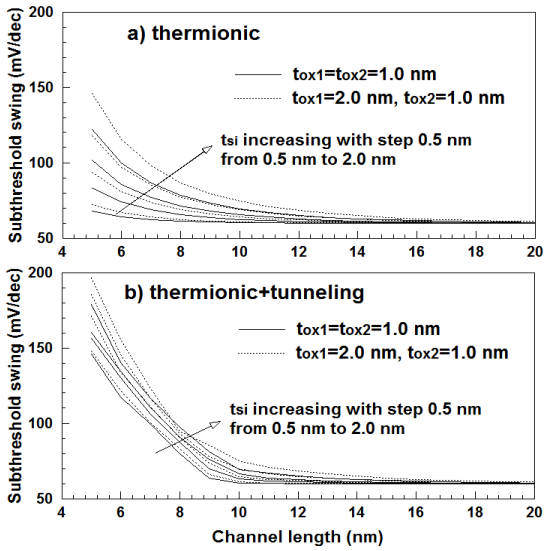


Figure 3. Subthreshold Swings as Functions of Channel Length with Channel Thickness as a Parameter

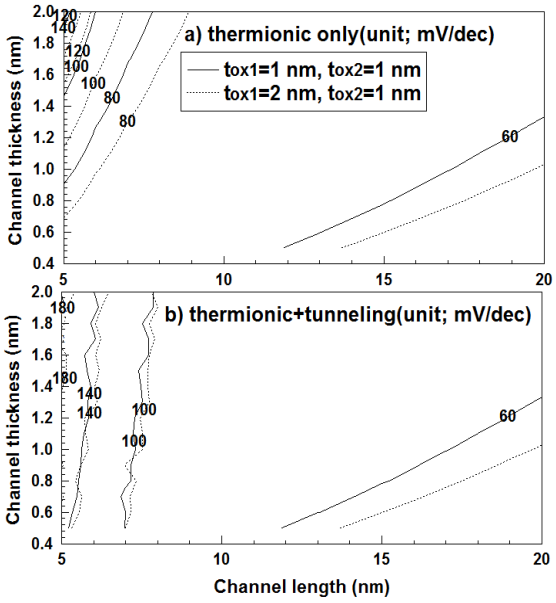


Figure 4. Subthreshold-Swing Contours for Channel Length and Thickness, with the Top and Bottom Oxide Thicknesses as Parameters.

4. CONCLUSION

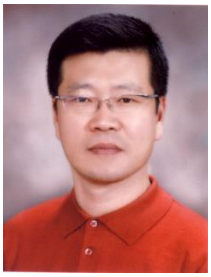
A model for analyzing SSs of sub-20 nm asymmetric DGMOSFETs including tunneling current is proposed in this paper. The SSs obtained by this model have been compared to 2D numerical simulations to verify the model. The model of Ding et al. for thermionic current and WKB approximation for tunneling current are used in the subthreshold region of asymmetric DGMOSFET with channel lengths below 20 nm. Comparing DGMOSFETs with symmetric and asymmetric structures, the SSs of symmetric DGMOSFETs are lower than those of asymmetric. The thicker channel thickness is, the larger SSs becomes in the case of

both symmetric and asymmetric structures. The results show that, in the case of included tunneling current, SSs are more dependent on channel length than thickness in the region of channel lengths below 10 nm.

REFERENCES

[1] T. Nagumo and T. Hiramoto, "Design Guideline of Multi-Gate MOSFETs with Substrate-Bias Conrol", *IEEE Trans. Electron Devices*, vol. 53, pp. 3025-3031, 2006.
[2] J. Nam, C. Kang, K. Kim, H. Yeo, B. Lee, S. Seo and J. Yang, "Influence of Ionizing Radiation on Short-Channel Effects in Low-Doped Multi-Gate MOSFETs", *IEEE Trans. Nuclear Science*, vol.59, pp. 3021-2026, 2012.
[3] T. Bentricia, F. Djeffal, E. Chebaki and D. Arar, "Impact of the drain and source extentions on nanoscale Double-Gate Junctionless MOSFET analog and RF performances", *Materials Science in Semiconductor Processing*, vol. 42, pp. 264-267, 2016.
[4] M. Chanda, S. De and C.K. Sarkar, "Modeling of characteristic parameters for nano-scale junctionless double gate MOSFET considering quantum mechanical effect", *J. Comput. Electron*, vol. 14, pp. 262-269, 2015.
[5] S. F. Najam, M.L.P. Tan and Y.S. Yu, "General SPICE Modeling Procedure for Double-Gate Tunnel Field-Effect Transistors", *J. Inf. Commun. Converg. Eng.*, vol. 14, no. 2, pp. 115-121, 2016.
[6] Z. Ding, G. Hu, J. Gu, R. Liu, L. Wang and T. Tang, "An analytical model for channel potential and subthreshold swing of the symmetric and asymmetric double-gate MOSFETs", *Microelectronics J.*, vol. 42, pp. 515-519, 2011.
[7] S. Dubey, P.K. Tiwari and S. Jit, "A two-dimensional model for the subthreshold swing of short-channel double-gate metal-oxide-semiconductor field effect transistors with a vertical Gaussian-like doing profile", *J. of Applied Physics*, vol. 109, p. 054508, 2011.
[8] D. Munteanu and J.L. Autran, "Two-dimensional modeling of quantum ballistic transport in ultimate double-gate SOI devices", *Solid State Electron.*, vol.47, pp. 1219-1225, 2003.

BIOGRAPHIES OF AUTHORS



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