# FPGA Hardware Realization: Addition of Two Digital Signals Based on Walsh Transforms

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| Article Info | ABSTRACT |
|---|---|
| | This paper presents hardware realization of an addition of two digital signals based on Walsh transforms and inverse Walsh transforms targeted to the Xilinx FPGA Spartan 3 board. The realization utilizes Walsh Transform to convert the input data to the frequency domain and the inverse Walsh transform to reconvert the data from the frequency domain. The designed system is capable of performing addition, subtraction, multiplication and Arbitrary Waveform Generation (AWG). However, in the present work, the hardware realization of addition only has been demonstrated. The Clock frequency for realization into the board is supplied by an external function generator. Output results are captured using a logic analyzer. Input data to the board (system) is passed manually through the available slide switches on-board.<br><br> |

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## 1. INTRODUCTION

The simplicity operations of Walsh transforms attracted many scientists to develop, use, apply and even combine it with other transform's models. Historically, the fundamental theory of Walsh transforms has been proposed since long time ago [1-3]. Several novel designs of how to realize Walsh transforms have been introduced in the last several decades.

In 1976, Fino and Algazi proposed how to achieve Walsh transform using addition and subtraction technique [4]. The idea attracted many researchers for hardware realization of Walsh transforms. However, the method required addition and subtraction of samples in word level. Later, a method of the bit level systolic array is developed to increase the speed [5]. Then, Nayak and Meher proposed a fully pipelined two-dimensional (2D) bit-level systolic architecture to achieve a more efficient implementation [6].

Amira et al. proposed a new way of implementing Walsh transforms in years 2000 and 2001 based on Hadamard matrices called Fast Hadamard Transform (FHT) [7-9]. A more intense research has been carried out during last decade. For example, a method of how to generate Walsh functions in four different orderings has been introduced [10]. Later, Chandrasekaran proposed power analysis of Walsh transforms [11]. Then, a technique of efficient architecture of Walsh transforms was developed in 2008 [12] besides many other designs that has been published.

The concept of application of Walsh transforms for addition and multiplication of two digital signals was described earlier [13-14]. A more intensive works on this also has been published. Most of the researchers and scientists focus on developing Walsh transforms only. However, even less, a technique of inverting Walsh transforms is also have been developed [15-16].

The simplicity of Walsh transforms, combines with the powerfully of Fourier transforms result in a more efficient transform algorithm was available [17-19]. A method of calculating both DFT and WHT is developed through the factorization of intermediate transform T by Bousasakta and Holt [17]. An efficient algorithm which combines the calculation of DFT and WHT was also introduced. The technique is based on the development of radix-4 fast Walsh Hadamard Transform (FWHT) [18]. Another efficient method of calculating both DFT and WHT using radix-2 was published [19]. The new idea that utilizes Rademacher functions for generating Discrete Fourier Transforms (DFT) has been carried out [20-21]. This works proved a strong link between DFT and WHT since both of them can be generated by applying the product of Rademacher functions.

In the present work, we use Walsh transforms for hardware realization of the addition of two digital signals targeted to Xilinx Spartan 3 board. The rest of the paper is organized as follows. Section 2 deals with the brief theory of Walsh ordering. Section 3 covers system design concept, Section 4 deals with hardware realization. Section 5 presents significant conclusions.

## 2.    WALSH ORDERING

Walsh transforms is a unique transforms model; the coefficient may be ordered in different series. There are about four well-known orderings which are sequency (Walsh), dyadic (Paley), natural (Hadamard) and logic [1]. The original Walsh functions that are used to generate Walsh transforms are ordered in sequency. Meanwhile, Hadamard ordering is often created based on Hadamard matrices. Then, Paley ordering can be produced by applying bit reversal of the Hadamard ordering. The last ordering model is more convenient when it is generated based on the component-wise product of Rademacher functions [22]. Logic ordering model orders the coefficients in the increasing number of components of Rademacher functions.

Table 1 shows four different Walsh ordering for m=3 Rademacher functions for a total $w=2^m=8$ possible of discrete Walsh functions [1].

Table 1. Orderings of Walsh Functions Represented as Product of Rademacher Functions

| w | Ordering | | | |
|---|---|---|---|---|
| | Walsh | Paley | Hadamard | Logic |
| 0 | $R_0$ | $R_0$ | $R_0$ | $R_0$ |
| 1 | $R_1$ | $R_1$ | $R_3$ | $R_1$ |
| 2 | $R_1 R_2$ | $R_2$ | $R_2$ | $R_2$ |
| 3 | $R_2$ | $R_2 R_3$ | $R_2 R_3$ | $R_3$ |
| 4 | $R_2 R_3$ | $R_3$ | $R_1$ | $R_1 R_2$ |
| 5 | $R_1 R_2 R_3$ | $R_1 R_3$ | $R_1 R_3$ | $R_1 R_3$ |
| 6 | $R_1 R_3$ | $R_2 R_3$ | $R_1 R_2$ | $R_2 R_3$ |
| 7 | $R_3$ | $R_1 R_2 R_3$ | $R_1 R_2 R_3$ | $R_1 R_2 R_3$ |

## 3.    SYSTEM DESIGN (ADDITION)

The design of an integrated system covering addition, subtraction, multiplication and AWG has been presented earlier [13-16]. However, the design requires a very significant hardware and hence it needs quite expensive FPGAs. Also, only addition of two digital signals is desired. Thus the system is redesigned to offer hardware realization of addition only. This design can easily be accommodated in the simplest and cheapest FPGA board – the Spartan 3 board. Thus a highly economical system is made available.

Figure 1 views design of integrated system for transform lengths N=4 and input word lengths WI=4. *Choice* and *Ordering* are used to select the suitable processes and Walsh orderings respectively. Signal *Enter* is used to *pass* the input signals X and G.
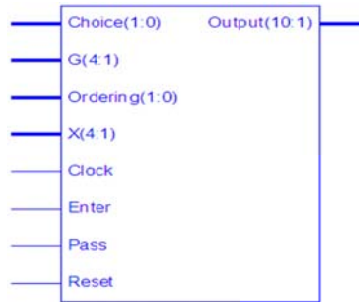
Figure 1. Design of Integrated System for N = 4 and WI = 4

Signal Pass is used to control the output view, if Pass = 0, the resulting signal will be available at the Output. Conversely, when Pass = 1, the Walsh coefficients of X, G and result signals are available at the Output.

Table 2 shows possible choice of DSP processes for simplicity realization into FPGA, meanwhile, Table 3 views all possible choices of and Walsh ordering, except for logic ordering.

Table 2. List of DSP Processes

|                | Choice (1) | Choice (0) |
|----------------|------------|------------|
| Addition       | 0          | 0          |
| Subtraction    | 1          | 0          |
| Multiplication | 1          | 1          |
| AWG            | 0          | 0          |

Table 3. Walsh Ordering Choices

|          | Ordering (1) | Ordering (0) |
|----------|--------------|--------------|
| Hadamard | 0            | 0            |
| Paley    | 0            | 1            |
| Sequency | 1            | 0            |

## 4.  HARDWARE REALIZATION
### 4.1.  Behavioral Simulation

Figures 2 and 3 show behavior simulation results of the designed system. Initially, *Reset* goes high to clear all buffers in the system. Inputs X and G are passed into the system controlled by Enter. Entry data X, G and output addition result view in Figure 2, meanwhile coefficients of X, G and output based on Paley ordering are shown in Figure 3.
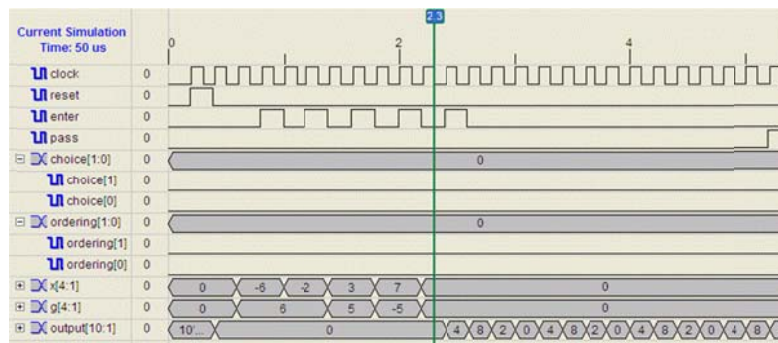


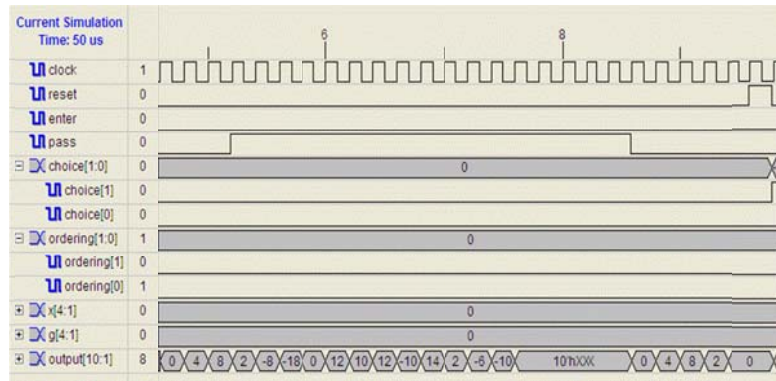Figure 2. Entry and Output Signals for N = 4 and WI = 4

Figure 3. Walsh Coefficients of Entry and Output Signals for N = 4 and WI = 4

### 4.2. Synthesis Report

The next step is to extract some important information through synthesis report. This report is available after implementation stage. Some of the important data of the implemented system are given below. It can be seen that the selected device is suitable for carrying out the design addition system. It requires 381 slices, 177 slice flip-flops, 694 of 4 input LUTs, 26 I/Os (all of them are bonded), 12 multipliers (18x18 bits) and 2 Gclks. Based on this requirement, the design system can run up to maximum 31.753 MHz. The realization can capture input data with arrival time before 9.276 ns and the output data will be available at the output port after 6.216 ns.

```
synthesize Selected Device : 3s200ft256-4
 Number of Slices:              381  out of   1920    19%
 Number of Slice Flip Flops:    177  out of   3840     4%
 Number of 4 input LUTs:        694  out of   3840    18%
 Number of IOs:                 26
 Number of bonded IOBs:         26  out of    173    15%
 Number of MULT18X18s:          12  out of     12   100%
 Number of GCLKs:                2  out of      8    25%
Speed Grade: -5
   Minimum period: 31.493ns (Maximum Frequency: 31.753MHz)
   Minimum input arrival time before clock: 9.276ns
   Maximum output required time after clock: 6.216ns
   Maximum combinational path delay: No path found
```

### 4.3. Clock to Pad

Another important data after implementation step is clock to pad delays. This delay is vary based upon location of each output path inside the chip. The deviation of these delays corresponding to different outputs should be as small as possible to avoid glitches. As can be seen below, the delays of different pads vary from 6.403 ns to 6.405 ns and the deviation is minuscule (maximum 0.002 ns). There is no clock phase require for implementing the design system.

```
Clock Clock to Pad
-----------+-----------+-----------------+-------+
           | clk (edge)|                 | Clock |
Destination|  to PAD   |Internal Clock(s)| Phase |
-----------+-----------+-----------------+-------+
Output<1>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<2>  |  6.405(R) |Clock_BUFGP      | 0.000|
Output<3>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<4>  |  6.405(R) |Clock_BUFGP      | 0.000|
Output<5>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<6>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<7>  |  6.403(R) |Clock_BUFGP      | 0.000|
Output<8>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<9>  |  6.404(R) |Clock_BUFGP      | 0.000|
Output<10> |  6.403(R) |Clock_BUFGP      | 0.000|
-----------+-----------+-----------------+-------+
```

### 4.4. Hardware Adjustments

The synthesis results viewed in the previous section are based on automatic selection of I/Os by Xilinx ISE software. In other words, the input and output ports are selected automatically by software to minimize deviation of clock to pad delay or time. It can be seen that the clock to pad delays of all outputs are around 6.4 ns. Some adjustments are required for matching the I/O availability in Spartan 3 board.

Table 4 shows all configurations for input and output. This selection is based on the availability input and output of FPGA board. Three push button switches are assigned for signals Reset (L13/ push button BTN2), Pass (M13/ Push Button BTN0) and Enter (M14/ Push Button BTN1). While, input data X(J14, J13, K14, K13/SW7 to SW4)and G (F12, G12, H14, H13/SW3 to SW0) require toggle switches since they have to be available continuously before signal Enter goes high. Eight switches are needed to handle the input data because each of them is formatted in the form of 4 bit number. In other to capture the Output (D5, C5, D6, C6, E7, C7, D7, C8/Pin 5 to 12 of Expansion Connector A2), an expansion cable is required for connecting output results to logic analyzer. The output result is also displayed in on-board LEDs for indication and manual verification.

Table 4. Output and Some Inputs Selection for Hardware Realization

|  | Pin / Position on Board | Input/ Output |
| --- | --- | --- |
| Reset | L13 / Push button BTN2 | Input |
| Enter | M13 / Push button BTN0 | Input |
| Pass | M14 / Push button BTN1 | Input |
| X (1, 2, 3, 4) | J14, J13, K14, K13 / SW7 to SW4 | Input |
| G (1, 2, 3, 4) | F12, G12, H14, H13 / SW3 to SW0 | Input |
| Output (1, 2, 3, 4, 5, 6, 7, 10) | D5, C5, D6, C6, E7, C7, D7, C8 / Pin 5 to 12 of Expansion Connector A2 | Output |

### 4.5. Hardware Results

Hardware realization has been done using Spartan 3 board. The clock to the system is supplied by external function generator at a frequency of 20 MHz. Input X and G are passed into the board manually through 8 slide switches as listed in Table 4 and output is viewed using logic analyzer TLA5000B. Figure 4 views four values of signal output H = {0, 4, 8, 2} as a result of addition process at frequency 20 MHz.



Figure 4. Output Signal of Integrated System (Addition Process) for N = 4 and WI = 4

Figure 5 shows the Walsh coefficients of the input signals and the output signal. There are 12 numbers; the first four {2, -8, -18, 0} are coefficients of signal X; next four values {12, 10, 12, -10} are coefficients of signal G and the last four numbers {14, 2, -6, -10} are coefficients of the output signal.

A close examination is shown in Figure 6. The figure shows some glitches during transition from 2 to -6 which are the second and the third coefficients of signal output. These glitches appear due to variation in clock to pads delays. As marked in Figure 6, the longest clock to pad delay is 14.14 ns, and this is longer compared to the synthesis result which is around 6.4 ns. The increased delay due to hardware adjustment as listed in Table 4, cable delay and delay of Logic Analyzer.

Figure 7 shows how two input signals are passed into the board. Four slide switches on the right are assigned for signal input X = {6, 6, 5, -5} and other four switches are assigned for signal input G = {-6, -2, 3, 7}. The details are shown in Table 4.
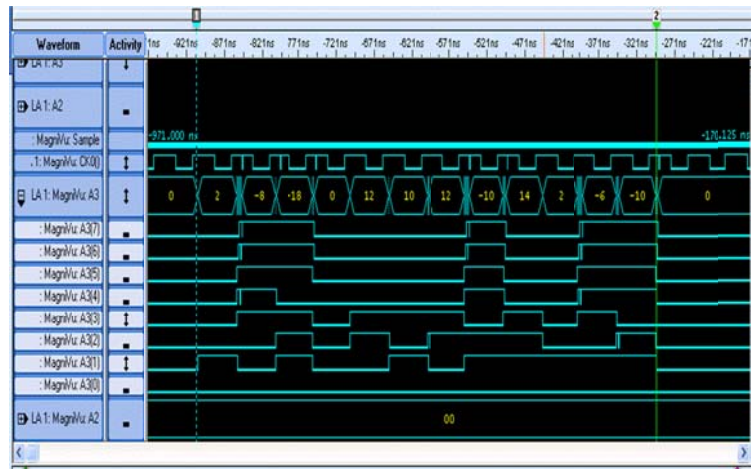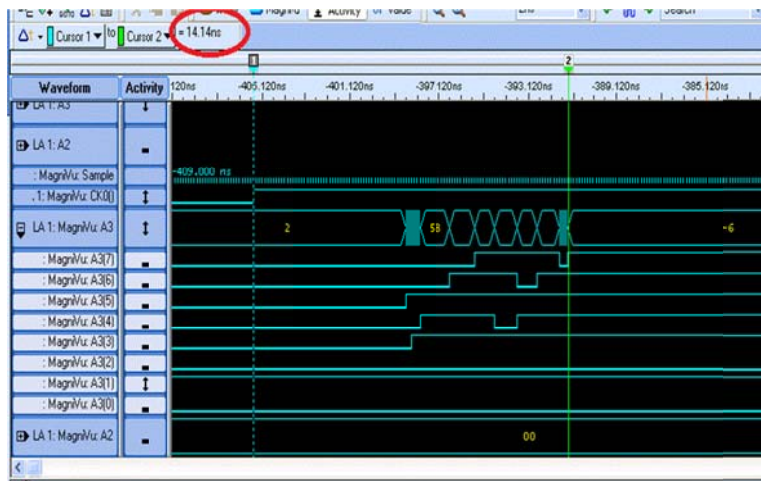


Figure 5. Walsh Coefficients of Signal X, G and Output



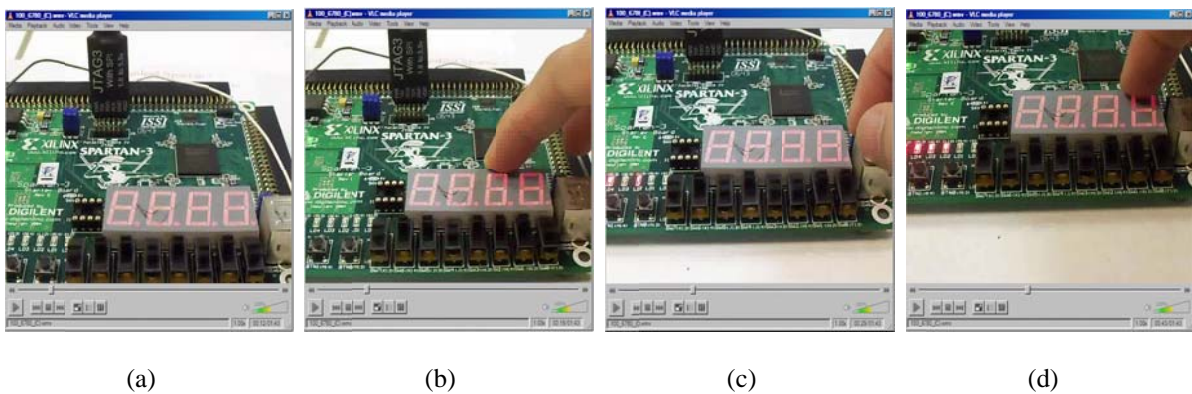Figure 6. Close Examination between the Coefficients 2 and 6



(a)                  (b)                  (c)                  (d)

Figure 7. Input Signals X and G of Integrated System for N = 4 and WI = 4; (a) "0110 1010" = "6 -6" (dec); (b) "0110 1110" = "6 -2" (dec); (c) "0101 0011" = "5 3" (dec); (d) "1011 0111" = "-5 7" (dec)

In order to see a more clear hardware realization (human eyes viewed), the outputs are passed to the LEDs equipped on the board and the frequency that has been reduced to 1 Hz. Figure 8 views output signal H = {0, 4, 8, 2} when the system is operated under addition mode. Figures 9 to 11 show coefficients of signal X = {2, -8, -18, 0}, G = {12, 10, 12, -10}, and H = {14, 2, -6, -10} respectively. The LEDs are displaying the coefficients to the output when push button (assigned for Pass) is pressed.
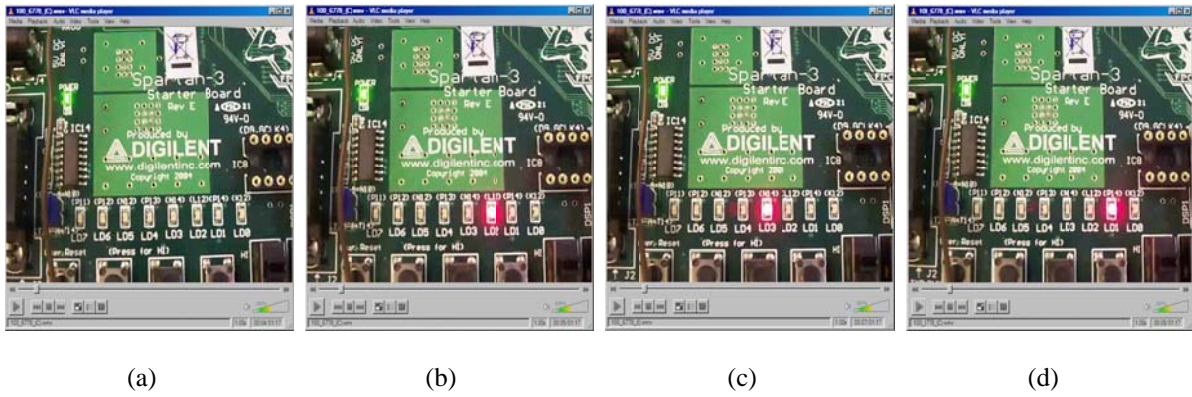


|        (a)        |        (b)        |        (c)        |        (d)        |

Figure 8. Output Signal of Integrated System (addition) for N = 4 and WI = 4; (a) "00000000" = 0 (dec); (b) "00000100" = 4 (dec); (c) "00001000" = 8 (dec); (d) "00000010" = 2 (dec)



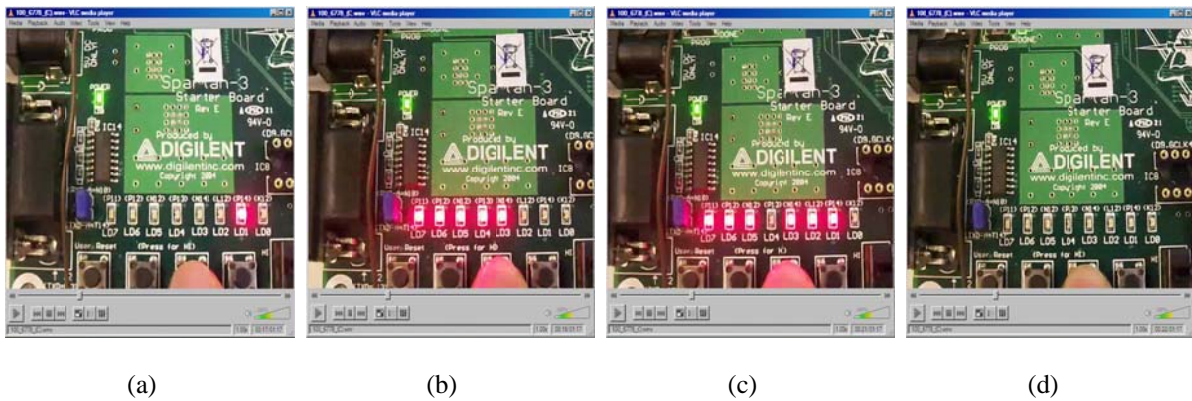|        (a)        |        (b)        |        (c)        |        (d)        |

Figure 9. Coefficients of Input Signal X of Integrated System (addition) for N = 4 and WI = 4; (a) "00000010" = 2 (dec); (b) "11111000" = -8 (dec); (c) "11101110" = -18 (dec); (d) "00000000" = 0 (dec)



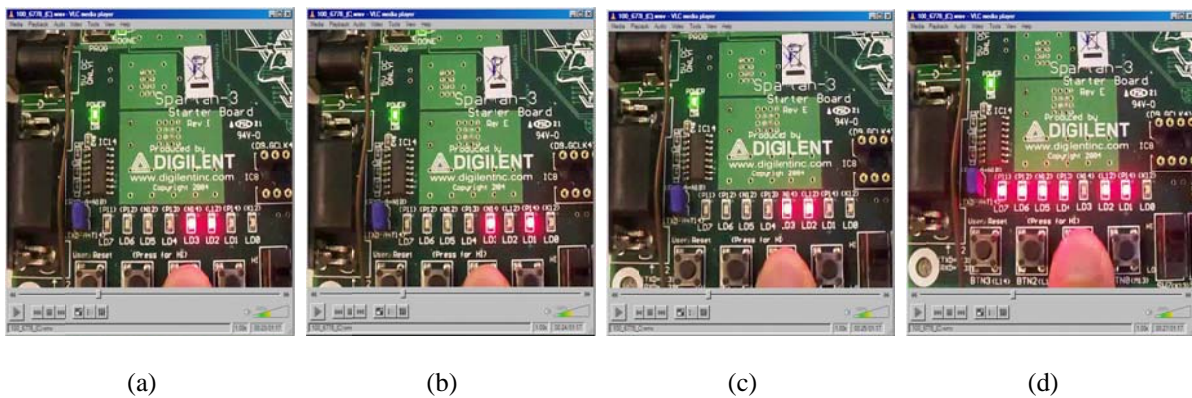|        (a)        |        (b)        |        (c)        |        (d)        |

Figure 10. Coefficients of Input Signal G of Integrated System (addition) for N = 4 and WI = 4; (a) "00001100" = 12 (dec); (b) "00001010" = 10 (dec); (c) "00001100" = 12 (dec); (d) "11110110" = -10 (dec)

|        (a)        |        (b)        |        (c)        |        (d)        |

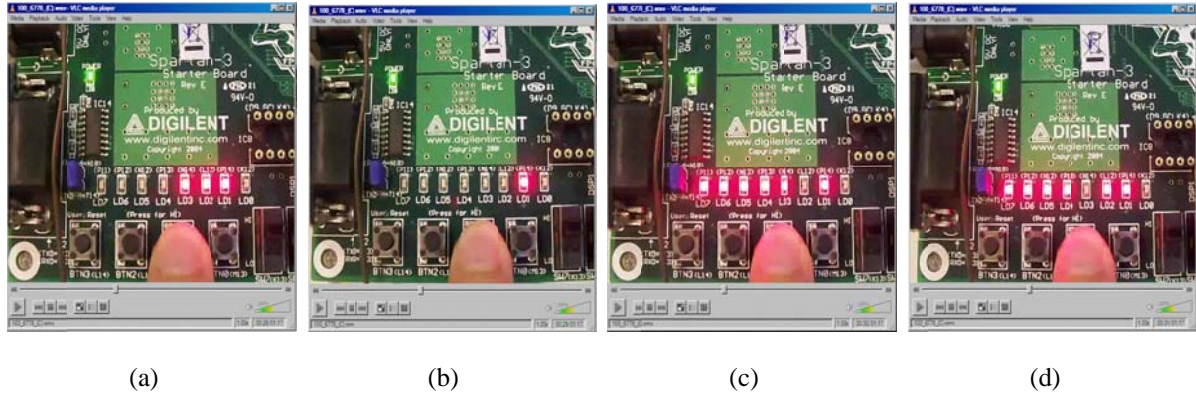Figure 11. Coefficients of Output Signal H of Integrated System (addition) for N = 4 and WI = 4;
(a) "00001110" = 14 (dec); (b) "00000010" = 2 (dec); (c) "11111010" = -6 (dec); (d) "11110110" = -10 (dec)

## 5.   CONCLUSION

Hardware realization of addition of two signals based on Walsh transforms has been done successfully. The realization has been targeted to FPGA Spartan 3 board. The clock is generated using an external function generator. The output is captured using logic analyzer TLA5000B.  Because of hardware adjustments, the time from clock to pad increases more than twice from 6.403 ns to 14.14 ns. Although the system is designed to perform addition, subtraction and multiplication processes, the hardware realization of only addition is presented due to hardware limitation of the Spartan 3 board.

## REFERENCES

[1]   M.G. Karpovsky, R.S. Stankovic and J.T. Astola, *Spectral Logic and Its Applications for The Design of Digital Devices*, John Wiley & Sons Inc. Publication, New Jersey, 2008
[2]   K.G. Beauchamp, *Applications of Walsh and Related Functions with an Introduction to Sequency Theory*, Academic Press, 1984
[3]   M. Maqusi, *Applied Walsh Analysis*, 1st ed., Heyden and Son Ltd, London, 1981
[4]   B.J. Fino, V.R. Algazi, Unified Matrix Treatment of the Fast Walsh-Hadamard Transform, *IEEE Transactions on Computers*, 1976; 42: 1142-1146
[5]   L.W. Chang, M.C. Wu, A bit level systolic array for Walsh–Hadamard transforms, *Transaction on Signal Processing*, vol. 31, no. 3, pp. 341–347, 1993.
[6]   S.S. Nayak, P.K. Meher, High Throughput VLSI implementation of discrete orthogonal transforms using bit-level vector-matrix multiplier, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*. vol. 46, no. 5. pp. 655–658, 1999.
[7]   A. Amira, A. Bouridane, P. Milligan, *A Novel Architecture of Walsh Hadamard Transform using Distributed Arithmetic Principles*, in Proc. of The 7th IEEE International Conference on Electronics, Circuit & Systems (ICECS'2K), Beirut, Lebanon, 2000.
[8]   A. Amira, A. Bouridane, P. Milligan, M. Roula, *Novel FPGA Implementations of Walsh-Hadamard Transforms for Signal Processing*, in Proc. of IEE Vision, Image, and Signal Processing, 2001.
[9]   A. Amira, A. Bouridane, P. Milligan and M. Roula, an FPGA implementation of Walsh–Hadamard transforms for signal processing, *Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEEE International Conference on*, Salt Lake City, UT, 2001, pp. 1105-1108 vol. 2.
[10]  B.J. Falkowski, T. Sasao, *Unified Algorithm to Generate WalshFunctions in Four Different Orderings and Its ProgrammableHardware Implementations*, in Proc. of IEE on Vision, Image and Signal Processing, 2005, pp. 819–826.
[11]  A. Amira, S. Chandrasekaran, Power Modeling and Efficient FPGAImplementation of FHT for Signal Processing", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 3, pp. 286–295, 2007.

[12] P.K. Meher, J.C. Patra, *Fully-Pipelined Efficient Architectures for FPGA Realization of Discrete Hadamard Transform*, in Proc. OfInternational Conference on Application-Specific Systems, Architecture and Processors (ASAP 2008), 2008, pp. 43–48.

[13] Zulfikar, S.A. Abbasi and A.R.M. Alamoud, FPGA based processing of digital signals using Walsh analysis, *Electrical, Control and Computer Engineering (INECCE), 2011 International Conference on*, Pahang, 2011, pp. 440-444.

[14] Z.M. Yusuf, S.A. Abbasi and A.R.M. Alamoud, "FPGA Based Analysis and Multiplication of Digital Signals," *Advances in Computing, Control and Telecommunication Technologies (ACT), 2010 Second International Conference on*, Jakarta, 2010, pp. 32-36

[15] Zulfikar, S.A. Abbasi, and A.R.M. Alamoud, "FPGA Based Complete Set of Walsh and Inverse Walsh Transforms for Signal Processing," *Transaction of Electronics and Electrical Engineering*, vol. 18, no. 8, pp. 3-8, October 2012

[16] Zulfikar, S.A. Abbasi, and A.R.M. Alamoud, "Design of Real Time Walsh Transform for Processing of Multiple Digital Signals," *Transaction of International Journal of Electrical and Computer Engineering*, Vol. 3, No. 2, pp. 197-206, April 2013

[17] S. Boussakta and A.G.J. Holt, "Fast algorithm for calculation of both Walsh-Hadamard and Fourier transforms (FWFTs)," in *Electronics Letters*, vol. 25, no. 20, pp. 1352-1354, 28 Sept. 1989

[18] M.T. Hamood and S. Boussakta, "Fast Walsh–Hadamard–Fourier Transform Algorithm," in *IEEE Transactions on Signal Processing*, vol. 59, no. 11, pp. 5627-5631, Nov. 2011

[19] T. Su and F. Yu, "A Family of Fast Hadamard–Fourier Transform Algorithms," in *IEEE Signal Processing Letters*, Vol. 19, No. 9, pp. 583-586, Sept. 2012.

[20] Zulfikar and H. Walidainy, "A novel 4-point discrete Fourier transforms circuit based on product of Rademacher functions", *Electrical Engineering and Informatics (ICEEI), 2015 International Conference on*, Denpasar, 2015, pp. 132-137.

[21] Zulfikar, H.Walidainy, "Design of 8-point DFT based on Rademacher Functions", *Transaction of International Journal of Electrical and Computer Engineering*, Vol. 6, No. 4.

[22] R.E.A.C. Paley, "A Remarkable Series of Orthogonal Functions (I)," *London Mathematical Societies*, 34 (1932) pp. 241-264

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He joined as teaching staff in the Department of Electronics at Politeknik Caltex Riau, Pekanbaru, Indonesia in 2003. He served as head of Industrial Control Laboratory, Politeknik Caltex Riau from 2003 to 2006. In 2006, he joined the Electrical Engineering Department, Syiah Kuala University. He has been appointed as head of Digital Laboratory for two successive years. His current research interests include VLSI design and System on Chips (SoC).

**Shuja A. Abbasi,** he was born at Amroha, India in 1950. He obtained the degrees of B.Sc. Engineering and M.Sc. Engineering in Electrical Engineering in 1970 and 1972 respectively from Aligarh Muslim University (AMU), Aligarh, India with the first position in the University. He didPh.D. from University of Southampton, England in 1980 in Microelectronics.
He joined as Assistant Professor in the Department of Electrical Engineering at Aligarh Muslim University, Aligarh, India in 1971, was promoted to the positions of Associate Professor and Professor in 1982 and 1986 respectively. He shifted to the newly created Department of Electronics Engineering at AMU as Professor in 1988. He served as Chairman, Department of Electronics Engineering, AMU from 1996 to 1999. He held many Academic/Administrative positions in the past at AMU and outside. He joined as Professor of Electronics Engineering at College of Engineering, King Saud University, Riyadh, Saudi Arabia in 1999 and is continuing there since then. He has more than 100 research publications to his credit so far. He has completed many client funded projects from various organizations. His current interests include VLSI design and technology.

**Abdulrahman A. Alamoud,** he was born in Onaizah, Saudi Arabia on Sept. 21, 1946. He earned his B.Sc. degree in Electrical Engineering, College of Engineering (COE) from the University of Riyadh (renamed later as KSU). He earned his M.Sc., in Microelectronics, and Ph.D., in photovoltaic solar cells, from West Virginia University, Morgantown, W.V., USA in 1974 and 1984 respectively. In June 1984, he joined the Department of Electrical Engineering, KSU and was promoted to the rank of Professor in 1999. In 1991 he took a one year leave of absence from KSU and joined the Advanced Electronics Company AEC), Riyadh, Saudi Arabia as the Special Projects Director. In1992 he was appointed as Director, Research Center, COE, KSU for a two term period in June 1996. In the academic year June 1996- Sept 1997 he was a Visiting Research Associate Professor,National Renewable Energy Laboratory, Golden, Colorado, USA (July15-Dec.15, 97) where he worked on the development of thin films CdTe Solar Cells and characterization of materials (such as semiconductors thin films and Saudi white sand rocks) and a Visiting Research Associate Professor, VLSI Research Group**,** Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada. Worked on the design of VLSI circuits using Cadence (Mar.9-Aug.22, 97). He was chosen to be the Vice Dean for Administrative Affairs, COE, KSU during the period of June 1999- June 2005. His research interests are in both microelectronics, Solar Cells and Materials, and Photovoltaic Systems.