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Effect of Parasitic Elements on the Performance of Buck-Boost Converter for PV Systems

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ABSTRACT

In the proposed study, MOSFET device used in buck-boost converter for PV systems is studied. The parameter of MOSFET Rds (on) is varied and its effect on output voltage is studied. The parasitic elements in inductor and capacitor such as resistance on buck-boost converter performance are studied. From the proposed study it has been found that the effect of parasitic resistance in capacitor is less as compared to parasitic resistance effect of inductor. Also the proposed study gives better insight into parasitic effect of Printed Circuit Board and losses incurred due to the same. In PV systems buck-boost converter is used to convert solar energy to electrical energy which is then stored in battery to drive the loads. These parasitic elements will have considerable effect on the performance of buck-boost converter such as efficiency and output voltage as validated by experimental results.

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1. INTRODUCTION

In recent years renewable energy has gained more importance, due to fossil fuel exhaustion and increase in environmental problems because of conventional power generation. PV system is one of the renewable energy sources. For converting solar energy to electrical energy a good efficient buck-boost converter is needed. In buck-boost converter, a inductor, a capacitor and a MOSFET switch is used. In all these there are parasitic elements which affect the performance of buck-boost converter. In the proposed study, effects of parasitic elements are discussed in detail. The effect of filter elements inductor and capacitor on the performance of buck converter is discussed in [1]. The performance parameters such as ripple content in the output current and voltage, efficiency and regulation are studied. But the parasitic elements effect on the performance of buck-boost converter is not discussed. DC-DC switching converters are discussed in [2] and here the effect of parasitic elements on voltage conversion ratio is discussed. Due to parasitic elements voltage gain reduces and this gain reduction is avoided by limiting the duty ratio. Due to parasitic element up to certain value of duty ratio the gain increases after that gain reduces drastically. The effect of parasitic elements in inductor is considered. But the effect of parasitic elements present in MOSFET switch and capacitor are not considered. Nur Mohammad et. Al [3] discussed on parasitic effects on the performance of DC-DC Single Ended Primary Inductor Converter (SEPIC) in Photovoltaic applications. In this paper, the effect of parasitic elements on the performance of DC-DC SEPIC in PV systems is discussed. The parasitic element in inductor used in converter is varied and its effect on output voltage has been seen. It has been found that the gain and the efficiency are reduced. In this paper it is mentioned that the effects of parasitic should be considered to improve accuracy, performance stability and robustness of the converter. But only inductor parasitic resistances are considered and capacitor parasitic resistances are not considered. Also the effects of parasitic elements present in MOSFET switch are not considered. The voltage degradation when non idealities such as parasitic resistance of inductor and source resistance are taken into account is discussed in [4]. The paper discusses about efficiency degradation of the converter when the parasitic resistances are considered. But only inductor and source parasitic resistances are considered and capacitor parasitic resistance is not considered. Also the effects of parasitic elements present in MOSFET switch are not considered. The small signal ac equivalent circuit model for buck-boost converter is developed in [5]. The characteristics output voltage as a function of duty ratio is nonlinear but this has been linearised while developing the model. The effect of winding resistance in inductor is considered while developing the model. In the proposed study, MOSFET model from Simulink is considered. The various parameters in MOSFET model are discussed in section 2. Effect of parasitic element in MOSFET is discussed in Section 3. Effect of parasitic element in inductor is discussed in Section 4. Effect of parasitic element in capacitor is discussed in Section 5.

2. EFFECT OF PARASITIC ELEMENT IN MOSFET

For the proposed work the MOSFET model from Simulink has been chosen. The MOSFET model and its equivalent circuit is shown in Figure 1 The MOSFET device is connected in parallel with an internal diode that turns on when the MOSFET device is reverse biased. This internal diode is provided to protect against reverse voltage. The model is done using an ideal switch and it is turned ON or OFF using a gate signal g. The diode is connected in parallel with the switch.

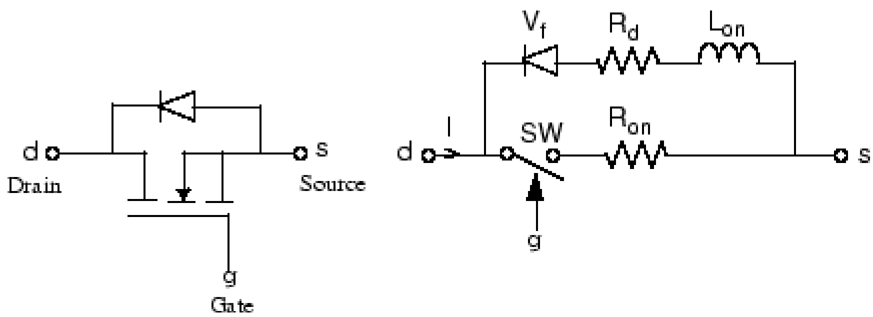

Figure 1. MOSFET and its equivalent circuit

The ON state voltage of MOSFET Vds will vary according to following aspects

- When MOSFET is turned ON Vds=Rds(on)* I where I is the current flowing through the device when it is turned ON.
- When the device is turned OFF, anti-parallel diode starts conducting then

Vds = Rd*I-Vf +Lon*di/dt where Vf is the internal diode forward voltage drop. The anti-parallel diode inductance is denoted as Lon and it is used only for continuous systems. For discrete systems this has been set to zero. The initial current is denoted as Ic and it is the initial value of current that flows in the MOSFET. For the steady state analysis the initial current should be considered. Snubber resistance Rs and Snubber capacitance Cs are used in the model to give protection against dv/dt. The MOSFET block implemented in simulink is a macro model of the MOSFET. It will not consider the device geometry and complex physical processes involved in fabrication of the device [2]. The MOSFET block available in simulink should not be connected in series with an inductor, a current source, unless its snubber circuit is in use. The design specification of buck-boost converter is as follows:

- Input voltage = 5 to 20V
- Output voltage = -12V
- Switching frequency = 50 KHz
- Wattage rating = 25 Watt
- Inductor ripple current (Δi_L) = 3% of I_L
- Output Voltage Ripple (ΔV_{out}) = 0.01*V_{out}=0.12
- The buck-boost converter is designed and the values obtained are
- Inductor L=1.5 mH
- Capacitor C=220 μF

The buck-boost converter is simulated with these values and it has been found that it meets the specifications. The simulation diagram is shown in Figure 2. The parasitic resistance Rds(on) plays a role when the switch is closed. The effect MOSFET parasitic resistance Rds(on) on output voltage is observed and it is as shown in Figure 3. Rds (on) computes power loss and efficiency in a circuit containing a MOSFET switch. The power dissipated in the MOSFET is given by the product of Rds(on) and drain current. In Figure 3, series 1 represents for Rds(on) value equal to 0Ω, series 2 represents for Rds(on) value equal to 0.001Ω, series 3 represents for Rds(on) value equal to 0.05Ω and series 4 represents for Rds(on) value equal to 0.08Ω. It has been observed that as the value of Rds(on) increases the output voltage decreases.

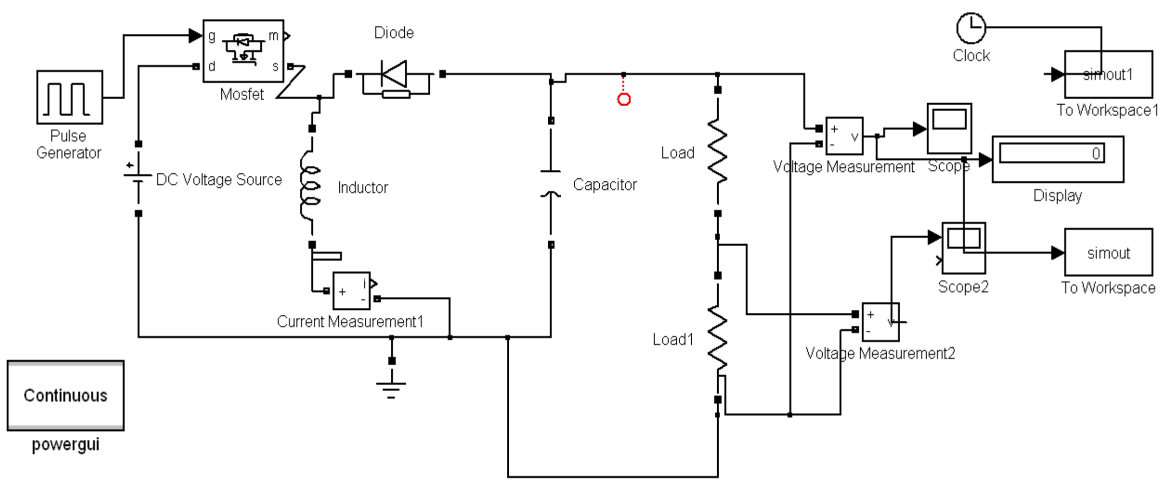

Figure 2. Buck-Boost Converter Simulation Diagram

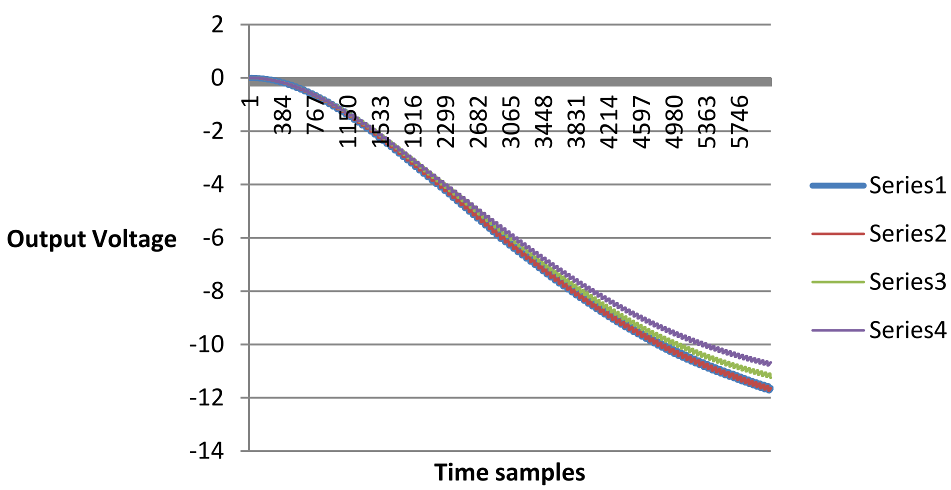

Figure 3. Effect of Rds(On) on output voltage

Table 1. Effect of Rds(On) on output voltage

Rds(on)	Output voltage
Rds=0 Ω	-11.95V
Rds=0.001Ω	-11.85V
Rds=0.05Ω	-11.27V
Rds=0.08Ω	-10.92V

3. EFFECT OF PRINTED CIRCUIT BOARD (PCB) PARASITICS

The contribution of stray inductances and capacitances are present in PCBS. These are considered as parasitic elements from PCB. Power loss due to trace is given by Ptrace and this is given by

$$P_{trace} = I_{trace}^2 R_{trace} \quad (1)$$

Power loss due to stray inductance is called as P_{Lstray} and it is calculated as

$$P_{Lstray} = I_{trace} L_{stray} (\frac{di}{dt}) \quad (2)$$

where Lstray is calculated from $L_{stray} = 2 * 10^{-4} Le \left[\ln\left(\frac{2Le}{W+H}\right) + 0.2\left(\frac{w+H}{Le}\right) + 0.5\right]$ (3)

The stray capacitance is calculated as $C_{stray} = 0.085 \mathcal{E}r A/d$ (4)

The stray capacitance power loss P_{cstray} is given by

$$P_{cstray} = \frac{V_d^2 C_{stray} f_{sw}}{2} \quad (5)$$

The total loss in PCB is given by $P_{pcb}=P_{trace} + P_{Lstray} + P_{cstray}$ (6)

Where Le is length of PCB trace and H is height of PCB trace and W is width of PCB trace, Ɛr is dielectric constant of air, A is the area of plates and d is separation between the plates.

4. EFFECT OF PARASITIC ELEMENT IN INDUCTOR

The effect of variation in inductor parasitic resistance on output voltage is shown in Figure 4. The results are tabulated in Table 2. The series 1 represents the output voltage variation for ideal inductor i.e R_L = 0Ω. The series 2 represents the output voltage variation for inductor with R/R_L = 100 where R is the load resistance. The load resistance value is equal to R = 3.215Ω and we get R_L = 0.03215 Ω. The series 3 represents the output voltage variation for inductor with R/ R_L = 80 and we get R_L = 0.047 Ω. The series 4 represents the output voltage variation for inductor with R/ R_L = 40 and we get R_L = 0.093 Ω. The series 5 represents the output voltage variation for inductor with R/ R_L = 8 and we get R_L = 0.467 Ω.

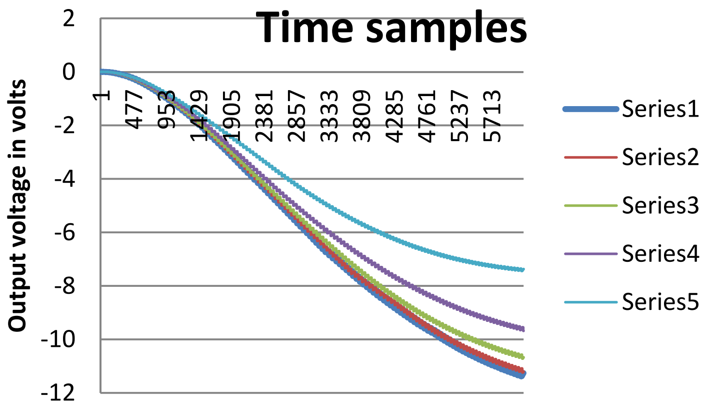

Figure 4. Effect of parasitic resistance variation of inductor

From the graph it has been observed that as the value of parasitic resistance of inductor increases the voltage gain of buck-boost converter decreases. Therefore, the value of parasitic resistance R_L should be minimum as possible. The ideal efficiency is unity and the efficiency of a buck boost converter when parasitic elements are considered is given by

$$\eta = \left[1 - \frac{Vsn}{Vg} - \frac{Vsf(1-d)}{dVg}\right]\left[\frac{1}{1+\frac{\alpha+\beta d}{(1-d)^2}}\right] \quad (7)$$

Table 2. Effect of parasitic resistance variation of inductor

Parasitic resistance of inductor value	Output voltage
Ideal Inductor $R_{L=0}$	-12.03V
$R_{L=0.03215\Omega}$	-11.68V
$R_{L=0.047\Omega}$	-11.29V
$R_{L=0.093\Omega}$	-10.7V
$R_{L=0.467\Omega}$	-7.2V

Where Vsn is the ON state switch voltage drop and Vsf OFF state switch voltage drop, d is the duty ratio and Vg is the source voltage $\alpha=R_L/R$ $\beta=R_g/R$.

5. EFFECT OF PARASITIC ELEMENT IN CAPACITOR

The parasitic resistance in a capacitor used in buck-boost converter is varied and its effect on the performance of buck-boost converter is seen and this is as shown in Figure 5. The output voltage values are tabulated in Table 3. It has been found that the parasitic resistance in capacitor has no significance effect on the output voltage. Higher the value of parasitic resistance lesser will be the output voltage.

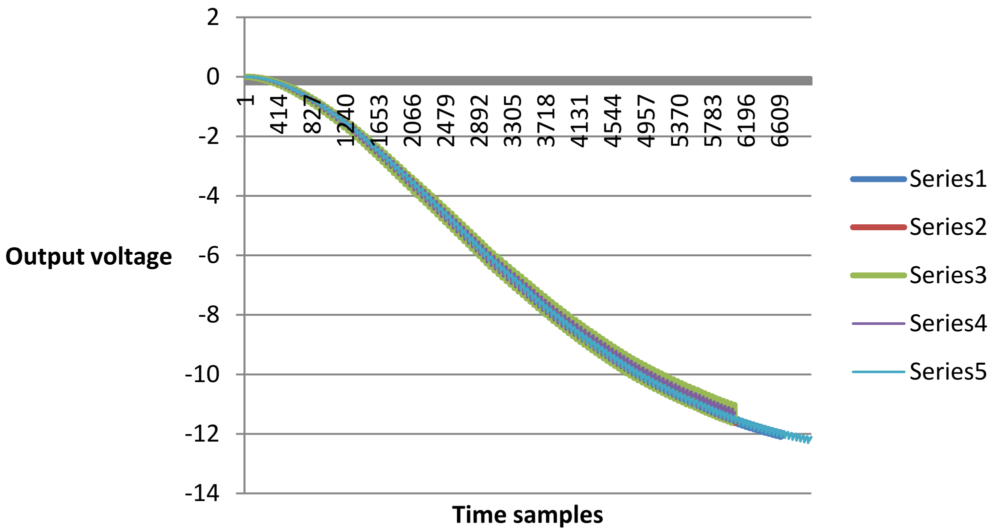

Figure 5. Effect of parasitic resistance variation of capacitor

Table 3. Effect of parasitic resistance variation of capacitor

Parasitic Resistance Value	Output voltage
R=0	-12V
R=0.001Ω	-11.95V
R=0.01Ω	-12.13V
R=0.05Ω	-11.79V

6. CONCLUSION

In the proposed study, the effect of parasitic capacitances in a MOSFET such as gate to drain capacitance, Cgd and gate to source capacitance Cgs are not considered. It has been also found that the effect parasitic resistance in capacitor on output voltage is less as compared to the effect of parasitic resistance of inductor. Also in the proposed study the parasitic effects of PCB is explained. While developing buck-boost converter on a PCB these effects should be considered. The parasitic effect of resistance and capacitances from the solar panel also should be studied which effects the maximum power point tracking. The proposed study has given better insight into parasitic elements effect on the performance of buck-boost converter used in PV systems. These parasitic even effects the battery charging used in PV systems. Due to parasitic the efficiency degrades and therefore the effect of parasitic should be minimized so as to improve the efficiency.

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Subramanya Bhat is currently pursuing Ph.D, under Visvesvaraya Technological University, Belgaum, India. He is currently working as an Associate professor in the department of Electronics & Communication Engineering, Canara Engineering College, Mangalore, India. He has presented more than 15 papers in National and International conferences and Journals. His research interests include power electronics, signal processing, control systems and image processing. He has given more than 10 invited talks in his research field. He was awarded with many best paper awards in National and International conferences.

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