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A CMOS-based Analog Function Generator: HSPICE Modeling and Simulation

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ABSTRACT

In many Engineering applications, analog circuits present many advantages over their digital counterparts and have recently been particularly used in a wide range of signal processor circuits. In this paper, an analog non-linear function synthesizer is presented based on a polynomial expansion model. The proposed function synthesizer model is based on a 10th order polynomial approximation of any of the required non-linear functions. The polynomial approximations of these functions can then be implemented using basic CMOS circuit blocks. The proposed circuit model can simultaneously synthesize and generate many different mathematical functions. The circuit model is designed and simulated with HSPICE and its performance is demonstrated through the simulation of a number of non-linear functions.

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1. INTRODUCTION

Analog nonlinear circuits have many applications, especially in signal processing, communication, instrumentation, neuralnetworks, and medical equipment. As a result, a large number of analog signal processors have been discussed in the literature. Initially, analog signal processors were designed with the use of passive electronic components such rersistors and simple semiconductor devices such as diodes and BJT transistors. With the advant of JFET and MOSFET transistors, the non-linear characteristics of these devices have then been exploited in the design of such processors. Many approaches involving the use of piecewise-linear function approximations of non-linear functions have been reported in the literature [1], [2]. In this respect, BJT and BiCMOS transistors have been used to simulate non-linear functions.

More recently, CMOS analog circuits based on the exponential-law and the square-law characteristics of a MOS transistor operating in strong and weak inversion respectively have been reported [3], [4]. These circuit realizations present some disadvantages, the two most important being the realization of only one function at a time and their operation in voltage mode or mixed current and voltage mode. However, in current-mode circuits wider signal bandwidths and larger dynamic ranges of operation can be obtained as opposed to voltage-mode circuits .

A number of CMOS current-mode analog processors have been reported in the litearture. However, these circuits present many disadvantages such as their realization of only a few functions and only one funtion at a time [5]-[7]. In addition, these circuits are based on piecewise linear approximations of the non-linear functions.

CMOS current-mode analog signalsynthesizer has recently been proposed [7]. The circuit was based on a third order Taylor's series expansions of nonlinear functions which restricted the number of functions that can be realized and the accuracy of their realizations.

2. MODEL FORMULATION

In this paper, a CMOS-based circuit model of a current-mode anlog function synthesizer that can realize a large number of non-linear functions is presented. The circuit model is based on a 10th-order polynomial approximation of any non-linear function and is compatible with the CMOS technology currently used in digital signal processing. Another adavantage of the proposed model is the operation of the CMOS transistors in the strong inversion region, leading to the possible circuit operation at high frequencies. Other advantages of the proposed circuit model are the simulatneous realization of many nonlinear functions at a time that do not need the use of piece linear approximation. In the proposed circuit model, a 10^{th} order polynomial of the form given in equation (1) is used to approximate non-linear functioins with a high degree of accuracy.

$$f(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 + a_6x^6 + a_7x^7 + a_8x^8 + a_9x^9 + a_{10}x^{10} \quad (1)$$
$$|x| < 1$$

3. PROPOSED CIRCUIT MODEL

Equation (1) can be realized by taking the sum of theweighted output currents of a number of building blocks that consist of the traditional class-AB current mirror circuit to provide both power-raising and amplification of the current input, and adding it to a constant current. One such building block is the squarring unit shown in Figure 1.

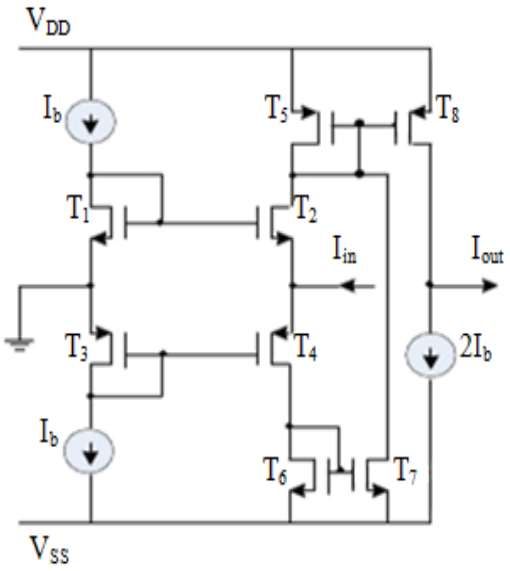

Figure 1. Modified current mirror to provide output currents proportional to the square of the input current

The Transisitors T_1 and T_2 as well as T_3 and T_4 are assumed to be well matched and Transistorss T_1 through T_8 are assumed to have the same value of the transconductance parameter i.e., $\beta n = \beta p$ and are operating in their stauration region. The aspect ratios (W/L) of transistors $T_1 - T_8$ of Figure 1 are given in Table 1.

Table 1. Aspect Ratios (W/L) for the transistors of Figure 1

Transistor	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
W/L	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1

With these assumptions, the translinear principle is applied to produce the output current I_{out} which can be then expressed as [7]

$$I_{out} = \frac{{I_{in}}^2}{8I_b} \quad (2)$$

In order to obtain another output current proportional to the input current, two additional transistors T_9 and T_{10} are added with aspect ratios 1/2 and 1/1 respectively as shown in Figure 2.

From this circuit, output currents of value $a_1 x$ or $a_2 x^2$, can be obtained by using additional current mirrors of different aspect ratio values (W/L) .

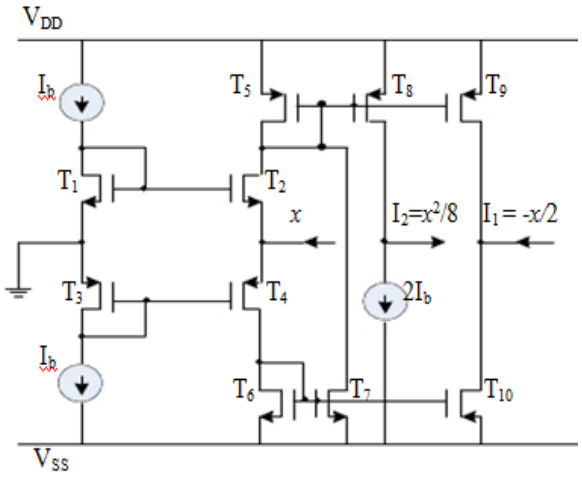

Figure 2. Modified squaring circuit of figure 1 to provide outputcurrents proportional to the input current and its square.

Applying the translinear principle, the normalized output current in Figure 2 will be given by :

$$I_1 = -\frac{I_{in}}{2I_b} \text{ or } I_1 = -\frac{x}{2} \quad (3)$$

where $x = I_{in}/I_b$ represents the normalized input current. Equation (2) can also be re-written using the normalized input current as:

$$I_{out} = \frac{{I_{in}}^2}{8I_b} \text{ or } I_2 = \frac{I_{out}}{I_b} = \frac{x^2}{8} \quad (4)$$

And in order to obtain a current proportional to x^3, the followingrelation is used:

$$\frac{(x+x^2)^2}{8} - \frac{(x-x^2)^2}{8} = \frac{x^3}{2} \quad (5)$$

The corresponding circuit will therefore requires two modified squaring circuits with inputs proportional to the difference and the sum of the input current and its square. The required third order term in equation (1) can then be obtained by selecting appropriate values of the aspect ratios (W/L).

Therefore, and in order to obtain output currents proportional to even and odd powers of the input current, the modified squaring circuit of Figure 2 along with equation (5) are repeatedly used. Tables 2-a and 2-b give the details of the inputs that are used to produce output currents proportional to x^3 through x^{10}.

Table 2-a. Output currents proportional to odd powers of input currents

I_{in}	$x + x^2$ and $x - x^2$	$x + x^4$ and $x - x^4$	$x + x^6$ and $x - x^6$	$x + x^8$ and $x - x^8$
I_1	$x^3/2$	$x^5/2$	$x^7/2$	$x^9/2$

Table2-b. Output currents proportional to even of input currents

I_{in}	x	x^2	x^3	x^4	x^5
I_2	$x^2/8$	$x^4/8$	$x^6/8$	$x^8/8$	$x^{10}/8$

It can therefore be seen that higher-order terms of equation (1) can be obtained by repetitive use of the circuit model of Figure 2 without the need for dedicated current multipliers. With this design and the addition of a normalized DC current, any nonlinear function can be realized using MOSFET current-mirrors with the appropriate aspect ratios (W/L). Figure 3 shows the basic circuit model of the function synthesizer where B refers to the squaring circuit model of Figure 2. The circuit shows only outputs proportional to x through x^6.

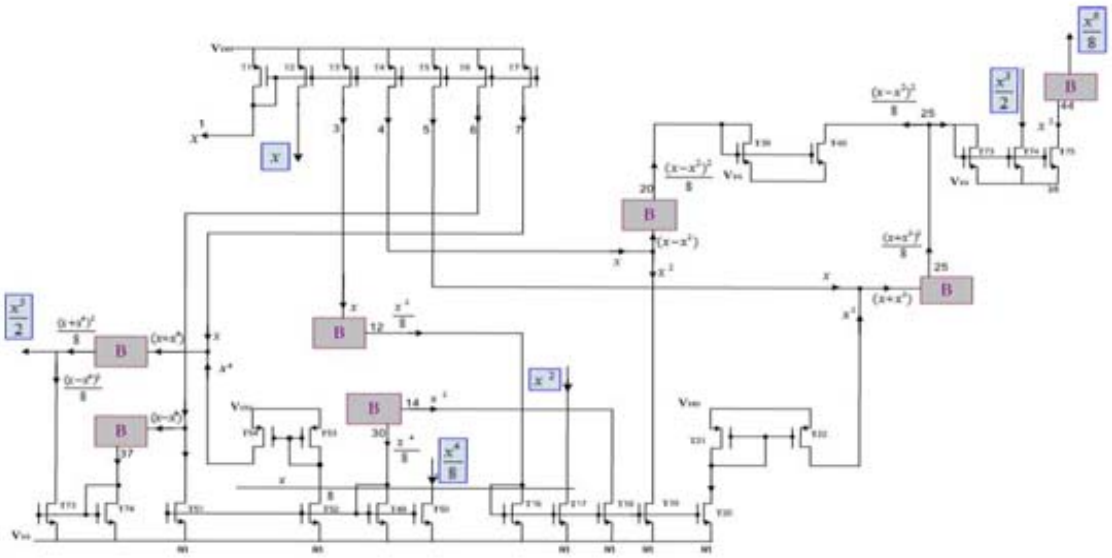

Figure 3. Basic circuit model for the function synthesizer showing outputs proportional to the first 6 terms of the polynomial expansion

4. SIMULATION RESULTS

The basic circuit models of Figure 3 was used in the simulation of a number of nonlinear functions. The corresponding polynomial expansion coefficients a_i, i = 1, … 10 for selected functions are given in Tables 3-a and 3-b, and the transistors'aspects ratios were selected accordingly. HSPICE circuit simulation environment was used and the simulation was carried out using the BSIM2 level 39 MOSFET transistor models with L=0.1μm, bias current I_b=1μA and supply voltages V_{DD} = -V_{SS} = 2V. For each function simulation, the input current was changed from 0 μA to 1μA, and the output currents throughload resistances of 1=$M\Omega$ was obtained obtained. A DC current source = 1μA wasadded to the output node to represent the constant term in equation (1) which equals, according to Tables 3-a and 3-b, either to 1 or zero.

Table 3-a. Polynomial expansion coefficients for selected functions

Function	a_0	a_1	a_2	a_3	a_4	a_5
sin(x)	0	1	0	-1/6	0	1/120
$\frac{1}{\sqrt{1+x}}$	1	-1/2	3/8	-5/16	35/ 128	- 0.2461
tanh(x)	0	1	0	-1/3	0	2/15
ln(1- x)	0	-1	-1/2	-1/3	-1/4	-1/5
e^x	1	1	1/2	1/6	1/24	1/120
$J_1(x)$	0	1/2	0	-1/16	0	1/384
$I_0(x)$	1	0	1/4	0	1/64	0
$\sqrt{1-x^2}$	1	0	-1/2	0	-1/8	0

Table 3-b. Polynomial expansion coefficients for selected functions

Function	a_6	a_7	a_8	a_9	a_{10}
sin(x)	0	-1/5040	0	1/362880	0
$\frac{1}{\sqrt{1+x}}$	0.2256	-0.2095	0.1964	-0.1855	0.1762
tanh (x)	0	-17/315	0	0.0219	0
ln(1-x)	-1/6	-1/7	-1/8	-1/9	-1/10
ex	1/720	1/5040	1/40320	1/3628 80	1/3628800
$J_1(x)$	0	-1/18432	0	1/14745 60	0
I_0 (x)	1/2304	0	1/14745 6	0	1/14745 600
$\sqrt{1-x^2}$	-1/16	0	-5/128	0	-7/256

The exact nonlinear functions were calculated and their graphs compared with those of the simulated functions as illustrated in Figure 4. Inspection of this figure clearly shows that the simulated results are in excellent agreement with the calculated ones. Table 4 shows the range of input current values for which the error between corresponding functions is less than 1% which further reflects the accuracy of the proposed function synthesizer circuit model.

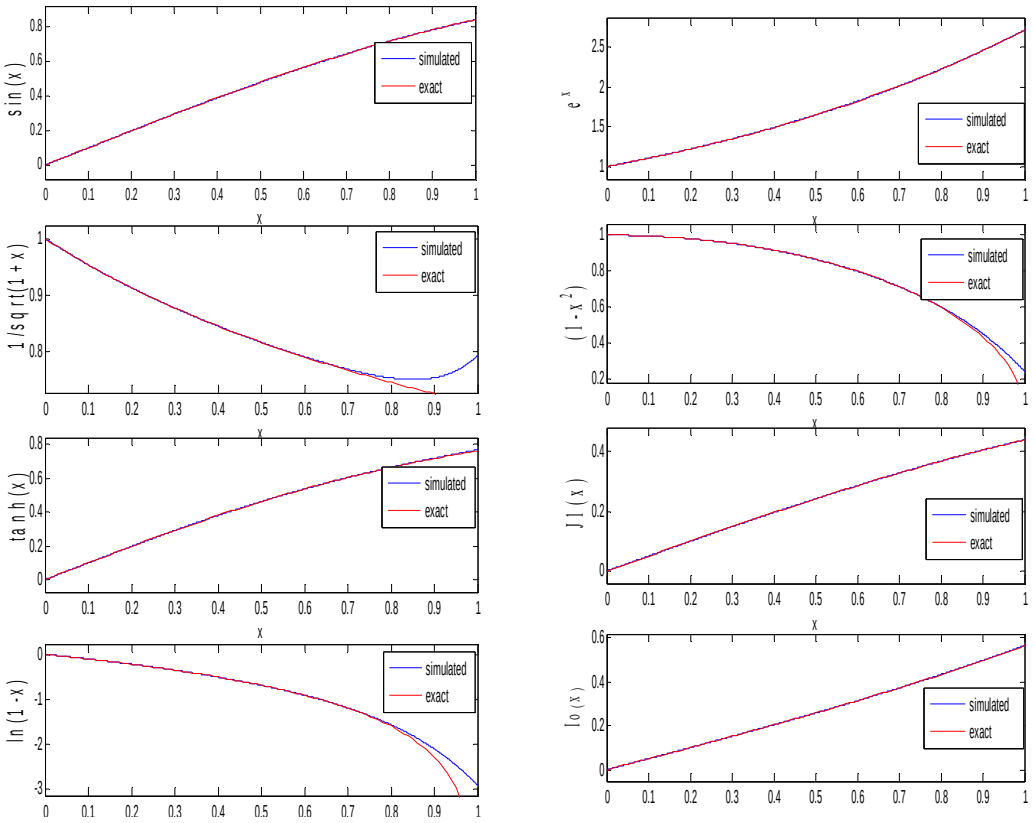

Figure 4. Simulated and calculated functionsfrom Tables 3-a and 3-b

Table 4. Range of input current values

Function	sin(x)	$\frac{1}{\sqrt{1+x}}$	tanh (x)	ln(1-x)	e^x	$J_1(x)$	$I_0(x)$	$\sqrt{1-x^2}$
Range of x	< 1 μA	< 0.8 μA	< 1 μA	< 0.8 μA	< 1 μA	< 1 μA	< 1 μA	< 0.9 μA

5. CONCLUSION

Design of a simple function synthesizer using MOSFET transistor models available in HSPICE simulation environment has been presented. The circuit model was based on approximating any nonlinear function with the first 10 terms in its polynomial expansion. The circuit model that realizes any of these functions consists of power-factor raising circuits built around a basic current squarer circuit, a weighted current amplifier and a dc current source. The proposed synthesizer model can be easily modified to implement many functions by proper selection of the transistors' aspect ratios. The accuracy of the synthesized function will be primarily decided by the number of terms used in the power expansion approximation and the effects of mismatch between transistors used in practical implementation of the required current-mirrors. Expanding further the approximation requires the use of additional similar power-raising circuit blocks. HSPICE Simulation of a number of nonlinear functions supported by the evaluation of the mean square error between exact and simulated functions values verified the validity of the proposed function synthesizer circuit model.

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BIOGRAPHY OF AUTHOR

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