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A Low Power 32 Bit CMOS ROM Using a Novel ATD Circuit

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ABSTRACT

A low power high speed 32 Bit ROM circuit implemented on 0.18µm CMOS process has been presented in this paper. The circuit is build using a parallel ROM core structure and runs on 1.8 V supply voltage. A novel Address Transition Decoder (ATD) circuit is proposed which energizes the ROM components such as Row Decoder, Column Decoder, ROM core etc, for short time intervals when there is a transition in input address bits. The power consumed in ROM with proposed ATD circuit is 0.78 mW, which corresponds to 82.27% reduction in power as compared to ROM without ATD circuit (4.46 mW). At the output almost full signal swing has been achieved without using any sense amplifier. The implemented ROM has a very low latency of 0.56 ns.

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1. INTRODUCTION

With an ever increasing demand for portable consumer electronic products powered by batteries in the market, The ASIC designers are facing the challenge of developing techniques for low power consumption. This requires that each and every module of the system must be designed for lowest possible power. Almost every digital device have embedded ROM blocks in them to store fixed information such as micro codes, look up tables, words library etc. These ROM blocks consume lots of power because they have highly capacitive lines which are frequently accessed. The main source of power dissipation in ROMs is the storage array or ROM core which consumes about 90% of the total power [2].

Basic structure of 32 bit ROM is shown in Figure 1. This ROM is organized as a 32x1 bit ROM having 4 rows and 8 columns which correspond to 2 row address bits and 3 column address bits. A row containing 8 memory locations is selected according to 2 row address bits. Now out of these 8 memory locations one memory location is selected according to 3 column address bits whose content is the desired output. For power reduction an ATD circuit is used in this design to precharge the circuit before every memory read operation.

The paper is further organized as follows – Next section describes various components of 32 Bit ROM that is ROM core, Address Decoders and ATD circuit in detail. Simulation results and waveforms are explained in section III and conclusion in section IV.

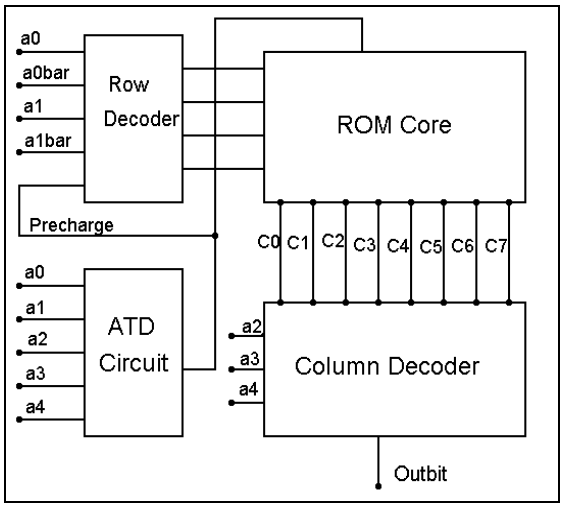

Figure 1. 32 Bit ROM Structure

2. RESEARCH METHOD

The main objective of this paper is to design a low power 32 bit ROM by employing power reduction techniques. A number of low power techniques for ROMs, both at architectural and circuit level have earlier been proposed. These include hierarchical word line, selective precharge, voltage scaling, NMOS precharge etc. High power saving can be achieved only by using multiple power reduction techniques [2]. B D Yang and L S Kim proposed a low power charge recycling ROM architecture which showed 13% improvement in power consumption but suffered about 1.5 times area overhead and 2.3 times speed overhead [6]. In this paper we have focussed on the design of a novel ATD circuit which reduces the power comsumption of ROM. Implementation details of proposed ATD circuit and all other ROM components is presented in this section.

2.1. ROM Core or Storage Array

The ROM core is used to store information through the placement of transistors. This can be implemented in two ways-NAND array, in which pull down transistors are connected in series or NOR array, where pull down transistors are connected in parallel. NAND arrays have high packing density but low speed operation as compared to NOR arrays [9]. In this paper we have used NOR array for high speed operation. In Fig. 2 a parallel 8 bit ROM core is shown. It has 4 PMOS transistors acting as pull up devices.

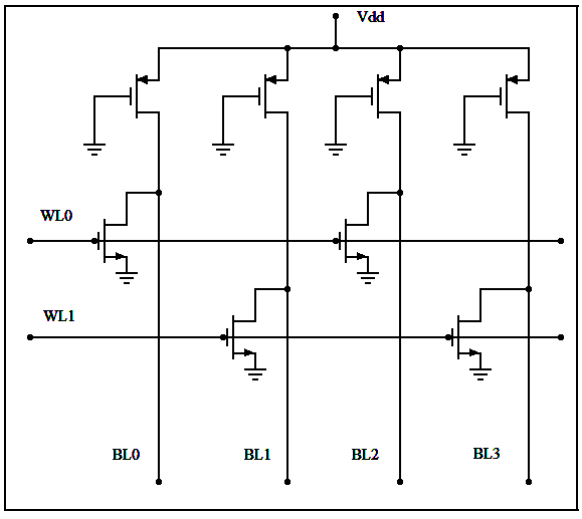

Figure 2. Eight bit CMOS ROM core (NOR array)

The presence of a pull down NMOS shows that logic zero is stored in that location. In the absence of a pull down device, the output is pulled to logic high state by pull up device showing that the presence of logic one.

2.2. Address Transition Decoder (ATD) Circuit

ATD circuit is the key component of this design which reduces the static power dissipation to almost zero. It acts as a pre-charge circuit which provides supply voltage to ROM core and address decoders in the form of short pulses only when a memory read operation is to be performed or there is a change in input address bits, otherwise no supply voltage is given to any ROM component which almost eliminates the static power dissipation in the ROM.

Wei Cui et al., used an ATD circuit in their ROM design, which is implemented basically using delay blocks and Ex-OR gates whose schematic is illustrated in Fig. 3 [1]. A delay of 4.1 ns has been used in this ATD circuit. The width of the output pulse depends upon the time period of this delay circuit. To implement a delay circuit using buffers requires a number of buffers cascaded in series which results in increased area and power consumption of the circuit. Also there is a good amount of delay present between address transition and output pulse generation which hampers the proper functioning of the ROM.

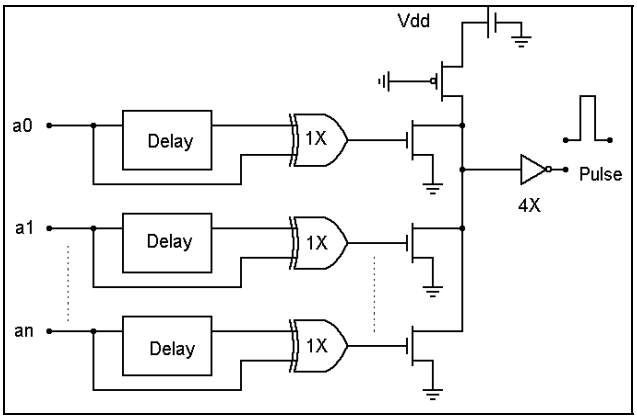

Figure 3. ATD Circuit using delay blocks

To overcome these problems a novel ATD circuit is proposed in this paper which is implemented using dual edge pulse generators and an OR gate. The block diagram of novel ATD circuit is shown in Fig. 4.

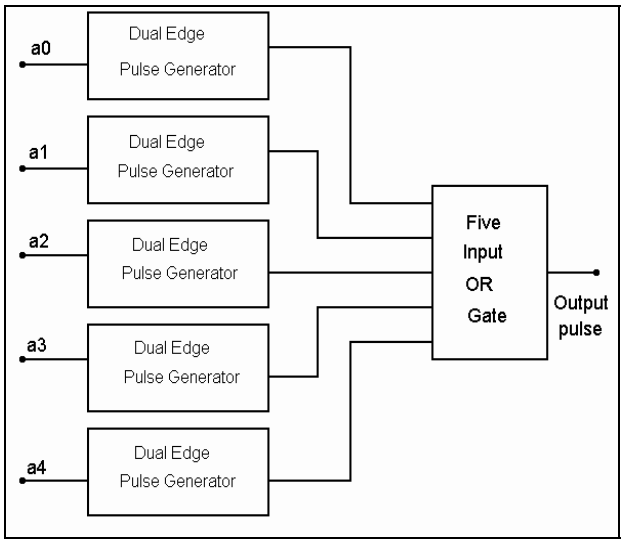

Figure 4. Proposed ATD Circuit Block Diagram

A dual edge pulse generator circuit is used as a component, which generates a short pulse on both rising and falling edges of the input clock signal [8]. The width of generated pulse is 1.2 ns and the delay is also less than the ATD circuit discussed in [1]. The schematic of pulse generator circuit is shown in Fig 5.

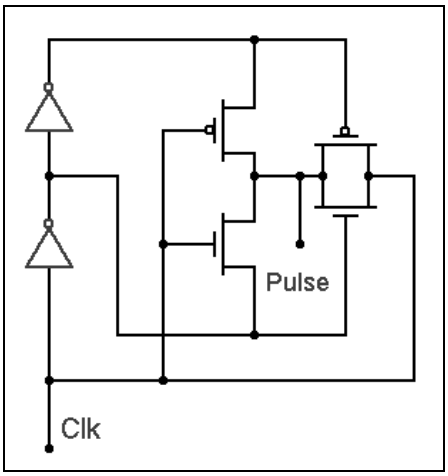

Figure 5. Dual Edge Pulse Generator Circuit

All the input address bit lines are given as inputs to five pulse generators and the outputs of all pulse generators are fed to a five input OR gate so that whenever an address transition take place at any one of the address bit lines, a pulse is generated at the output of the OR gate. The drive strength of the OR gate should be made sufficiently large so that it can drive the other ROM components easily.

2.3. Address Decoders

Two address decoders are used in the designed ROM, one is the 2: 4 row decoder which enables one out of four rows and other is a column decoder that can be described as an 8: 1 multiplexer. Like storage array, the row decoder can also be implemented either as NOR array or NAND array [1]. In this design NOR based address decoder is used, whose schematic is shown in Fig 6.

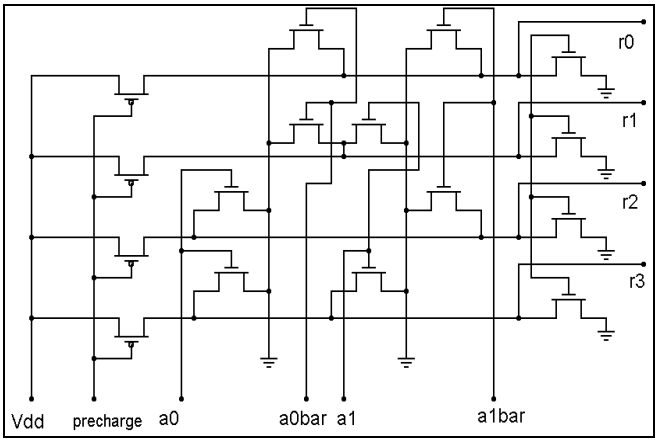

Figure 6. CMOS NOR based **2: 4 Row** Decoder

The column decoder can be implemented as an 8 : 1 multiplexer but to reduce the number of transistors and chip area a tree based column decoder is used that uses a binary reduction scheme [10]. The schematic of column decoder is shown in Fig 7. The number of transistors for a 2^k input tree based column decoder is given by

$$N_{trans} = 2^k+2^{k-1}+ - - - 2^0 = 2 \text{ x } (2^k - 1) \quad (1)$$

In this design, number of inputs = $2^k = 8$, k = 3
Therefore

$$N_{trans} = 2x\ (2^3 - 1) = 14 \quad (2)$$

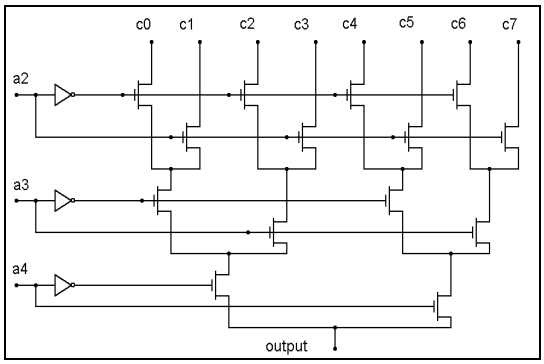

Figure 7. 8:1 Tree Based Column Decoder

3. RESULTS AND ANALYSIS

The ROM Core, Row Decoder, Column Decoder and ATD schematics are designed using Cadence Virtuoso Schematic Editor and are simulated using Cadence Spectre tool at 180nm technology. The Table I shows bit pattern stored in ROM core for test purpose. The simulations are performed at input transition frequency of 200MHz. The waveforms in Fig. 8 show the results corresponding to eight input addresses 00000 to 00111 respectively.

Table I. Bit Pattern Stored in ROM Core

	BL0	BL1	BL2	BL3	BL4	BL5	BL6	BL7
WL0	0	1	0	1	0	1	0	1
WL1	1	0	1	0	1	0	1	0
WL2	0	1	0	1	0	1	0	1
WL3	1	0	1	0	1	0	1	0

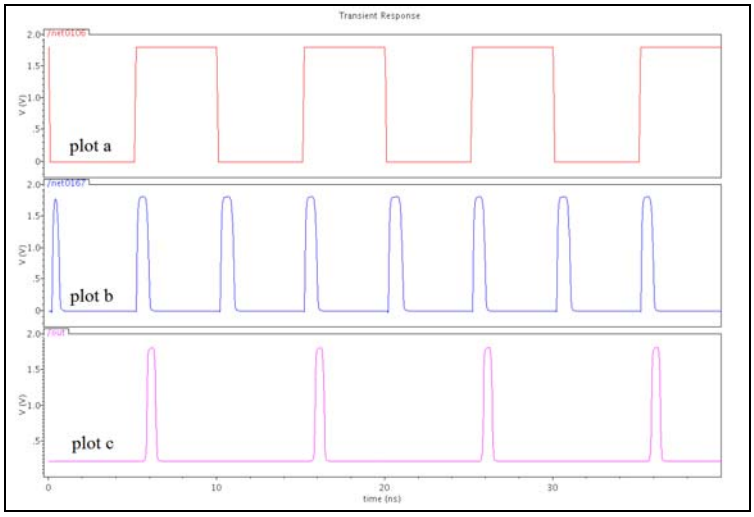

Figure 8. Simulation Results (a) input address changing every 5ns (200MHz), (b) ATD circuit output, (c) ROM output corresponding to input address bits

The power & time delay calculations are performed using Visualization & Analysis XL Calculator provided in Cadence Spectre tool. The power consumed in 32 Bit ROM is 0.782mW and delay is 0.56ns which results in improved PDP of 0.438 PJ.

In a ROM the amount of power consumed varies with the address transition frequency and also with the bit pattern that is stored in the ROM core. This is illustrated with a graph shown in Fig 9. From the graph we can see that power consumption increases with increase in frequency and also the power consumed is more when more zeroes are stored in ROM core than ones.

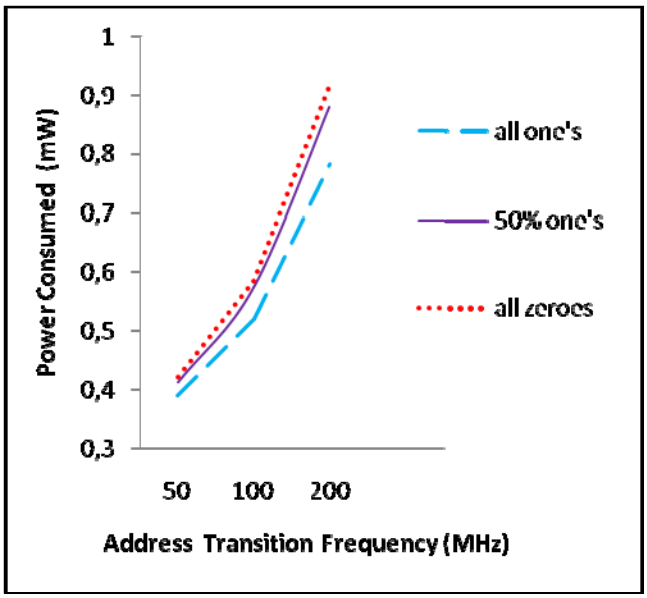

Figure 9. Variation of power with frequency and ROM contents

Table II list some of earlier CMOS ROM designs existing in literature along with important parameters of each design.

Table II. Overview of the work already carried out in the field of Low Power CMOS ROM Design

Paper Ref.	ROM Organiza -tion	Technolog y Node	Supply Voltag e	Freq. (MHz)	Power (mW)	Delay (ns)
[1]	1Kx 16Bits	180 nm	1.8 V	100	-	8.6
[3]	128 x 1 Bit	180 nm	0.7 V	50	0.0389	-
[4]	8Kx16 Bits	350 nm	3.3 V	100	8.63	-
[5]	1Kx32 Bits	350 nm	3.3 V	100	5.35	7.8
[6]	1Kx32 Bits	250 nm	2.5 V	100	3.53	6
[7]	4Kx32 Bits	250 nm	2.5 V	240	8.2	-
This Work	32 x 1 Bit	180 nm	1.8 V	200	0.78	0.56

4. CONCLUSION

A 32 Bit low power ROM has been proposed which uses a novel ATD circuit for power reduction. The designed ROM with ATD circuit shows an improvement of 82.27% in power consumption as compared

to a ROM without an ATD circuit. Full voltage swing is achieved at the output without using any sense amplifier. The output must be read in a specific time slot as defined by the pulses generated by ATD circuit, beyond this time slot output always remains at zero level. Maximum input transition frequency is limited to 0.4 GHz. The ROM circuit exhibits a good PDP of 0.438 PJ due to high speed and low power consumption.

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