

High Performance Low Power Dual Edge Triggered Static D Flip-Flop

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ABSTRACT

In this paper a low-power double-edge triggered static flip-flop (DETSFF) suitable for low-power and high performance applications is presented. The designed DETFF is verified at gpdk 180nm-1.8V CMOS technology. Comparison with some of the latest DETFFs shows that the proposed DETSFF can achieve the lowest power consumption, lowest clock to Q delay and thus Power-delay-product (PDP). Moreover, the proposed DETSFF comprises of only 15 transistors hence require lesser number of transistors and thus requires lesser overall silicon area.

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1. INTRODUCTION

The increasing trend of portable hand held electronic devices have set a goal of high performance computing with lower energy consumption. The focus of VLSI designer is to achieve best possible tradeoff between power and delay for a circuit while keeping smallest possible area and complexity to reduce the overall cost of manufacturing.

Flip-Flops are key circuit elements in realizing digital systems. The performance of the Flip-Flop is an important parameter to determine the performance of the overall design. They have large impact on the circuit speed and power consumption. Therefore, the study on Flip-Flops has become quite significant in recent years.

True single phase clocking (TSPC) [1] has been shown to be an efficient technique to achieve very high-speed digital VLSI design. One method to improve the design performance is to use dual edge triggered flip-flop (DETFF). The dual-edge triggering is an effective technique to reduce the power consumption in the clock distribution network. In this approach flip-flops samples data on both rising and falling edges of the clock so that only half the clock frequency is needed to obtain the same data throughput as compared to that of single edge triggered flip-flops (SETFFs) [2]. Several low power, high speed dual-edge triggered flip flop designs have been studied [3-7].

In this brief, we present a novel low-power, high speed DETSFF design based on a signal feed-through scheme. This mechanism is implemented by introducing a two inverted master latches which operate at alternate clock phases, their output is coupled to a static slave latch at alternate clock phases to form a new dual edge triggered flip flop design with enhanced speed and optimum power-delay-product (PDP).

Various approaches have been followed for implementing dual edge triggered flip flops [8-9]. Each technique has its own advantages and disadvantages. They are briefly discussed in the following section.

1.1. Dual Edge Triggered Static Pulsed Flip-Flop (DESPFF)

Aliakbar [8] introduced a new innovation in designing a dual edge triggered flip flop. Figure 1 shows the schematic of DSPFF. Its pulse generator design incorporates four inverters which are used to generate the inverted and delayed clock signals. The signals from pulse generator along with two NMOS pass transistors generates a narrow sampling window at both the transition edges i.e. rising and falling edges of the clock.

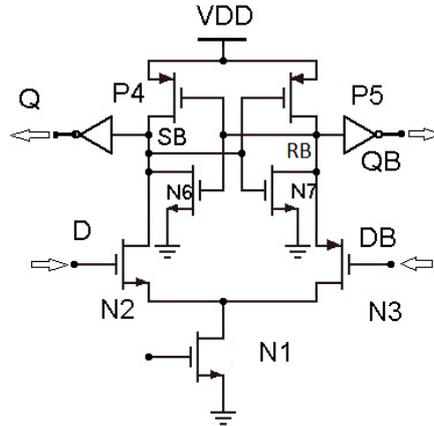


Figure 1. Dual-edge triggered static pulsed Flip-flop structure

Once the PULS signal is generated by the pulse generator circuit, both NMOS pass transistors N1 and N2 are switched ON to pass the input data so that either SB or RB will be discharged. The explicit pulse generator is simple and suitable for dual-edge triggering. The static feature of DSPFF eliminates unnecessary transitions which help in reducing power dissipation. Symmetrical rise time and fall time delays can be obtained by sizing the transistors aspect ratios optimally. Due to the large capacitive loads at the SB and RB nodes the flip-flop latency may be degraded. Moreover because of high-voltage drop across transistor N3 or N4 when they are OFF, DSPFF design suffers from high leakage current.

1.2. Dual Edge Triggered Sense Amplifier Flip-Flop (DESAFF)

Dasari [9] introduced a new technique for implementing a low energy dual edge triggered flip flop. The schematic diagram of DET-SAFF is given in Figure 2. The design consists of three stages: the dual pulse generating stage, the sensing stage to reduce the time of signal propagation and the latching stage. The DET-SAFF uses same simple pulse generator [6]. The dual edge triggered pulse generator produces a narrow pulse signal at the rising and falling clock edges. In a sense amplifier based flip-flop in the evaluation phase, as soon as D is low SB will be set to logic high, and if D is high RB will be set to logic high. To avoid redundant transitions at major internal nodes the conditional precharging technique is applied in the sensing stage of DETSAFF.

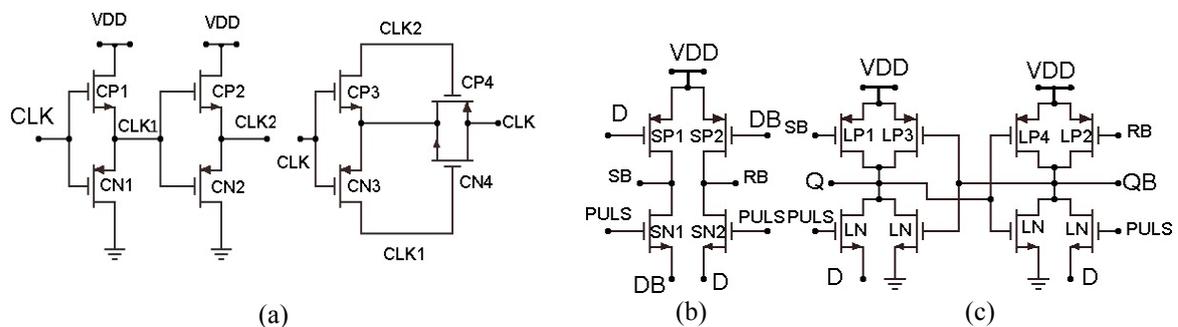


Figure 2. Dual edge-triggered Sense Amplifier flip-flop (DESAFF): (a) Dual pulse generator (b) Sense amplifier flip flop (c) Symmetric Latch

SP1 and SP2 are the two input controlled PMOS transistors which are embedded in the precharge paths of nodes SB and RB respectively. Thus if D remains at high logic for n clock cycles, SB may only be discharged during the first clock cycle. For the remaining clock cycles SB will be floating when PULS remains low. RB only needs to be precharged in the first clock cycle and it remains at its high state for the following cycles. A fast symmetric latch was developed to increase speed. DESAFF design suffers from unnecessary transitions which results in more power consumption.

1.3. Low Power Dual Edge Triggered Flip-Flop (DEPFF)

Dasari [9] introduced a dual-edge triggered flip-flop with low power and high performance. The flip-flop design has two stages. These are dual-edge triggered pulse generator stage and latching stage. The schematic of latching stage is shown in Figure 3. The pulse generator generates narrow pulse at both the rising edge and falling edge of the clock. In the latching stage, the output of the latch can follow the input data quickly.

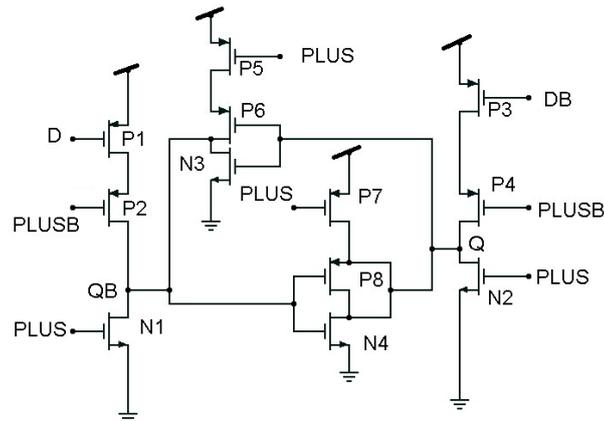


Figure 3. Low Power dual edge triggered flip-flop

When there is a pulse at the latching stage D and DB can help the Q and QB charge or discharge directly. Hence the Clock-to-Q delay effectively reduces which improves the speed of the flip-flop. The efficiency of the design depends upon the width of the clock pulse generated. Moreover the clock generator stage consumes more power due to switching activity.

2. RESEARCH METHOD

The Proposed design incorporates signal feed through technique to reduce the switching delay. Two pass transistors N1 and N2 controlled by the clock are included so that input data can drive node X1 and X2 directly. Node X1 feeds the first stage of inverters formed by transistor P1 and N4 while node X2 feeds the inverter stage formed by transistors P2 and N3 as shown in Figure 4. Transistors P1 and N4 along with pass transistors N1 form inverted master latch M1. While transistors P2 and N3 along with pass transistor N2 forms inverted master latch M2. Transistors N6, N5, N8 and P4 comprises slave latch S. These two inverted latches M1 and M2 are triggered in alternative clock levels which are controlled by two complementary signals CLK and CLK bar. As a result; the proposed DETSFF does not require extra power to overwrite the latch. A static slave latch stores the data from each inverted latch in alternative clock phases. For example, during phase 1 i.e. rising CLK and falling CLKbar, transistor N2 is turned ON while transistor N5 is turned OFF. As a result, the master latch 2 is activated and isolated from the slave latch. The input data passes through the master latch and updates the node X1. The parasitic capacitance at node X1 serves as a temporal storage for the input data, which will update the slave latch in the next clock phase. Since transistor N1 is turned OFF and transistor N6 is turned ON. The master latch 1 is deactivated and coupled to slave, thus the slave latch gets updated with the value stored at node X1.

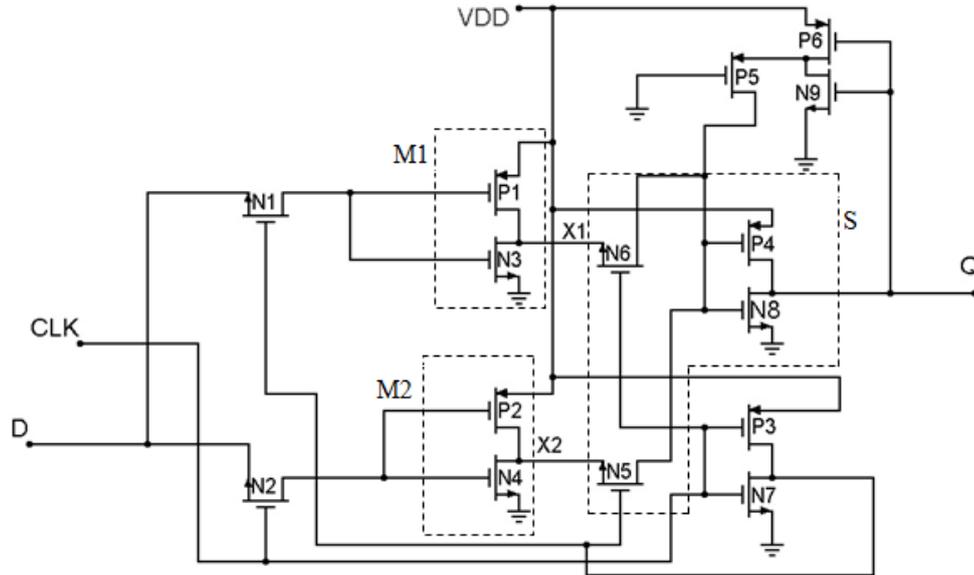


Figure 4. Proposed DETSFF Design

During phase 2, i.e. falling CLK and rising CLKbar the role and operation of the master latches 1 and 2 is reversed. In this clock phase, master latch 2 is deactivated and coupled to the slave latch, whereas master latch 1 is activated and disconnected from the slave latch. The slave latch is refreshed with the data stored at node X2. Therefore the D logic is shifted to Q at each transition.

3. RESULTS AND ANALYSIS

Spectre pre layout and post layout simulations were performed to verify the design. The simulation parameters used are presented in Table 1.

Table 1. Simulation Parameters

Model File	BSIM3v3
Nominal Conditions	1.8V , 27° C
Rise Time	25ps
Fall Time	25ps
Clock Frequency	800MHz

3.1. Simulation Results

Different data input sets were applied and power dissipation was calculated at different switching factor (α). The results for power dissipation on different input data sets are shown in Table 2, which clearly indicate that power dissipation increases with increase in switching factor.

Table 2. Average Power Dissipation at Different Input Data Sets

Sr. No	Input Set	Power in (μ w)
1	00001011	21.29
2	00011010	22.27
3	01010011	26.33
4	01010110	27.26
5	01010101	28.83

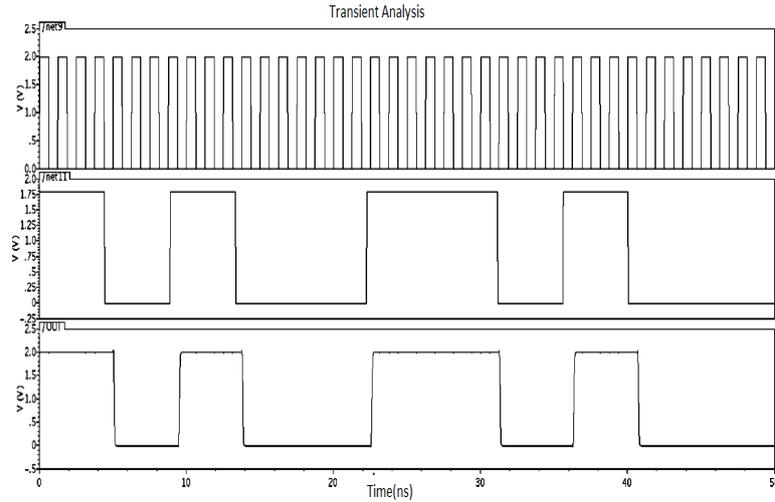


Figure 5. Simulation Waveforms

Figure 5 represents the obtained simulation waveforms. The first waveform represents clock, the middle waveform indicates data input and the last waveform reflects output. Figure 6 represents average power consumption measured for different data switching activity (%) at different supply voltages which clearly indicates the strong dependence of power dissipation on supply voltage and α .

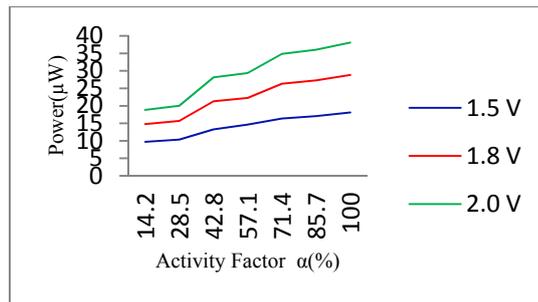


Figure 6. Power Dissipation at different α (%)

The variation of clock to Q delay with different values of rise time and fall time keeping same input data set is plotted in Figure 7. The clock to Q delays keeps on increasing with increase in Rise/Fall time.

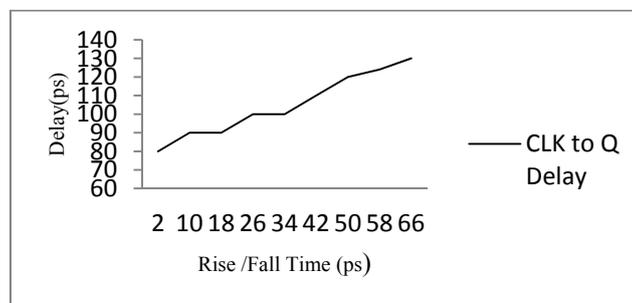


Figure 7. CLK to Q Delay at Different values of Rise/Fall time

The layout of proposed structure was designed in cadence virtuoso layout editor and is presented in Figure 8. The area of the designed layout is $66.47108 \mu\text{m}^2$.

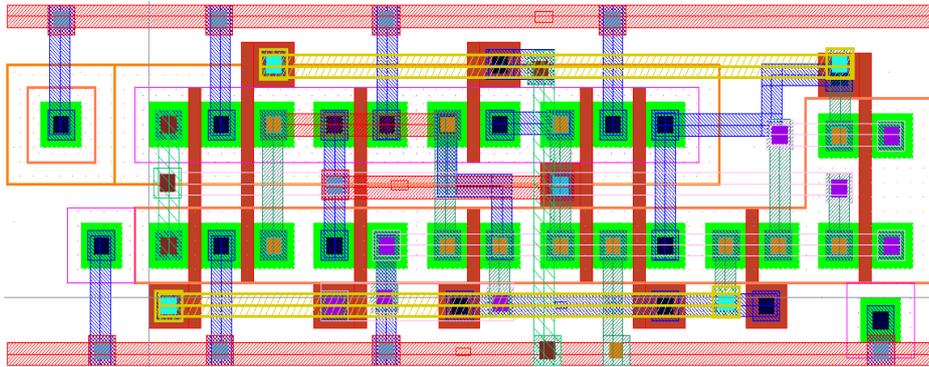


Figure 8. Layout Design for the proposed DETFF

Based on the obtained simulation waveforms the set-up time and hold time of the designed flip flop is found to be equal to 25 ps and 7 ps respectively.

3.2. Results Comparison Analysis

In this section obtained results are compared with the existing designs.

Table 3. Comparison Analysis

Transistor Count	Delay (ps)	Power (W)	PDP (fJ)	Design
15	79	26.02μ	2.055	This Work
25	2500	1.42m	3550	DESAFF
18	4000	1.99m	7960	DESPFF
20	7300	140μ	1020	DEPFF

Table 3 shows the parameters of the proposed design, such as power, delay, and number of transistors, power delay product compared with different existing dual edge trigger flips flop designs such as DESPFF [8], DESAFF [9], and DEPFF [9]. Obtained results shows that proposed DETSFF offers 98.6%, 98.16%, 81.4% reduction in power dissipation, 16.66%, 40%, 25% reduction in area, when compared to DESPFF, DESAFF, and DEPFF respectively. Results can be presented in figures, graphs, tables and others that make the reader understand easily [2], [5]. The discussion can be made in several sub-chapters.

4. CONCLUSION

A dual-edge triggered static flip-flop is proposed for low-power and high-performance applications. The proposed structure has lesser number of transistors thus leading to lesser area. Based on obtained simulation results, the proposed DETSFF offers improvement in power dissipation by 81% and offers 96% improvement in performance in terms of clock to Q delay.

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