

A 5.9 GHz Low Power and Wide Tuning Range CMOS Current-controlled Ring Oscillator

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ABSTRACT

Designing low power, low noise, wide tuning range and small size circuit in one single chip is very challenging. This paper describes a low power, wide tuning range three-stage current-controlled ring oscillator (CCO) which has been designed on 0.18 μ m CMOS technology. The CCO circuit has a tuning range from 251 MHz to 5.5 GHz or it has a tuning width of 183%. Using 1.8V supply voltage, the CCO circuit consumes current from 144 μ A to 9.76mA. Phase noise is -104 dBc/Hz at 5.5 GHz and 4MHz offset frequency. FoM is -154.4 dBc/Hz which is the best among published counterpart papers. The size of the core oscillator circuits without bonding pads is only 0.0003 mm².

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1. INTRODUCTION

Oscillator is a crucial component in phase-locked loop (PLL) and phase locked loop is one of the key elements in many communication devices and circuits. According to its controlling input, oscillator can be classified into two groups, voltage-controlled oscillator (VCO) and current-controlled oscillator (CCO) as shown in Fig. 1(a) and 1(b). Among the oscillator types, LC oscillator is widely used because it has better phase noise. However, LC oscillators have narrow tuning range and need large die area. Ring oscillators on the other hand provide wide tuning range, relatively constant voltage swing and low voltage operation [1], [2], [7]. These oscillators also require less die area compared with LC counterpart and can be built in any standard CMOS processes.

Various topologies of ring oscillator circuits have been reported in the literatures. Among them, three-stage ring oscillator topology has been reported successfully in [8], [11] and [12]. This success makes three-stage topology very attractive.

This paper presents the analysis and design of 5.5 GHz controlled oscillator in which its frequency varies linearly with its load current source or it can be written as a current controlled oscillator (CCO). Circuit architecture is described in Section II along with a simplified analysis for its frequency of oscillation. Section III presents oscillator design and post layout simulation results. Finally, Section IV concludes the paper.

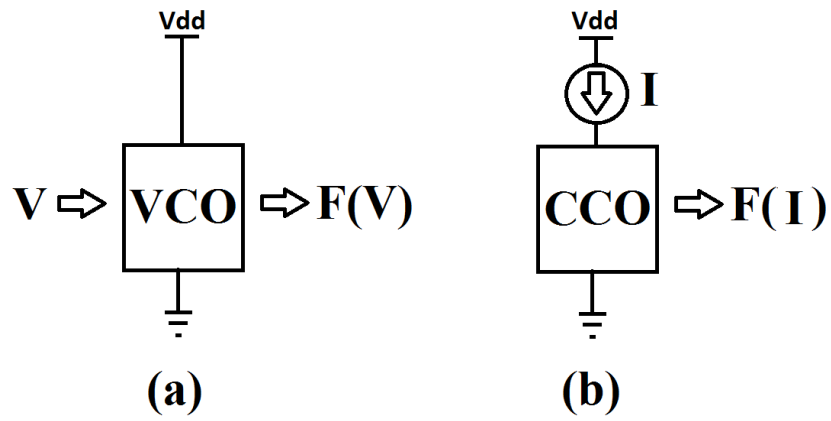


Figure 1. A block diagram of a VCO (a) and CCO (b).

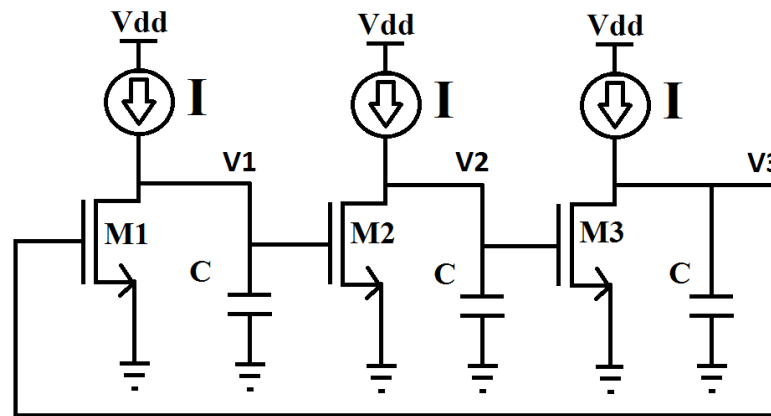


Figure 2. Circuit of the proposed three-stage ring oscillator with current load.

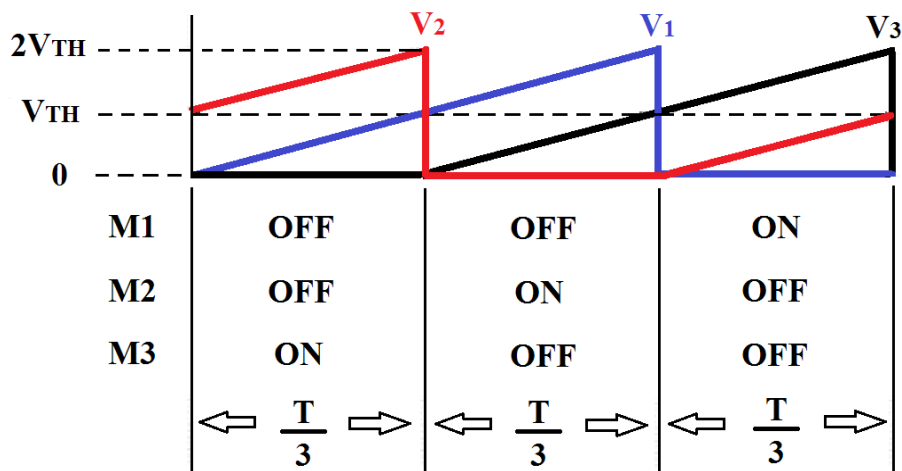


Figure 3. Simplified steady state oscillating waveforms.

2. CIRCUIT ARCHITECTURE

Fig. 2 shows general topology of the proposed current-controlled ring oscillator. It is based on a three-stage inverting ring oscillator [2]. Inverting stage consist of NMOS inverters driving a current source. Current source can be implemented by using resistive load circuit.

A simplified analysis of this circuit by using a switch model of NMOS is provided by [5]. The NMOS assumed becomes short circuit when its gate-source voltage V_{GS} exceeds its threshold voltage V_{TH} . By this assumption, only one NMOS can turn on at any given time. Assumed the three NMOS devices are identical or in other word they have same V_{TH} , the total period T can be divided equally by the ON duration of each transistor as shown in Fig. 3.

It can be seen from the picture that one NMOS can turn on for $T/3$ period and turn off for another $2T/3$ when the charging process in the capacitor is taking place. An NMOS is ON when its gate voltage reach threshold voltage (V_{TH}) and OFF when its gate voltage reach $2V_{TH}$. Voltage rises from V_{TH} to $2V_{TH}$ in $T/3$ period. Thus NMOS is ON in $T/3$ period. For example, in the first $T/3$ periode when the output of M1 (V_1) rises from zero to some point before V_{TH} , the next transistor (M2) is still turned off. M2 is turned on when V_1 reach some point above V_{TH} . M2 is turned on until V_1 reach $2V_{TH}$ in $T/3$ period. When M2 turn on, its output (V_2) goes to ground. Thus, because V_2 supply the gate of M3, M3 change its state from turning on to turning off which then the charging process of C_2 is taking place. Each transistor is turned on for $T/3$ when its output is zero and it is turned off for another $T/3$ during charging time of output capacitor by I . Thus, the output rises from zero at a slope of I/C and then turn on the next transistor in the ring. Therefore, based on this mechanism, we can derive formulae to obtain the period of the oscillation as follows

$$T = \frac{3C}{I} V_{TH} \tag{1}$$

Thus

$$f = \frac{I}{3CV_{TH}} \tag{2}$$

It shows that frequency varies linearly with current which is a desirable property for phase-locked applications. The minimum supply voltage can be calculated by looking at the maximum output voltage $2V_{TH}$ added by the minimum operating voltage of the current source as below

$$V_{DD}(\min) = 2V_{TH} + V_I \tag{3}$$

where V_I is the minimum operating voltage of the current source that can be minimized by the use of PMOS device as current source. It can be as low as PMOS overdrive voltage.

In practice, steady state oscillating waveform cannot behave as ideal as shown in Fig. 3 because the circuit needs a small duration (δ) for discharging each output capacitor since an NMOS cannot have zero resistance when turn on. Fig.4 illustrates this behavior.

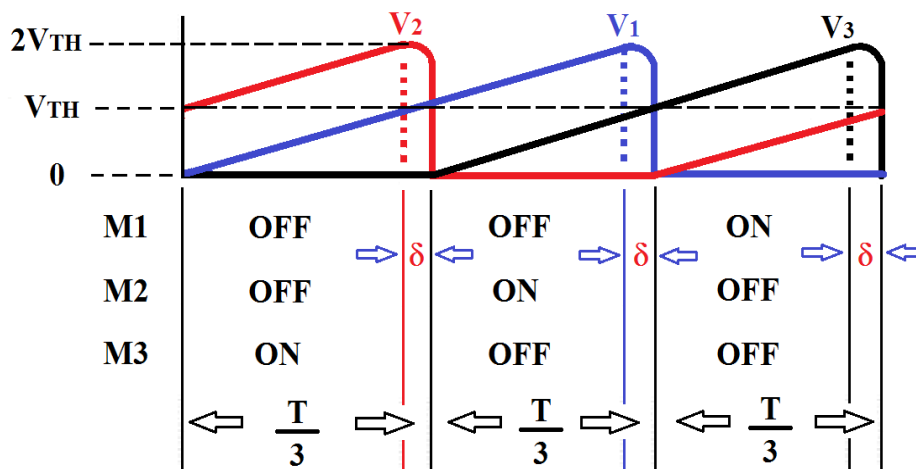


Figure4. Steady state waveforms when each NMOS has finite W and L .

This behavior has an increasing effect on its period of oscillation (T), which is derived as follows.

$$V_{TH} = V_L + \frac{\left(\frac{IT}{3} - I\delta\right)}{C} \quad (4)$$

$$V_H = V_{TH} + \frac{IT}{3C} \quad (5)$$

where $V_L \approx 0$ is the minimum drain voltage of an NMOS to carry current. The dynamic equation during this duration is derived as

$$C \frac{dv}{dt} = I - \frac{I^2 t^2 \beta}{2C} \quad (6)$$

where voltage at $t = 0$ to δ is V_H and V_{TH} , while $\beta = \mu_n C_{ox} \frac{W}{L}$

By doing some integration and algebraic manipulation at the above equations, we can come up with an exact formulae to determining T as given by

$$T = \frac{3C \left((V_{TH} - V_L) + \sqrt[3]{\frac{n}{2} + \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} + \sqrt[3]{\frac{n}{2} - \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} \right)}{I} \quad (7)$$

3. CIRCUITS DESIGN AND POST LAYOUT SIMULATION RESULTS

Fig.5 shows the core circuit of the proposed current-controlled oscillator circuit. M1, M2, M3 are the main inverting stage, while M4, M5, M6 are the resistive load circuits. However, resistive load devices that commonly formed using NMOS static inverters are now replaced by PMOS resistive load so that power consumption depends directly on the current. Hence, spike that is caused by voltage supply which is typically found in a static inverter has been removed. Using PMOS as current source made V_{DS} can be as low as overdrive voltage that increases output voltage swing. PMOS load gate is operated in saturation region by connecting the gate to ground to obtain maximum current load. There is no capacitance used in order to get high frequency output, but there are parasitic capacitances at the output nodes that cannot be eliminated which can reduce frequency output.

The chip is implemented in $0.18\mu\text{m}$ CMOS technology. Picture of the chip layout is shown in Fig. 6. The size of the core oscillator and digital control circuits include bonding pads is 0.09 mm^2 (0.0003 mm^2 without bonding pads). This is noted as the smallest chip area compared to the published papers.

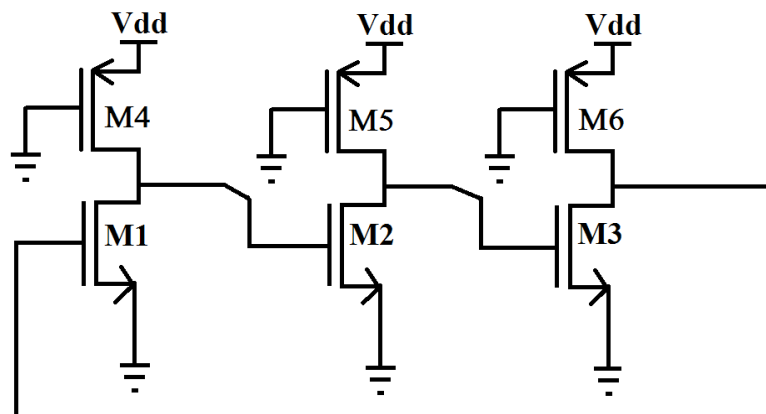


Figure 5. Schematic of the designed circuit.

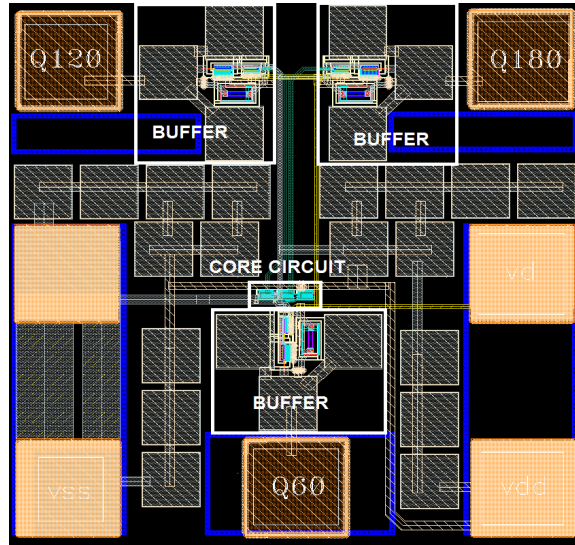


Figure 6. Chip layout of the proposed CCO

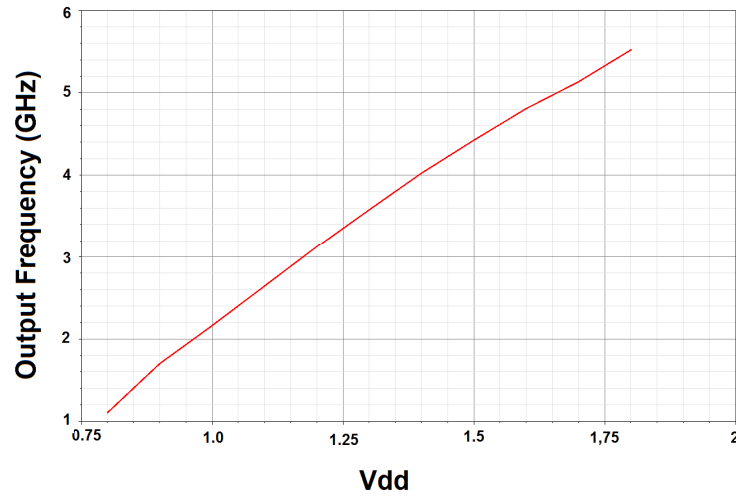


Figure 7. Tuning curve of the proposed CCO.

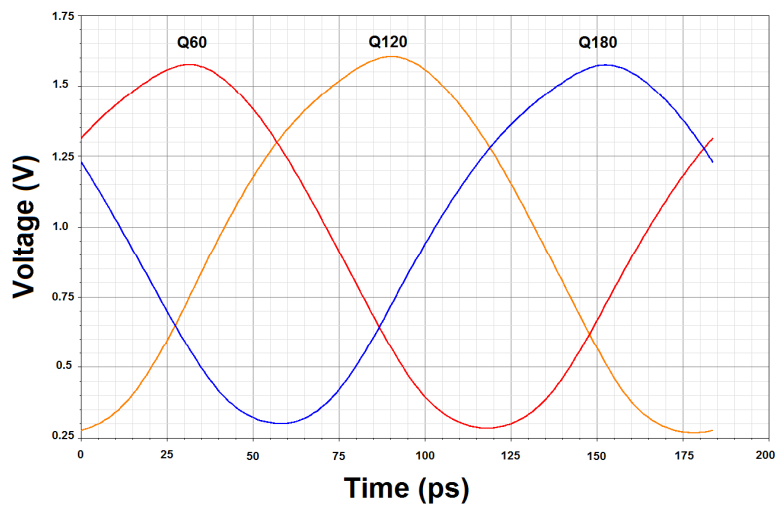


Figure 8. Output waveform at 5.5 GHz.

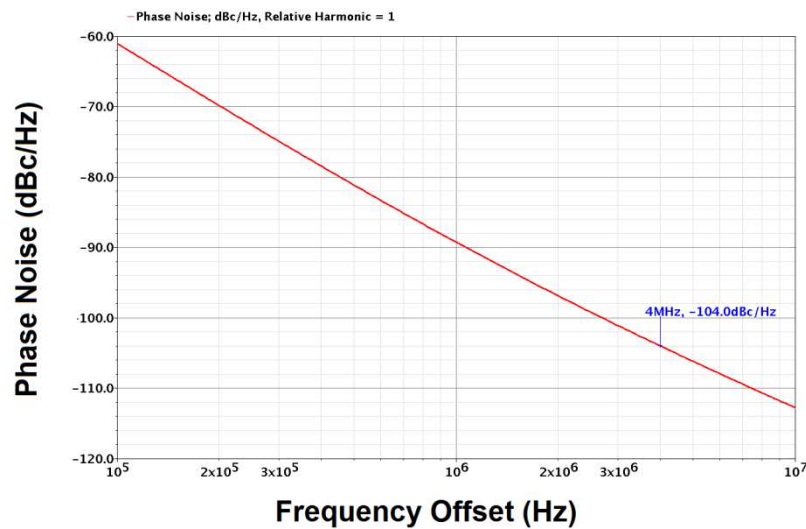


Figure 9. Phase noise of the proposed current-controlled oscillator at 5.5 GHz

Table 1. Performance Comparison.

Ref.	Freq. (GHz)	Technology	Pdc (mW)	Area (mm ²)	Tuning range	PN (dBc/Hz)	Offset (MHz)	FoM (dBc/Hz)
[8]	2	BiCMOS 0.6 μm	17	0.023	19%	-75	1	-140.2
[9]	2.2	BiCMOS 0.5 μm	100	0.5	84%	-106	2	-146.8
[3]	3.6	CMOS 0.18 μm	17	0.24	70%	-90.1	1	-148.9
[10]	2.2	BiCMOS 0.6 μm	11.8	-	-	-94	1	-150.3
[4]	11.5	BiCMOS 0.5 μm	75	0.13	16%	-94.3	2	-150.7
[12]	3.5	CMOS 0.18 μm	16.2	-	189%	-106	4	-152.7
[11]	10	inP HBT	250	0.85	-	-97	1	-153
[6]	1.8	Bipolar	22.5	-	32%	-82	1	-153.6
This work	5.5	CMOS 0.18 μm	17.5	0.0003	183%	-104	4	-154.4

----- Not Available

Fig. 7 shows the measured CCO tuning range. It shows a linear tuning curve. Tuning range is obtained by varying its voltage supply from 0.8V to 1.8V resulting output frequencies from 251 MHz to 5.5 GHz or about 183% wide. Output waveform in 5.5 GHz is shown in Fig. 8 which shows voltage swing more than 1.5 Volt. Phase noise -104 dBc/Hz at 4 MHz offset frequency from 5.5 GHz carrier frequency is shown in simulation result in Fig. 9. Current consumption noted as low as 9.76 mA at 1.8V supply voltage. At 251 MHz, phase noise and power consumption is -79 dBc/Hz and 68.4 mW respectively.

Table I summarize and compare the performance of the proposed current-controlled oscillator (CCO) to the recently published papers on the same technology. It can be seen that the proposed (CCO) has the best FoM performance. It has also wider tuning range. The proposed CCO also exhibits a low power for high frequency output with adequate phase noise. Figure of merit (FoM) of the proposed CCO is -154.4 dBc/Hz, by using FoM definition as

$$FoM = -20\log\left(\frac{f_o}{\Delta f}\right) + L(\Delta f) + 10\log P_{dissp(mW)} \quad (9)$$

with f_{osc} , $1/f$, $L(1/f)$, and $P_{dissp(mW)}$ denoting oscillation frequency, offset frequency, phase noise in dBc/Hz and power consumption in mW, respectively.

4. CONCLUSIONS

In conclusion, a CMOS three-stage current controlled ring oscillator based on an inverting NMOS with current load is analyzed and designed. The post layout simulation shows that the proposed current-controlled oscillator (CCO) circuit consumes small current to produce high frequency output. The proposed CCO has better performance compared to the published referred papers. FoM comparison result shows proposed CCO to be the best among published results. It has linear and wide tuning range and has very small chip area which makes it suitable for PLL and clock generation.

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