Capacitance-Voltage Characteristics of Nanowire Trigate MOSFET Considering Wave Function Penetration

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Article Info	ABSTRACT
	Short channel effects on the gate capacitance of nanowire trigate MOS field-effect transistors are studied considering wave function penetration. Capacitance-Voltage (C-V) measurements are commonly used in studying gate-oxide quality in detail. C-V test results offer a wealth of device and process information, including bulk and interface charges. Capacitance indicates switching speed of the MOSFET. It is our goal to minimize capacitance as possible as we can in MOSFET. Due to our necessary to compact the Integrated Circuit as possible as we can for getting small electronics devices. Capacitance determines the speed of the IC. Every engineer in this section should know capacitance of his implementing device MOSFET to get exact result from this device. Whenever we deal with 10X10 nm scale or less device of MOSFET. We must concern the effect of wave function penetration into device in this stage classical mechanics fails to describe exact result of the system because electron can move in only one direction (x), in 3 Dimension, it cannot move in other two direction (y, z). i.e. confined in two direction which is not predictable by classical mechanics here quantum mechanics (QM) gives better solution of this problem. Therefore we consider QM in our study. Here we presented how wave function play vital role considering small area of trigate MOSFET. It is the analytical approach of QM and highly recommendation to use QM rather than CM to get accuracy. This result will be helpful for determining capacitance of trigate MOSFET.

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1. INTRODUCTION

Trigate is a new technology which controls gate current using three wing around silicon dioxide of MOSFET. This device is called nanowire because its gate length is less than 100nm. Wave function penetration becomes vital role when cross section area of silicon of MOSFET becomes less than 10x10nm. We will consider 7x7 nm cross section area of silicon and channel length is 20 nm. Which is shown in Fig. 1 We also consider SiO_2 as insulator and Aluminum as electrode in our simulation. It is necessary to know the capacitance-voltage characteristics of trigate MOSFET whenever we implement this type of MOSFET. As transistor per chip is reducing day by day so we have to consider quantum mechanics not classical mechanics because quantum mechanics give actual probability of C-V characteristics than classical mechanics. To get actual result from quantum mechanics we use self –consistent of Schrödinger-Poisson's solver. Capacitance has mainly three region namely accumulation region, depletion region and inversion region. Actually inversion layer becomes volume inversion in our selected area this is cause of quantum effect.

2. THEORY

The I-V model is adequate only for describing the DC behaviour but for transient description the capacitances are absolutely essential. The intrinsic capacitances of the transistor are derived from the terminal charges. The charge on the top and bottom gate electrodes is equal to total charge in the body. The total charge is computed by integrating the charge along the channel since the two gates are electrically interconnected, we have [1]
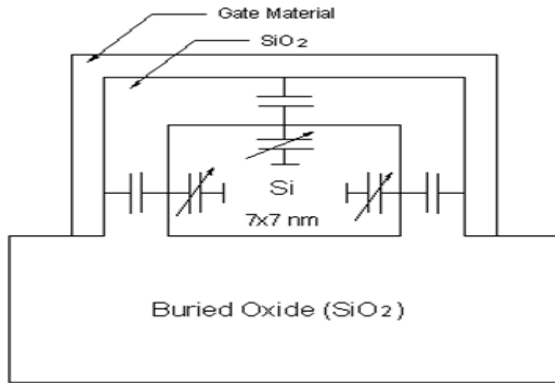
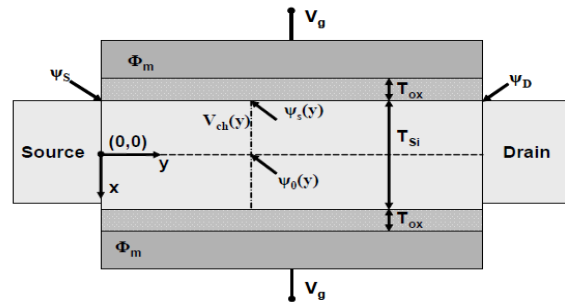Figure 1. Cross section area of nanowire trigate MOSFET.

Fig. 2 Schematic of the symmetric common-gate DG-FET.

$$Q_g = 2WC_{ox}\int_0^L \left(V_g - V_{fb} - \psi_s(y)\right) \cdot dy$$

(1)

Where
Q_g = the charge on the electrically interconnected gate.
$\Psi_s(y)$ = surface potential as a function of the position y along the length of the transistor.

The inversion charge in the body is divided between the source and drain terminals using the Ward-Dutton charge partition approach [2].
The charge on source terminal (Q_s) is:

$$Q_s = -2WC_{ox}\int_0^L \left(1 - \frac{y}{L}\right) \cdot \left(V_g - V_{fb} - \psi_s(y) - \frac{Q_{bulk}}{C_{ox}}\right) \cdot dy$$

(2)

Where
V_g = the gate voltage.
Q_{bulk} = bulk charge = $\sqrt{2q\varepsilon_{Si}N_A\psi_{pert}}$
Ψ_{pert} = perturbation potential.
V_{fb} = the flat band voltage.

Using charge conservation, the charge on drain terminal (Q_d) can be expressed as:

$$Q_d = -2WC_{ox}\int_0^L \frac{y}{L} \cdot \left(V_g - V_{fb} - \psi_s(y) - \frac{Q_{bulk}}{C_{ox}}\right) \cdot dy$$

(3)

The surface potential as a function of the position y along the length of the transistor ($\Psi_s(y)$) is obtained using current continuity. Current continuity states that the current is conserved all along the length of the transistor.

$$I_d(L) = I_d(y) \quad \text{where} \quad 0 \le y \le L$$

$\Psi_s(y)$ can be related to Ψ_S and Ψ_D by

$$\frac{y}{L} \cdot (B - \psi_S - \psi_D)(\psi_D - \psi_S) - (B - \psi_S - \psi_s(y))(\psi_s(y) - \psi_S)$$

where

$$B - 2\left(V_g - V_{fb} - Q_{bulk}\Big/C_{ox} + 2\,kT\Big/q\right)$$

Ψ_D = the surface potential at the drained .

Ψ_S = Surface potential at source terminal.

$$\psi_s = 2\frac{kT}{q}\left[\ln(\beta) - \ln(\cos(\beta)) + \ln\left(\frac{2}{T_{Si}}\sqrt{\frac{2\varepsilon_{Si}kTN_A}{qn_i^2}}\right)\right] + \psi_{pert}$$

Where

$$\beta = \frac{T_{Si}}{2}\sqrt{\frac{q^2}{2\varepsilon_{Si}kT}\frac{n_i^2}{N_A}}\,e^{\frac{q(\psi_0(y) - V_{ch}(y))}{kT}}$$

Where

$V_{ch(y)}$ = the channel potential.

$\Psi_{0(y)}$ = the potential at the center of the body.

The terminal charges are obtained by substituting Ψ_S (y) in Eqs. (1-3) and evaluating the integrals

$$Q_g = 2WLC_{ox}\left(V_{gs} - V_{fb} - \frac{\psi_S + \psi_D}{2} + \frac{(\psi_D - \psi_S)^2}{6(B - \psi_D - \psi_S)}\right)$$

$$Q_d = -2WLC_{ox}\left(\frac{V_{gs} - V_{fb} - Q_{bulk}\Big/C_{ox}}{2} - \frac{\psi_S + \psi_D}{4} + \frac{(\psi_D - \psi_S)^2}{60(B - \psi_D - \psi_S)} \right.$$
$$\left. + \frac{(5B - 4\psi_D - 6\psi_S)(B - 2\psi_D)(\psi_S - \psi_D)}{60(B - \psi_D - \psi_S)^2}\right)$$

$$Q_i = -(Q_{fg} + Q_{bg} + Q_{bulk} + Q_d)$$

(4)

The expressions for terminal charges are continuous and are valid over sub-threshold, linear and saturation regimes of operation. The terminal charges are used as state variables in the circuit simulation. All the capacitances are derived from the terminal charges to ensure charge conservation. The capacitances are defined as:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

(5)

Where, i and j denote the multi-gate FET terminals. Note that C_{ij} satisfies

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

(6)

Effect of Quantum mechanics on capacitances

         Using a self-consistent Schrodinger–Poisson solver, we can analyze the effect of wave function penetration on the capacitance. The study reveals that accounting for wave function penetration into the gate dielectric causes carrier profile to be shifted closer to the gate dielectric reducing the electrical oxide thickness. This shift increases with increasing gate voltage. This shifting results in an increased capacitance.

         It is well known that direct tunneling currents become significant in this regime and that the penetration of the wave function cannot be neglected [3]–[4], the capacitance of NMOS capacitors in the inversion region accounting for wave function penetration into the gate dielectric. The physical basis has been presented in [5] and [6].

         In this work, the Schrodinger and Poisson equations are used self consistently assuming that the wave function penetrates the gate dielectric. The wave function is assumed to go to zero at some point deep

inside the substrate, while a travelling wave boundary condition is imposed at the gate dielectric-gate electrode interface. The wave function inside the gate dielectric is connected to the asymptotic wave function in the gate electrode using the quantum transmitting boundary method [7].

The gate capacitance under strong-inversion conditions can be described by the equivalent circuit shown in Fig. 3 consisting of the oxide capacitance C_{ox} and the inversion-layer capacitance C_{inv} [8], [9]. The latter includes the contributions of both the electrostatic capacitance $C_{es,Si}$ and the quantum capacitance C_q [10] of the inversion layer. While $C_{es,Si}$ is related to the average distance of the channel electrons from the Si/SiO2 interface, C_q is related to the Density of States (DOS) in the inversion layer.
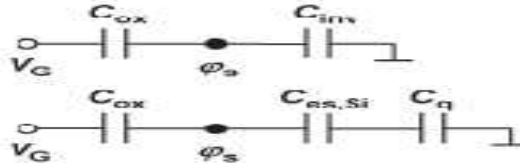

Fig. 3 Equivalent circuit for the gate capacitance in silicon MOS structures.

Where
C_q = quantum capacitance.
$C_{es,Si}$ = electrostatic capacitance.
C_{ox} = oxide capacitance .
C_{inv} = inversion-layer capacitance.

3.   RESULTS AND ANALYSIS

In the literature [3], Schrodinger's equation has been solved by forcing the wave function to zero at the dielectric-gate electrode boundary.

The C-V characteristics have come by solving Schrodinger-Poisson equation. The following figures indicate that how wave function penetration play vital role in the case of small thickness of oxide. In our simulation we present wave function penetration in the gate electrode.

The C–V calculated assuming such a border condition differ by an immaterial quantity from the C–V calculated by letting the wave function penetrate into the gate electrode.
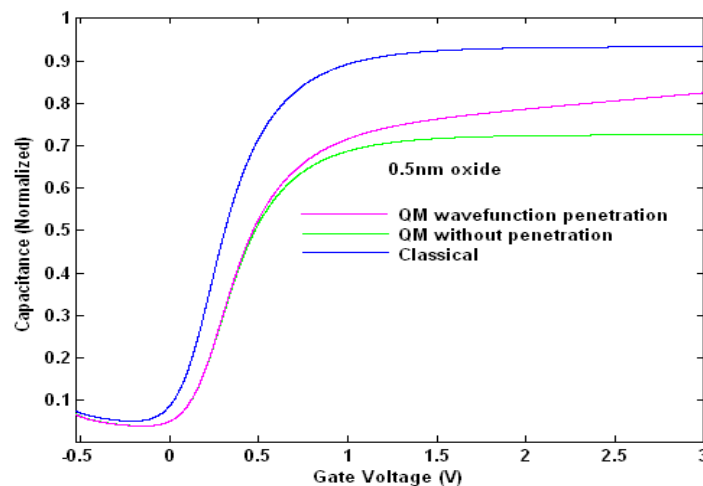

Fig. 4 Normalized classical and quantum mechanical capacitance obtained with and without wave function penetration for 0.5 nm oxide capacitor.

The classical and quantum-mechanical C–V individuality with and without wave function penetration for a metal– SiO_2 –Si system of gate oxide thicknesses 0.5 nm and 3.0 nm are exposed in Fig. 4 and 5 correspondingly. The capacitances are normalized to the strong inversion.
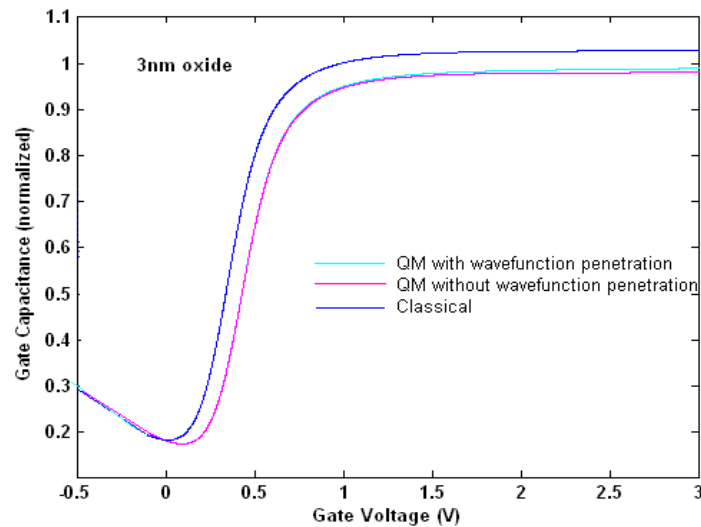
Fig. 5 Normalized classical and quantum mechanical capacitance obtained with and without wave function penetration for 3 nm oxide capacitor.

Classical capacitance values help for comprehending the impact of accounting for wave function penetration. It can be undoubtedly seen that the impact is larger for the 0.5 nm gate oxide case. There are two effects that contribute to the considerably superior impact for the 0.5 nm case. Firstly the field across the 3 nm gate oxide device is weaker than the field across the 0.5 nm device. Secondly the percentage contribution of the shift of the wave function closer to the interface is larger for the 0.5 nm gate oxide device the impact of this shift would be larger for the thinner oxide case.
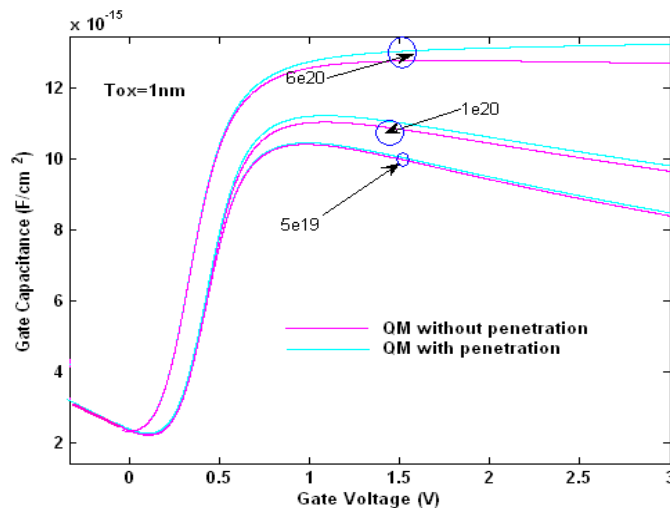

Fig. 6 Capacitance values for a 1.0 nm gate oxide capacitor with different doping with and without wave function penetration.

The C–V simulations discussed thus far were performed on devices with a metal gate. However, despite detrimental effects, poly silicon is still being used as the gate electrode. Hence, simulations were also performed with poly silicon replacing the metal as the gate electrode. The simulation results (Fig. 6) show that the wave function shift by the wave function influences the C–V significantly only for poly doping of greater than 1×10^{20} cm. This seems to indicate that the poly-depletion effect dominates over the shift effect due to wave function penetration and the models developed so far seem sufficient. It must, however, be pointed out that as the devices are scaled down to sub-20 nm gate lengths, metal gate electrodes will have to be used to obtain lower effective oxide thicknesses and higher capacitance values. Thus when metal gate electrodes are used the effect of wave function penetration will have to be considered.

Accounting for wave function penetration into the gate electrode causes a shift in the wave function closer to the interface, the more so the greater the voltage. This bias dependent shift results in a lower electrical oxide thickness and hence higher gate capacitance. The poly depletion effect is dominant over the wave function penetration effect. However, this effect is significant when highly doped poly silicon gates are used and will become significant when metal gate electrodes are used and the oxide thickness is reduced.
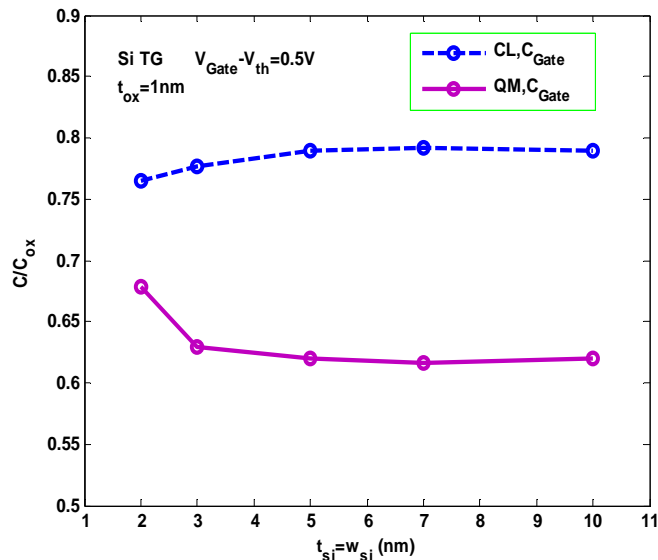

Fig. 7 gate capacitance normalized to the C_{ox} of trigate MOS structures as a function of the silicon cross section. (continuous line) Quantum–mechanical and (dash line) classical results are compared.

Fig. 7 the gate capacitance is shown normalized to C_{ox}, i.e., the maximum achievable capacitance value for every structure, as a function of the silicon size. We have linked this to quantum effects since no increase in C_G/C_{ox} has been observed from classical calculations. The gate capacitance of trigate MOS structures is affected by quantum effects are compared. From Fig. 7 a continuous increase in the C_G/C_{ox} ratio can be observed as the channel cross section is scaled below 7 nm x 7 nm. We have actually observed an increase in the C_G/C_{ox} ratio mainly via the spatial electron distribution. The quantum effects on C_q have been found to be less important for the gate capacitance except for very small cross sections in the order of 2 nm ✕ 2 nm.

4.   CONCLUSION

A comprehensive analysis of the effects of wave function penetration on the capacitance of NMOS capacitors has been observed. The study reveals that accounting for wave function penetration into the gate dielectric causes carrier profile shifted closer to the gate dielectric reducing the electrical oxide thickness. This shift increases with increasing the gate voltage. In this work we present analytical solution of Capacitance-Voltage characteristics of Trigate MOSFET considering wave function penetration which is essential to consider QM rather than CM when devices are small in size. We hope it will be helpful instrument for working in practical condition.

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