

Referenced Approximation Technique for a Rom-Less Sweep Frequency Synthesizer

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ABSTRACT

The main goal of this paper is to present a novel ROM-less direct digital frequency synthesizer for sweep instrumentation systems. It provides a main sweep channel for frequency analysis and a reference channel for phase and amplitude measurement block operating at constant frequency. For phase to amplitude converter, we propose a new trigonometric approximation technique based on a set of reference angles. In addition, we present the design of the proposed synthesizer and its evaluation in Matlab-Simulink environment. The simulation results illustrate the performances and demonstrate the effectiveness of our proposed circuit.

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1. INTRODUCTION

Recent applications of sensors characterization, systems identification and digital communications require controlled frequency generators with high stability and low frequency resolution [1]-[6]. In the case of sweep frequency analysis, it is also important to improve the measurement of required parameters such as amplitude and phase shift between input and output waves. The scheme of instrumentation system is shown in Figure 1 where the control and acquisition block configures the analyzing wave frequency and acquires the outputs of the measurement block for processing and displaying results.

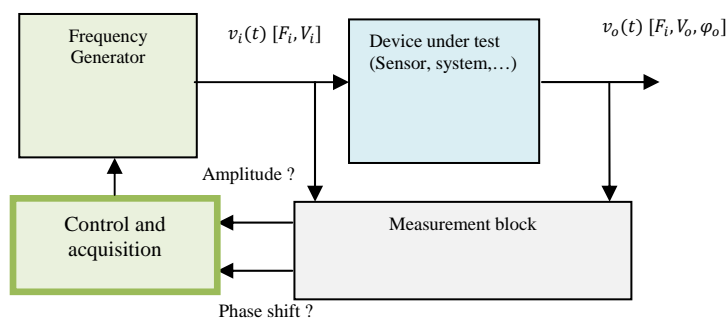


Figure 1. Block diagram of general instrumentation system

For stable measurement performances, the measurement block has to operate at constant frequency during the entire range of input frequency analysis. In the first stage, a High frequency to Low frequency conversion block is used. Figure 2 shows the structure of this conversion block where the processing signals are:

- Input signal: $v_i(t) = V_i \cos(2\pi F_i t)$;
- Output signal : $v_o(t) = V_o \cos(2\pi F_i t + \varphi_o)$;
- Reference signal: $v_r(t) = V_r \cos(2\pi F_r t + \varphi_r)$.

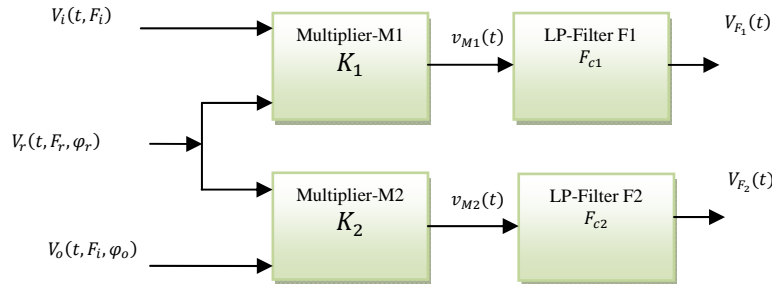


Figure 2. Diagram of HF to LF conversion block

After multiplication and low-pass filtering under the following conditions : $F_i - F_r \ll F_{c1} \ll F_i + F_r$; $F_i - F_r \ll F_{c2} \ll F_i + F_r$, we get out of the structure, two signals of same frequency $F_{mes} = F_i - F_r$ and phase shift $\varphi(V_{F2}/v_{F1}) = \varphi_o$ as expressed in Equations (1-2).

$$V_{F_1}(t) = \frac{K_1 V_i V_r}{2} \cos(2\pi(F_i - F_r)t - \varphi_r) \quad (1)$$

$$V_{F_2}(t) = \frac{K_2 V_o V_r}{2} \cos(2\pi(F_i - F_r)t + \varphi_o - \varphi_r) \quad (2)$$

In the second stage, the reference frequency F_r should follow the changes of input frequency F_i in order to keep the operating frequency F_{mes} constant. For this purpose, our work aims to study and design a novel circuit which integrates both frequency generators of analysis and reference signals. The proposed sweep frequency synthesizer, as shown in Figure 3, provides two channels such as the frequency shift remains constant. The main channel corresponds to the main output wave, whereas the reference channel will be used by the measurement block.

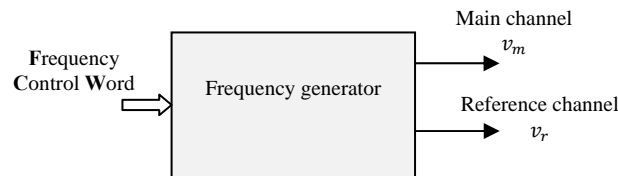


Figure 3. input-outputs of the proposed sweep frequency synthesizer

2. THEORETICAL OF THE DIRECT DIGITAL FREQUENCY SYNTHESIS

In scientific and industrial frequency generators, different techniques are used to produce the required accurate waveforms, such as analog oscillators, mixing frequencies sources or phase-locked loop circuits. Among these techniques, Direct Digital Frequency Synthesizers (DDFS) perform important specifications: low spurs level, fast switching speed, fast settling time, sub-hertz frequency resolution, continuous phase switching response and low phase noise [7],[8]. The principle of DDFS technique was introduced by Tierney in [9], and its corresponding conventional design architecture is shown in Figure 4, where the components are the following,

- **Phase accumulator:** provides the time reference as counter address of the waveform memory. It is updated at each rising or falling edge of the clock signal.
- **Waveform ROM:** contains samples of the waveform to be synthesized.
- **D/A Converter:** converts each numeric value into its proportional analog voltage.

- **Low-pass filter:** limits the spectrum of the synthesized wave at the Nyquist bandwidth related to the operating clock frequency F_{CLK} .

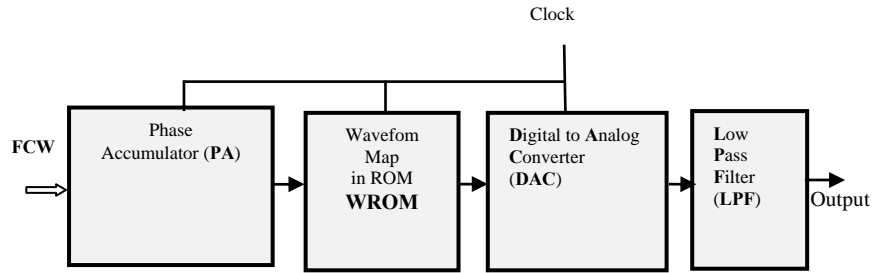


Figure 4. Conventional architecture of the ROM based DDS

The output frequency F_{OUT} depends on the reference clock frequency F_{CLK} , the frequency control word FCW and the size of the phase accumulator N , by the following expression [7]:

$$F_{OUT} = \frac{FCW}{2^N} F_{CLK} \quad (3)$$

The wave quality depends on the length of the phase accumulator, the ROM size, the ADC resolution and the order of low-pass filter. However, the most disadvantage of this architecture is the use of ROM memory which the high size requires an expensive semiconductor area and consumes a lot of power. Hence, a set of interesting approximation methods has been developed to compute directly the amplitude and then overcome the ROM inconvenient [9]-[11]. In most recent techniques, the ROM is replaced by a computation unit, called Wave Arithmetic Unit, which the complexity and the consumption power are very low. The role of this WAU as illustrated in Figure 5 is to compute the sine value of each input phase.

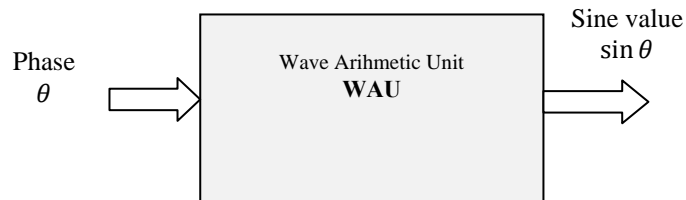


Figure 5. Architecture of the ROM free DDS

The principal methods correspond to COordinate Rotation DIGital Computer (CORDIC) algorithm, polynomial approximation as Euler infinite and chebyshev series or Taylor formulation [7],[10],[11]. An interesting work in [8], used a trigonometric approximation for small values of FCW in which the design architecture presents two advantages: low complexity (two multipliers, two adders and two registers) and one-cycle computation (no pipeline stages). However, the computation error increases strongly versus frequency control word and consequently induces a poor spurious free dynamic range. Hence, our work aims to improve this technique for the complete range of the phase accumulator with high computation precision.

3. THE PROPOSED METHOD

For a sine curve approximation, Shu-Chnug Yi proposes to compute two simultaneous quadrature outputs [8]. This technique used a difference $\Delta\theta$ between two consecutive angles (θ_k, θ_{k+1}) and Taylor's series of $\sin \theta$ and $\cos \theta$ at first order, according to the following expressions,

$$\sin \theta_{k+1} = \sin \theta_k + \Delta\theta \cos \theta_k \quad (4)$$

$$\cos \theta_{k+1} = \cos \theta_k - \Delta\theta \sin \theta_k \quad (5)$$

Thus, the DDFS wave can be computed for each value of phase. However, the frequency control word should be small enough to reduce the computation error [8]. In the proposed design architecture, the quadrature DDFS comprises two registers, two adders and two multipliers [8].

Our proposed technique aims to keep the advantages of the Trigonometric Approximation Method and also to reduce the computation wave error. For this objective, we propose to decompose the complete interval $\left[0, \frac{\pi}{2}\right]$ into r subintervals: $[\theta_k, \theta_{k+1}[$ where the reference phases $\left\{\theta_0 = 0, \theta_1, \dots, \theta_r = \frac{\pi}{2}\right\}$ have the following expression,

$$\theta_k = k \frac{\pi}{2r} ; k = 0, \dots, r. \quad (6)$$

The first order of Taylor's series of trigonometric functions in a small length subinterval $[\theta_k, \theta_{k+1}[$, allow to write: $\sin(\theta - \theta_k) = \theta - \theta_k$; $\cos(\theta - \theta_k) = 1$. Thus, we can approximate $\sin \theta$ as,

$$\sin \theta = (\theta - \theta_k) \cos \theta_k + \sin \theta_k \quad (7)$$

Furthermore, the localization of the reference subinterval corresponding to input phase allows developing two approximations methods,

- **Referenced Trigonometric Approximation Method (RTAM):** we compute the sine value in relation to θ_k as follows,

$$\forall \theta \in [\theta_k, \theta_{k+1}[; \sin \theta = (\theta - \theta_k) \cos \theta_k + \sin \theta_k \quad (8)$$

- **Symmetrical Referenced Trigonometric Approximation Method (SRTAM):** we compute the sine value in relation to distances $|\theta - \theta_k|$ and $|\theta - \theta_{k+1}|$ as follows,

$$\begin{aligned} &\forall \theta \in [\theta_k, \theta_{k+1}[; \\ &\sin \theta = \begin{cases} (\theta - \theta_k) \cos \theta_k + \sin \theta_k & \theta_k \leq \theta < \theta_k + \frac{\pi}{4r} \\ (\theta - \theta_{k+1}) \cos \theta_{k+1} + \sin \theta_{k+1} & \theta_k + \frac{\pi}{4r} \leq \theta < \theta_{k+1} \end{cases} \quad (9) \end{aligned}$$

Where the coefficients $(\cos \theta_k, \sin \theta_k)$ should be known according to the set reference angles.

To compare the computation error of these methods, we use the residual error $|\sin \theta_n - \sin \theta_n^*|$ and the mean of total square residual error TRE between $\sin \theta_n$ and its approximated value $\sin \theta_n^*$ for L points as follows,

$$TRE = \frac{1}{L} \sum_{k=1}^L (\sin \theta_n - \sin \theta_n^*)^2 \quad (10)$$

Figure 6 and Figure 7 show the residual error over the range $\left[0, \frac{\pi}{2}\right]$ according to the following parameters: phase accumulator size of $16bits$, $FCW = 200$, $r = 32$ and $r = 64$, respectively. It is clear that the Symmetrical RTAM has the least residual error than Referenced TAM and Trigonometric AM. Additional to the distribution of residual error, we evaluate the effect of the number of reference phases as presented in Figure 8. The mean of total residual error TRE decreases according to the number of reference phases which becomes an important parameter to improve the quality of synthesizers. We note that the SRTAM method has a low total residual error than the RTAM one. Hence, we retain the SRTAM approximation method for the design and the evaluation of performances in the next section. For the design, this architecture requires one multipliers against two in [8], one adder and a ROM memory to store $2 \times (r + 1)$ words corresponding to cosine and sinus reference coefficients. The required Matlab-Simulink blocks will be presented and detailed in the next section.

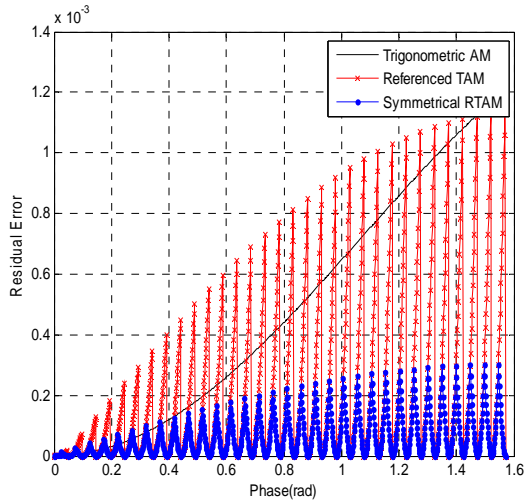


Figure 6. Residual error versus phase for $r = 32$

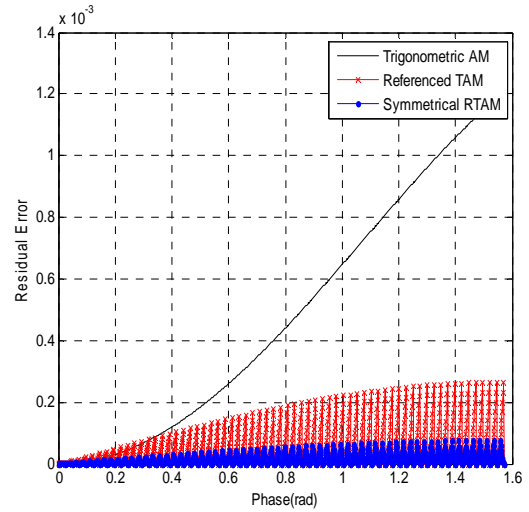


Figure 7. Residual error versus phase for $r = 64$

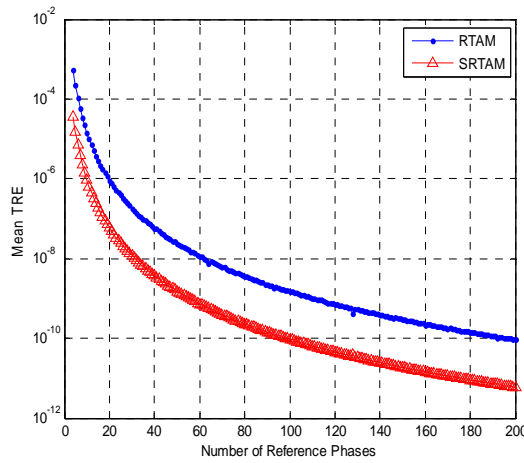


Figure 8. Mean of Total Residual error versus the number of reference phases

4. RESULTS AND DISCUSSION

4.1. Simulink implementation and Evaluation of the Wave Arithmetic Unit

In this section, we propose the Matlab-Simulink implementation and evaluation of the Wave Arithmetic Unit that computes the sine value of the input phase according to **SRTAM** approximation method. Figure 9 gives the required input and output signals while Figure 10 presents the Simulink-design architecture according to the following parameters:

- WAU: input-14 bits to output-10 bits.
- Activation on rising edge of clock signal.
- Number of reference phases: $r = 32$.
- Reference angles:

$$\theta(\text{rad}) = [0 \ 0.049 \ 0.098 \ 0.147 \ 0.196 \ 0.245 \ 0.294 \ 0.343 \ 0.392 \ 0.441 \ 0.490 \ 0.539$$

$$0.589 \ 0.638 \ 0.687 \ 0.736 \ 0.785 \ 0.834 \ 0.883 \ 0.932 \ 0.981 \ 1.030 \ 1.0791$$

$$1.129 \ 1.178 \ 1.227 \ 1.276 \ 1.325 \ 1.374 \ 1.423 \ 1.472 \ 1.521 \ 1.570]$$

- Reference quantized coefficients on 10bits format:

$$\text{InCos} = [1023 \ 1022 \ 1019 \ 1012 \ 1004 \ 993 \ 979 \ 964 \ 946$$

$$925 \ 903 \ 878 \ 851 \ 822 \ 791 \ 758 \ 724 \ 687$$

$$649 \ 609 \ 568 \ 526 \ 482 \ 437 \ 391 \ 344 \ 297$$

$$248 \ 199 \ 150 \ 100 \ 50 \ 0].$$

$InSin = [0 \quad 50 \quad 100 \quad 150 \quad 199 \quad 248 \quad 297 \quad 344 \quad 391 \quad 437 \quad 482 \quad 526$
 $568 \quad 609 \quad 649 \quad 687 \quad 724 \quad 758 \quad 791 \quad 822 \quad 851 \quad 878 \quad 903$
 $925 \quad 946 \quad 964 \quad 979 \quad 993 \quad 1004 \quad 1012 \quad 1019 \quad 1022 \quad 1023].$

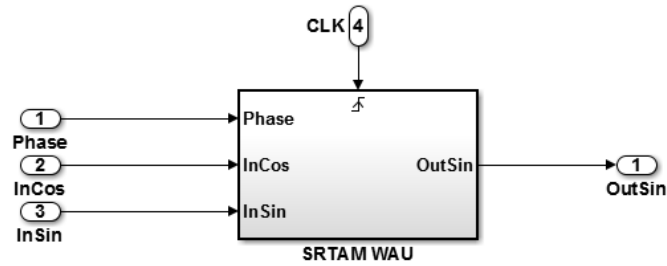


Figure 9. Inputs and outputs of SRTAM based Wave Arithmetic Unit

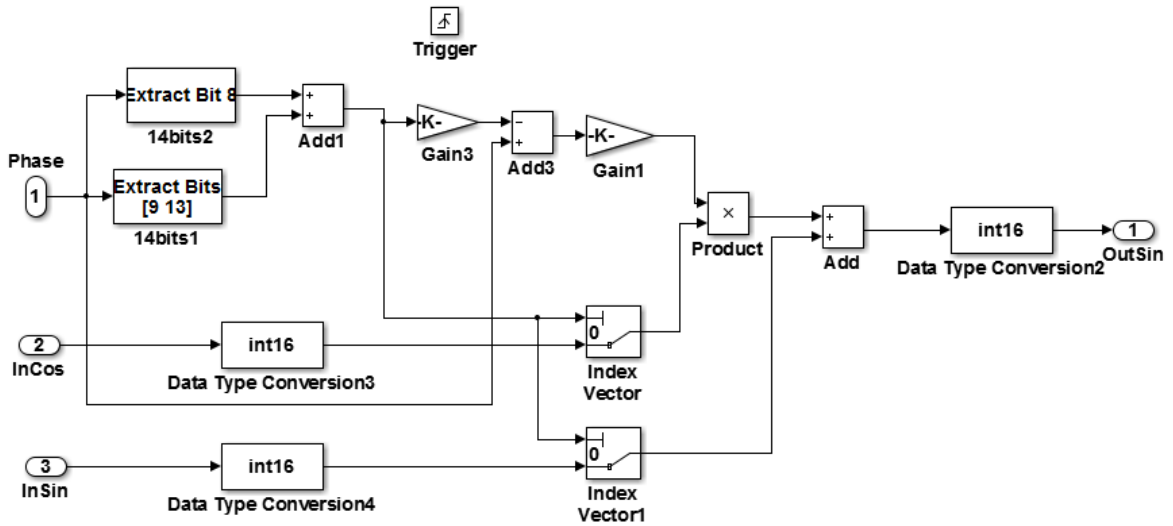


Figure 10. Simulink architecture of wave arithmetic unit 14bits to 10bits

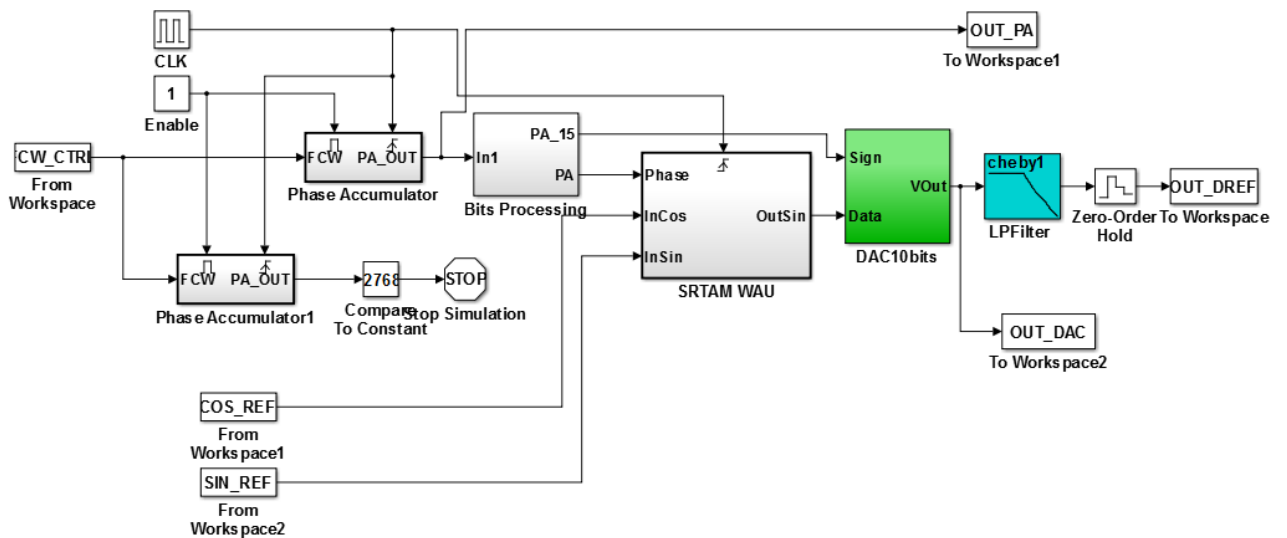


Figure 11. Simulink-model for DDS evaluation

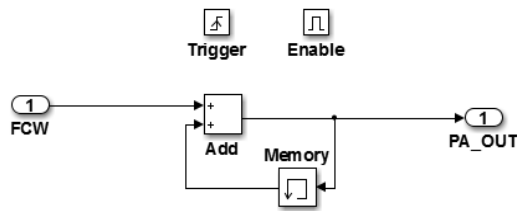


Figure 12. Simulink architecture of the phase accumulator

For the evaluation, the most used factor which evaluates the performances of direct digital synthesizer is the Spurious free dynamic range (SFDR) [8],[12]. This value represents the ratio of the power in the fundamental frequency, **S**, to power of the largest spurious signal, **R**, regardless of where it falls in the frequency spectrum. To this end, we have implemented the complete architecture of DDS based on the proposed Wave Arithmetic unit on Matlab-Simulink environment. The architecture is shown in Figure 11, using the phase accumulator of 16 bits presented in Figure 12, chebychev low pass filter : pass band frequency = 500KHz, pass band ripple= 1dB, Digital to Analog Converter: 10bits, Clock: 1MHz. Further, a computer program has been written in MATLAB to simulate the proposed architectures.

The SFDR is evaluated and plotted in Figure 13 and Figure 14 versus frequency control word for different values of the order of low-pass filter and for 16 and 32 references angles respectively. As a result, the SFDR changes from 65dB for small values to 43dB for higher values of FCW. Furthermore, there is small improvement of SFRD by an amount of 1dB for 32 reference angles. Regarding to the impact of low-pass filter, the SFDR will be unchanged from the 6th order. The obtained values of SFDR are sufficient for the production of sinusoidal waves with low harmonic contribution. In addition to previous simulation, we compare the spurious content of our method and the conventional DDFS architecture, as illustrated in Figure 15. As a consequence, the proposed method provides the same SFDR in the studied range of frequency control word and can be integrated in the synthesizer with high performance and low complexity.

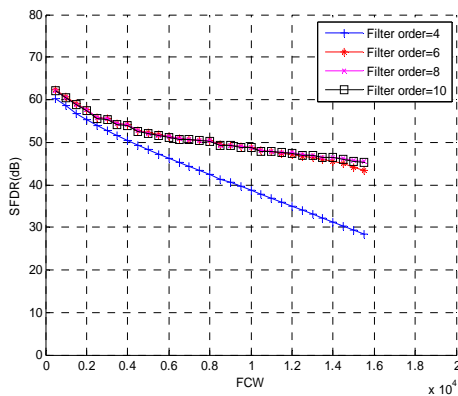


Figure 13. Spurious Free Dynamic Range versus Frequency control word for $r = 16$

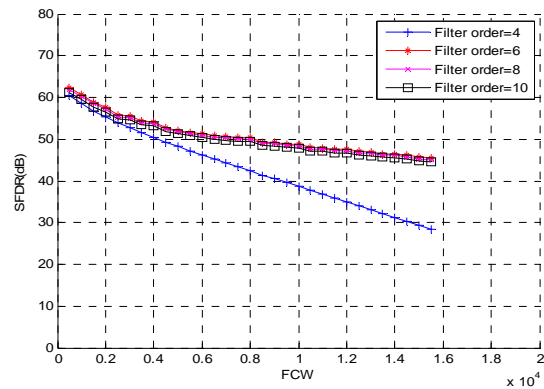


Figure 14. Spurious Free Dynamic Range versus Frequency control word for $r = 32$

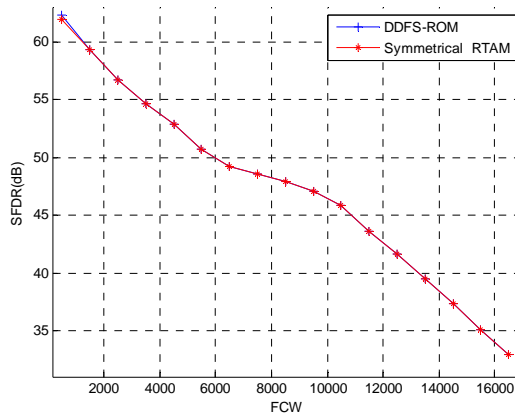


Figure 15. SFDR of DDSF-ROM and SRTAM for $r = 32$

4.2. Design and Simulink Implementation of a Sweep Frequency Synthesizer

To improve the performances of the measurement blocks of amplitude or phase of studied systems versus input frequency, we propose to design a sweep frequency synthesizer which provides two channels as shown in Figure 3: main channel for exciting system, and reference channel for measurement circuit. The Simulink implementation is given in Figure 16. The main and reference channels are noted v_m and v_r respectively. The HF to LF circuit is also implemented using the product block and low pass-filter. In Figure 17, we plot the following signals: phase accumulator, main channel, reference channel and measurement signal for $FCW = 2000$, $FCW_R = 500$ and $CLK = 1MHz$. The spectrums of different signals are shown in Figure 18. We note that the synthesized frequencies correspond to theoretical values: $F_m = FCW \times \frac{F_{CLK}}{2^{16}} = 30,517 KHz$; $F_r = FCW_R \times \frac{F_{CLK}}{2^{16}} = 38,146 KHz$; and the frequency of the measurement signal $F_{mes} = (FCW_R - FCW) \times \frac{F_{CLK}}{2^{16}} = 7,62 KHz$.

In the sweep mode, we have to change the frequency control word FCW for the same value of FCW_R to keep the measurement frequency F_{mes} constant. For this proposed circuit, we give in Figure 19, simulations outputs for the control range: $FCW = [512 \ 1536]$ and $FCW_R = 50$ corresponding to synthesized interval $[7,8125 KHz \ 23,4375 KHz]$ and measurement frequency of $762 Hz$. It is clear that the measurement signal has constant frequency during the sweep cycle whose value is controlled by reference word FCW_R . This consequence validates the main objective of our work.

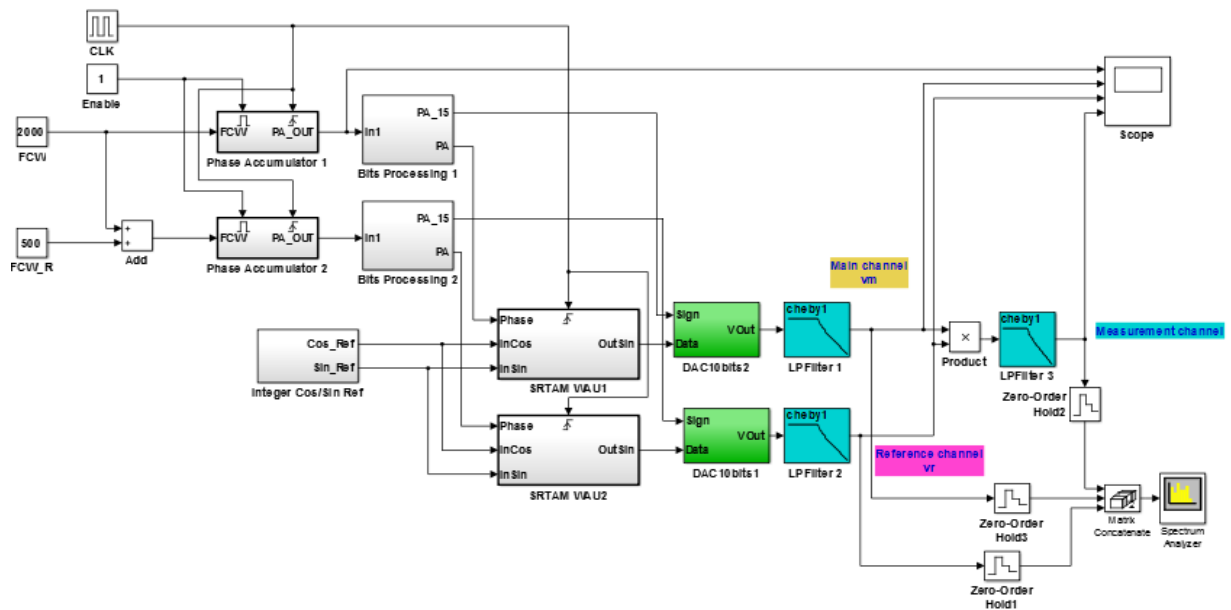


Figure 16. Simulink-architecture and evaluation of Sweep DDS

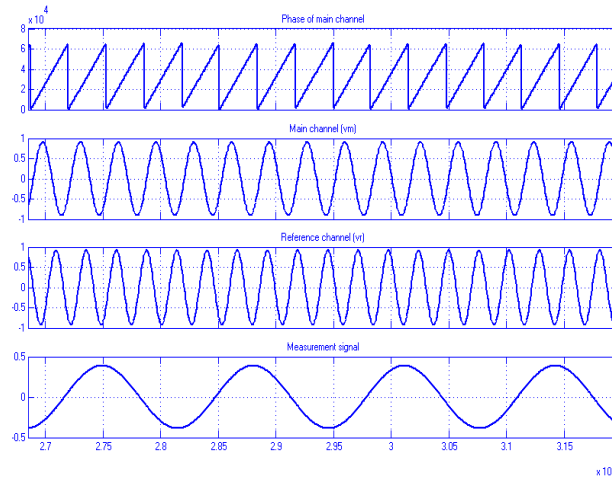


Figure 17. Phase and output channels of the proposed Sweep DDS

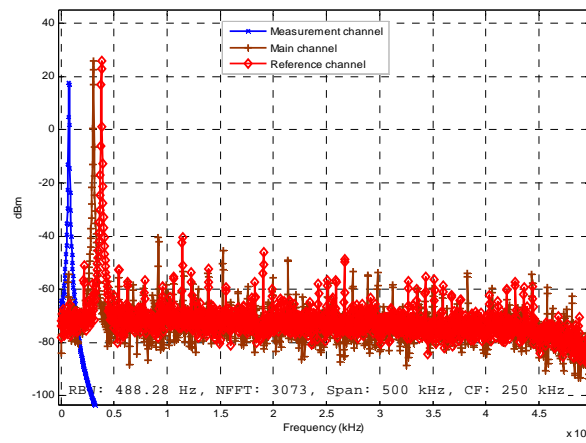


Figure 18. Spectrum of the main channel, reference channel and measurement wave

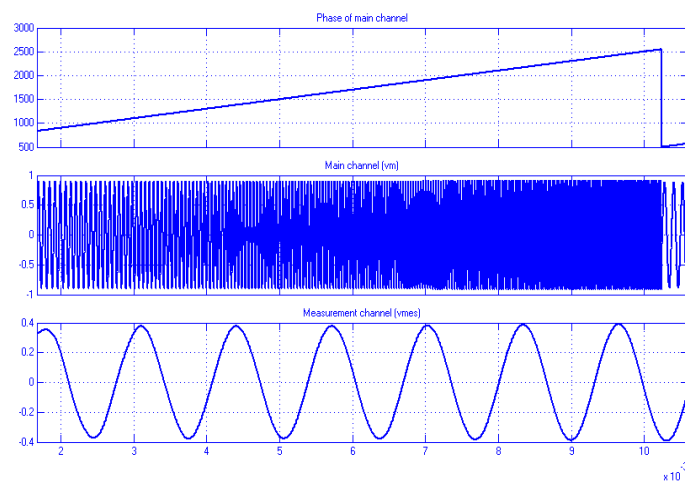


Figure 19. Outputs of Sweep DDS for: $FCW = [512, 1536]$ and $FCW_R = 50$.

5. CONCLUSION

This work has presented the architecture of a direct digital frequency synthesizer for instrumentation systems. All of the required blocks have been detailed, simulated and discussed. In this context, we have proposed a novel approximation method which exploits the reference phases and designed a Wave Arithmetic Unit. This WAU has low hardware complexity using one multiplier, one adder and a low size memory of reference coefficients. The main advantage of the proposed circuit is to provide two integrated channels: a main channel for excitation and a reference channel for measurement block. Hence, the amplitude and phase and other parameters can be measured at the same operating frequency which corresponds to the difference between reference and main frequencies. Simulations results demonstrated the effectiveness and the performances of the design architectures that can be improved according to reference phases and low-pass filters. Consequently, it is very useful to integrate the proposed circuit in ASIC or FPGA for industrial applications.

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