

Design of a Nonvolatile 8T1R SRAM Cell for Instant-On Operation

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ABSTRACT

Now-a-days, Energy consumption is the major key factor in Memories. By switching the circuit in off mode and with an lower voltages, leads to decrease in an power dissipation of the circuit. Compared to DRAM SRAM'S are mostly used because of their data retaining capability. The major advantage of using SRAM's rather than DRAM'S is that, they are providing fast power-on/off speeds. Hence SRAM's are more preferred over DRAM's for better instant-on operation. Generally SRAM's are classified in to two types namely volatile and non-volatile SRAM's. A non-volatile SRAM enables chip to achieve performance factors and also provides an restore operation which will be enabled by an restore signal to restore the data and also power-up operation is performed. This paper describes about novel NVSRAM circuit which produces better "instant-on operation" compared to previous techniques used in SRAM's. In addition to normal 6T SRAM core, we are using RRAM circuitry (Resistive RAM) to provide better instant-on operation. By comparing the performance factors with 8T2R and 9T2R, 8T1R design performs the best in the Nano meter scale. Thus this paper provides better performances in power, energy, propagation delay and area factors as compared with other designs.

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1. INTRODUCTION

Late advances in memory innovation have made conceivable new methods of operation for Nano scale IC's. On the other hand SRAM's are un-predictable, in this way non-stability capacity is required for shutdown operations [1],[2]. Generally SRAM's are preferred than DRAM's because of it's data retaining capability. SRAM performs both volatile and non-volatile operations. In our project we concentrate more on non-volatile SRAM which produces instant on operation [3] . These are designed in two technologies namely transistor technology and resistive technology. In accordingly, resistive technology uses 1R and 2R series. Compared to 2R series 1R produces more non-volatile operation effectively. Hence in this project we are using resistive technology which was often called as Resistive RAM (RRAM). For controlling or flowing of current/voltage through the resistor, we are using one additional transistor which was so called as control transistor. As we know that the transistor will act as a resistor in linear region. The RRAM circuitry which we are using in this paper was act as a "Mermistor" (memory resistor) [4].

As the years progressed, expanded thickness 64kb & quicker get to have been accounted for NVSRAM'S for military applications. The programming technology of an FPGA's are generally utilizes SRAM technology [1]. The energy consumption [5] has become a major source due to an considerably increase in an leakage current while we are reducing it's supply voltage and feature size of an SRAM. Instant

on operation means, by applying restore and power-up operation the data held in the SRAM will be cleared and that will be placed with the non-volatile data held in the storage cell. [6],[7] The demand for SRAM is increasing with large use of SRAM in system-on chip and in high performance VLSI circuits. Due to rapid increase in threshold voltage [3],[6],[8] fluctuations which were caused by the variations in ultra short-channel devices, [9] 6T SRAM and its parameters can not be worked under highly supplied voltages which causes an yield loss [10].

In this project, we are using a resistor instead of pass transistor though it provides less energy consumption because; pass transistor logic does not provide a complete '0' or '1' as an output signal. The Nano meter technologies used in this paper are of 22nm technology. They are BSIM (Berkley Short-channel IGFET Model), TSMC (Talwan Semiconductor Manufacturing Company Ltd) and PTC (Predictive Technology Model) [11]. The 45 nm technology leads to the drawbacks of stability, delay and an increase in power dissipation causes severe vt variation [6],[12] in ultra short-channel devices at an aggressively scaled technology nodes such as 22nm. The net constraints such as power, energy ,delay are calculated using this technology.

1.1. Resistive Technology

Resistive Random Access Memory (RRAM or Re RAM) is one of the type of NVRAM that works by the change of a resistance value across a dielectric material ie a solid state material which work or act as a mermistor [4]. A mermistor is an one of the form a non-volatile memory that was based on the switching of an resistor that in turns results in increasing the current flow through resistor in one direction and decreases in the another direction ie opposite direction. The materials used in this technology are of in broad range applications. They range from health care to video surveillance and other power gating techniques [13].

The physical phenomenon which has been done since 40years in the RRAM circuitry operation was resistance switching when an input voltage or current is applied, that resistance was so called as negative resistance [11]. MOM (Metal-Oxide-Metal) structures such as SiO_x , Al_2O_3 , TO_2O_5 , ZrO_2 & TiO_2 [8] are some of the materials that produce negative resistance. In a bipolar RRAM, when the applied voltage changes by increasing, an initial high resistance state gradually decreases to low resistance state. This is so called as a SET (Single Electron Transistor).

2. CONVENTIONAL DESIGN

This paper fully describes about the technology used for achieving a non-volatile SRAM for instant on operation. RRAM provides good stability and also produces a perfect output as compared to pass transistor logic. The normal 6T SRAM cell provides poor stability and high has static noise margins. On doing this operation, the stability of an SRAM cell decreases due to apply voltage divider between the driver transistors.

2.1. Previous NVSRAM's

This section reviews two NVSRAM cells using RRAM's for non-volatile storage. The 8T2R and 9T2R cells adopt different process and schemes to program the NVSRAM.

2.1.1. 8T2R NVSRAM memory cell [1]

The 8T2R NVSRAM cell is planned utilizing a complementary circuit (Figure 1) as shown below.

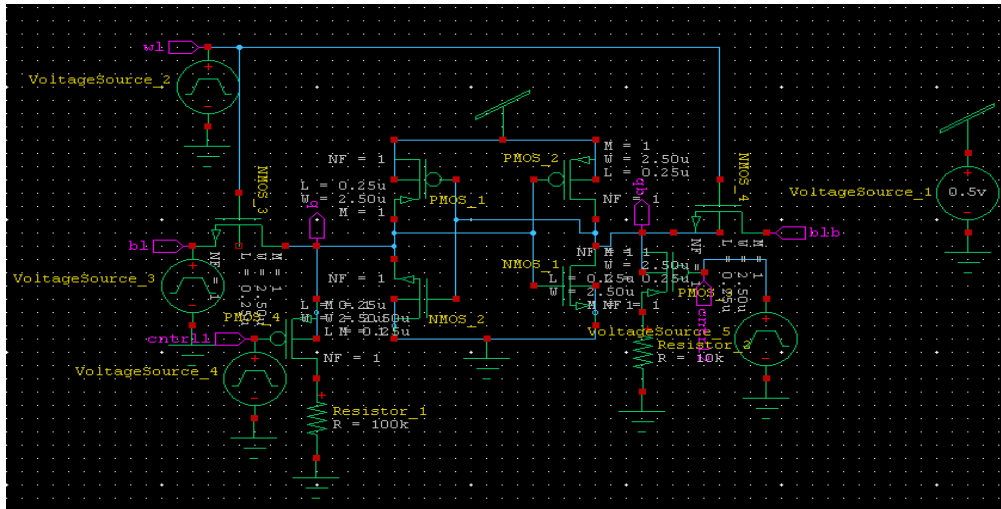


Figure 1. RRAM based 8T2R NVSRAM cell

Two RRAMs (RRAM1, RRAM2) are utilized per SRAM cell (given by the MOSFETs M1-M6). The resistive components are joined with the information hubs of the SRAM cell to store the intelligent data for the 6T cell during "Force off", in this manner withstanding to the general model of a NVSRAM, the resistive components are a piece of two RRAMs and are gotten to utilizing two control transistors. According to the data put away at the information hubs (D, DN) of the 6T center, each RRAM is modified either to a LRS or HRS [14],[15]. At the point when the force supply is turned ON, the information is composed back to the 6T SRAM center in view of the states put away in the resistive components.

2.1.2. 9T2R NVSRAM memory cell

So also, the 9T2R memory cell (Figure 2) [1] exploits two programmable RRAMs for non-unstable capacity amid the "Shut down" state as shown below.

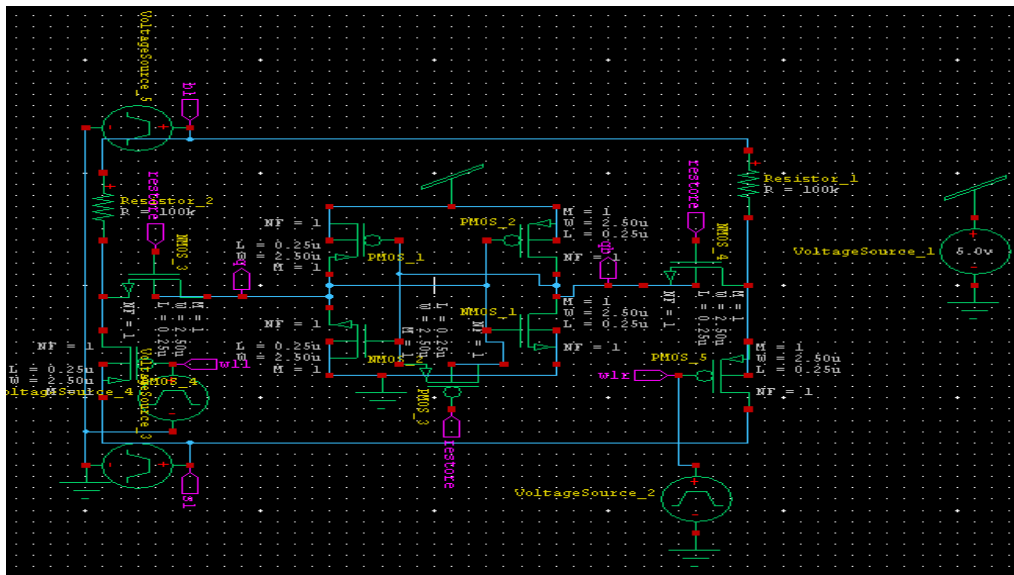


Figure 2. RRAM based 9T2R NVSRAM cell

Notwithstanding a 6T SRAM center, a leveling transistor is presented. The source and deplete of the center transistor are joined with the capacity hubs D and DN separately. The entryways of the two access transistors of the SRAM center and the evening out transistor are entwined to the Restore signal. Likewise

unique in relation to the 8T2R circuit, it uses just a solitary Piece Line (BL) and presents an extra Source Line (SL) to program the two RRAM's. The middle of the road hubs of the two 1T1R cells are associated with the first and supplement BL's of the SRAM center separately [6].

The wellsprings of two word line signals are entwined to the SL, while alternate finishes of the 1T1R cells are associated with BL. Each 1T1R cell has its own particular Word Line (signified as WLL and WLR individually); along these lines, the information are put away in the two RRAM's amid the "Shut down" state and restored back to the 6T SRAM center when the force supply is turned ON.

3. PROPOSED DESIGN

The proposed 8T1R NVSRAM outline is appeared in Figure 3. In this design we use only one 1T1R (with a resistive component denoted as RRAM1) was added to the normal 6T SRAM cell (M1-M6). The resistive RRAM1 was controlled by the transistor which was above the resistor. It is joined straightforwardly to the information node of the memory core and is utilized to store the logic data of the SRAM forced to produce its "Shut down" state. The transistor measuring methodology for outlining the 8T1R relies on upon the center of the proposed cell (for this situation, a 6T SRAM) and must consider its Read/Write operation rightness.

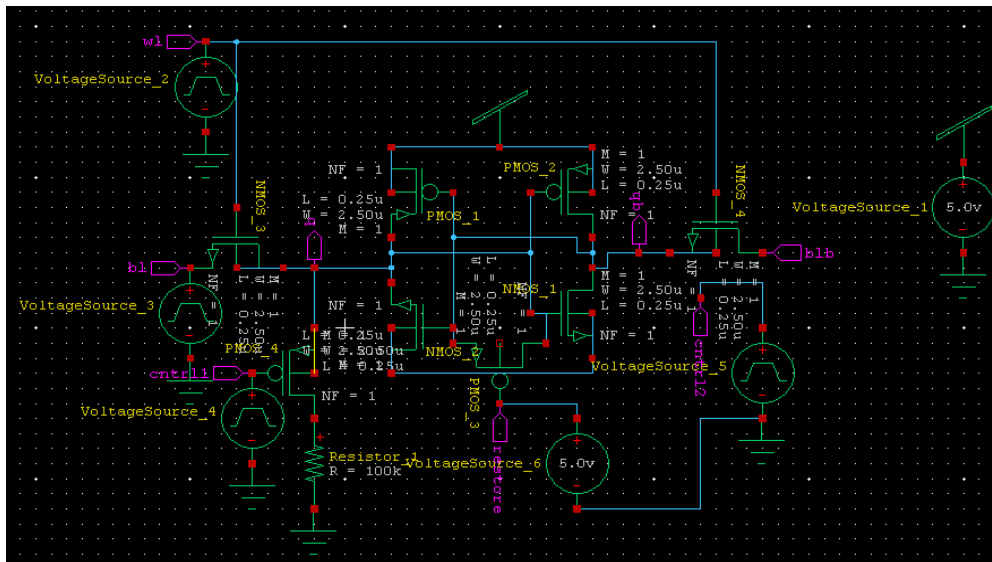


Figure 3. Proposed 8T1R NVSRAM cell

Subsequently, like the 8T2R NVSRAM cell and relying upon the particular data put away at the SRAM information hub, the RRAM component changes its resistance between the Low Resistance State (LRS) and the High Resistance State (HRS). The SET procedure changes the resistance component from HRS to LRS; the RESET procedure is utilized for the opposite operation. To accomplish non-unstable "Instant-on" operation, [3] the proposed memory cell has two essential states: "Shut down" and "Power-up". "Force up" requires to "Reset" (i.e. the RESET procedure happens in RRAM1, however influencing likewise the memory center), "Store" and "Restore".

4. SIMULATION RESULTS AND DISCUSSIONS

4.1. 8T2R NVSRAM cell

The 8T2R NVSRAM memory cell simulation results are as follows Normally SRAM performs both read and write operations. In read operation of this specific SRAM cell performs operations like when both inputs such as bit line and word line are high, the produced output i.e qb also goes to high [1].

In write operation, if wordline is set to low i.e zero, the output stores the previous SRAM value which performs instant-on operation. The inputs represented in this Figure 4, 5, 6 and they are in the order of bottom to top (bl, w1, q, qb, cntrl1, cntrl2).

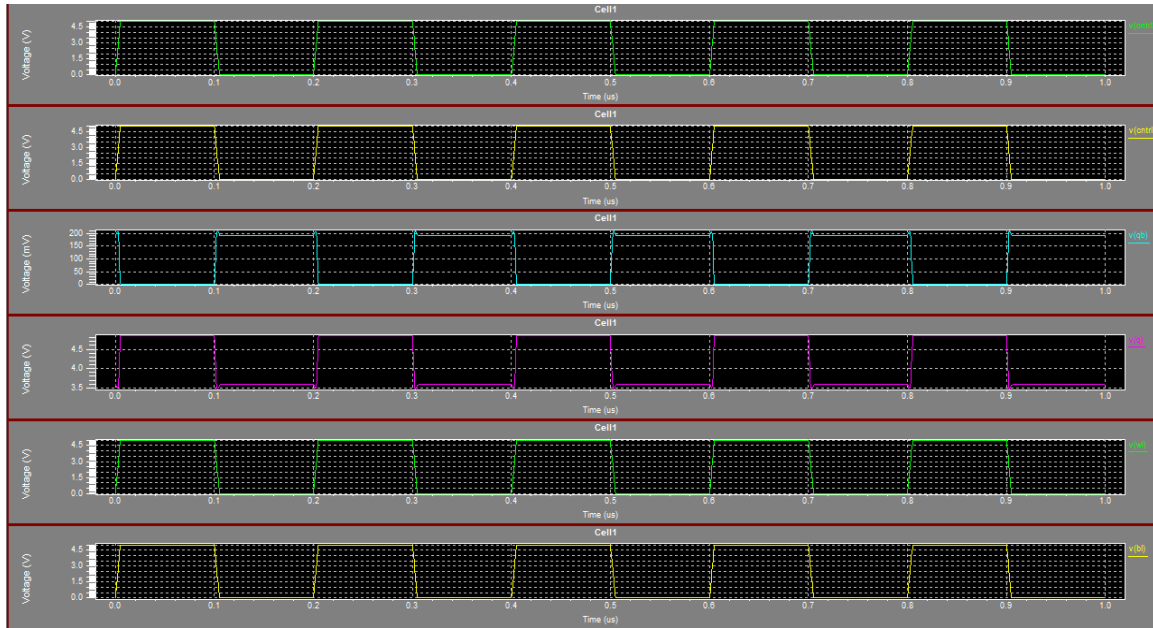


Figure 4. Simulation results of 8T2R NVSRAM cell for instant-on operation at 22nm technology

The above fig shows the simulation results of 8T2R NVSRAM cell for instant-on operation at 22nm technology. It performs both read and write operations in normal mode and in standby mode. In normal mode it performs read operation and in standby mode [7], it performs write operation. Suppose in the above figure if bitline is equal to 1 and also wordline is equal to 1 then qb is equal to 1. In other case if wordline is equal to 0, then the output qb stores the previous value which represents the instant-on operation.

4.2. 9T2RNVSRAM cell

The 9T2R NVSRAM memory cell simulation results are as Figure 5. This figure shows the simulation results of 9T2R NVSRAM cell for instant-on operation at 22nm technology. It performs both read and write operations in normal mode and in standby mode.

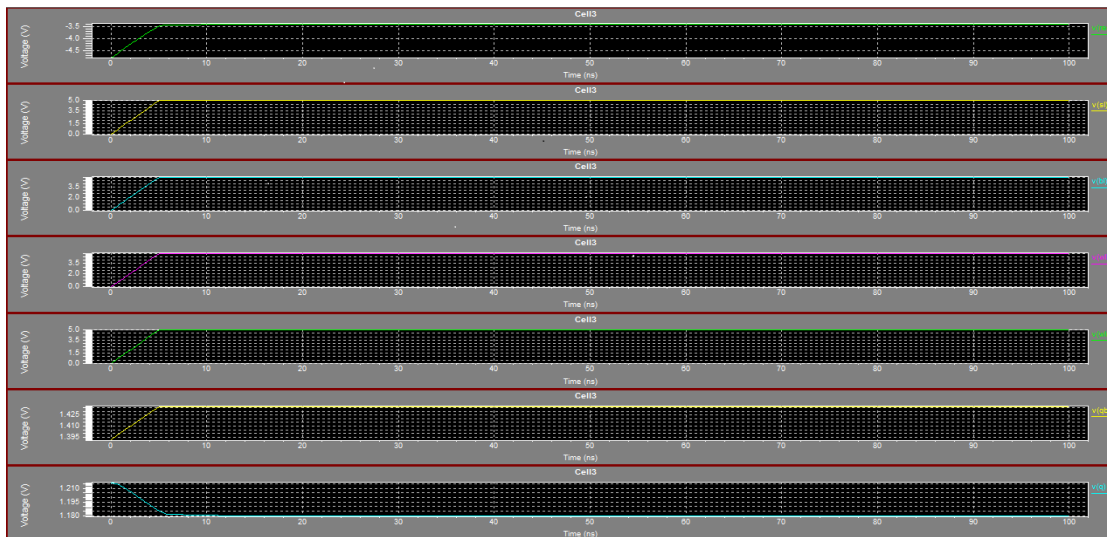


Figure 5. Simulation results of 8T2R NVSRAM cell for instant-on operation at 22nm technology

In normal mode and standby mode, it performs either low or high signal i.e 0 (or) 1. Because here we apply an restore signal. So, it will operate in standby mode. As compared to previous one it does not produces better instant-on operation like that design.

4.3. 8T1R NVSRAM cell

The 8T1R NVSRAM memory cell simulation results are as Figure 6. The figure shows the simulation results of 8T1R NVSRAM cell for instant-on operation at 22nm technology. It performs both read and write operations in normal mode and in stand by mode.

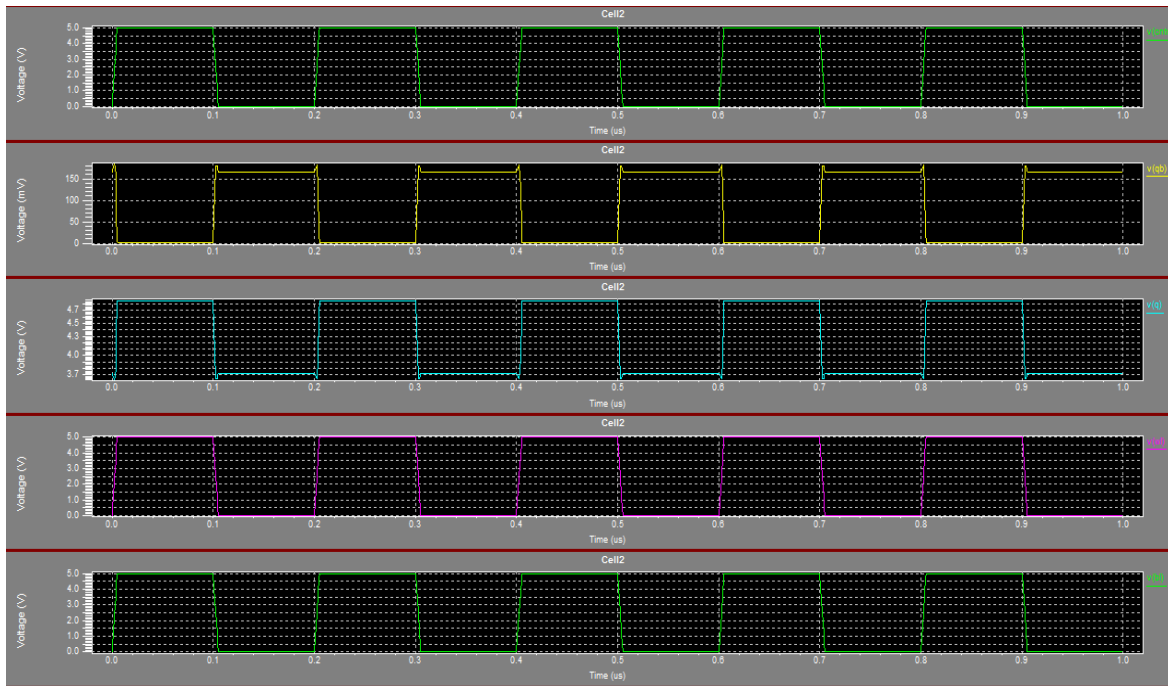


Figure 6. Simulation results of 8T1R NVSRAM cell for instant-on operation at 22nm technology

This proposed 8T1R NVSRAM provides instant-on-operation as best as compared to previous technologies. In read operation it performs the same operation as per the previous techniques and also in the write operation same technique follows. As per the figure, if wordline is equal to 1 it doesnot produces an perfect output signal as well if it will be equal to 0, it stores the previous value with out any distortions and also less delay and also minimizes some performance criteria due to the use of restore signal [6] in our design. Hence this proposed design produces less delay, low power and also occupies a less amount of area. So, we consider this as a better design for producing better instant-on operation.

Table 1. Comparison of different NVSRAM types

| NVSRAM Types | Power | Energy | Delay |
|--------------|--------|--------|-------------|
| 8T2R | 2.63 W | 5.24J | 2.4525e-010 |
| 9T2R | 9.54W | 10.2J | 5.4525e-012 |
| 8T1R | 2.53W | 7.60J | 2.5251e-010 |

5. CONCLUSION

This paper presents that a low power non-volatile SRAM (NVSRAM) cell design which can be utilized for instant-on operation i.e. by applying restore and power-up operation the data held in the SRAM will be cleared and that will be placed with the non-volatile data held in the storage memory cell. The proposed 8T1R SRAM memory cell achieves in an drastic reduction in terms of energy and power as

compared with other NVSRAM memory cells as we discussed in the introduction section. The normal 6T SRAM core requires efficient energy while the written operation is taking place and also in standby mode. But, the nature of a non-volatile SRAM (NVSRAM) saves energy dissipation in a significant manner. At last, this paper shows that the proposed NVSRAM memory cell produces an efficient variations in all the net constraints such as delay, power and energy.

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