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Efficient Low-Complexity Digital Predistortion for Power Amplifier Linearization

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ABSTRACT

In this paper, a low-complexity model is proposed for linearizing power amplifiers with memory effects using the digital predistortion (DPD) technique. In the proposed model, the linear, low-order nonlinear and high-order nonlinear memory effects are computed separately to provide flexibility in controlling the model parameters so that both high performance and low model complexity can be achieved. The performance of the proposed model is assessed based on experimental measurements of a commercial class AB power amplifier by applying a single-carrier wideband code division multiple access (WCDMA) signal. The linearity performance and the model complexity of the proposed model are compared with the memory polynomial (MP) model and the DPD with single-feedback model. The experimental results show that the proposed model outperforms the latter model by 5 dB in terms of adjacent channel leakage power ratio (ACLR) with comparable complexity. Compared to MP model, the proposed model shows improved ACLR performance by 10.8 dB with a reduction in the complexity by 17% in terms of number of floating-point operations (FLOPs) and 18% in terms of number of model coefficients.

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1. INTRODUCTION

Power amplifier (PA) is a major source of nonlinearity in a communication system since it is often driven close to the saturation region to achieve high power efficiency. The nonlinearity includes out-of-band emission which causes adjacent channel interference and in-band distortion that degrades the bit error rate performance. In modern high speed communications, transmission schemes with high spectral efficiency such as Orthogonal Frequency Division Multiplexing (OFDM) and Wideband Code Division Multiple Access (WCDMA) are more sensitive to PA nonlinearity and memory effects. This issue can be solved by backing-off the operating region of the PA into a linear mode at the expense of the degradation of the power amplifier efficiency. To overcome the conflict between the power efficiency and the linearity of the power amplifier, a linearization technique is required. One of the most cost-effective linearization techniques is the digital predistortion (DPD) [1].

Many DPD structures have been presented in the literature, containing the Volterra-based models [2]-[6], the polynomial-based models [7], the neural-network models [8],[9], and the LUT-based models [10],[11]. Even though the Volterra model is generally the most accurate structure in compensating the nonlinearity with memory effects of the power amplifier, it is mainly restricted to compensate mild

nonlinearity with memory effects of the PA. This is because of its high complexity in extracting Volterra kernels. Therefore, several special cases of Volterra model were proposed, such as the dynamic deviation reduction model [12].

However, high complexity DPD is undesirable because it leads to high power consumption and long-time delay due to intensive processing. Moreover, the main justification for the DPD technique is to gain more power-efficient PA, which is the most power consuming device in transmitters [13]-[15]. Therefore, it is essential that the power saved, by using DPD, is not spent on a high complexity DPD algorithm. Indeed, the MP model proposed in [2] is well-known for PA linearization. This model compensates for nonlinearities with memory effects using considerably lower model dimensions than the models reported in [4]. However, the linearity performance of the PA using the MP model is generally lower than the performance when using the models presented in [3],[4]. Therefore, achieving high linearity performance and simultaneously minimizing the DPD model complexity is crucial.

In this paper, a low-complexity DPD model is proposed and experimentally validated for linearizing power amplifiers with memory effects. The proposed model is constructed by separating the linear from the nonlinear memory effects to enhance linearization. The low-order nonlinear memory effect is then separated from its high-order terms to reduce the model computational complexity. Consequently, this algorithm will provide flexibility in controlling the dimensions of the model that can improve the linearity performance while reducing the computational complexity of the DPD model. Therefore, the main contribution of this paper is that the proposed model gives a better experimentally adjacent channel leakage power ratio (ACLR) performance than the MP model [2] with a considerable reduction in the model computational complexity. Moreover, the experimental results show that the proposed model outperforms the DPD model with single-feedback [3] in terms of ACLR performance with a comparable model complexity.

2. MODEL DESCRIPTION

In this section, the memory polynomial model is presented and the proposed model with its identification algorithm is clarified.

2.1. Memory Polynomial Model

The baseband predistorter can be modelled using the MP model, which is a good model as considered in [2], as shown in Equation (1):

$$z(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} c_{kq} x(n-q) |x(n-q)|^{k-1} \quad (1)$$

where $z(n)$ and $x(n)$ are the complex output and input signals of the MP predistorter model, respectively. c_{kq} , K, and Q are the model coefficients, nonlinearity order, and memory length, respectively.

In [2], the MP model, which was used as a digital predistorter, offers a good trade-off between performance and complexity. It has a good advantage since its parameters (i.e. the MP's coefficients) can easily be extracted using least square solutions with an indirect learning architecture proposed in [16] as shown in Figure 1. However, the MP model uses the same high nonlinearity order in all of the memory branches, which results in an oversized model and an increase in the computational complexity of its model.

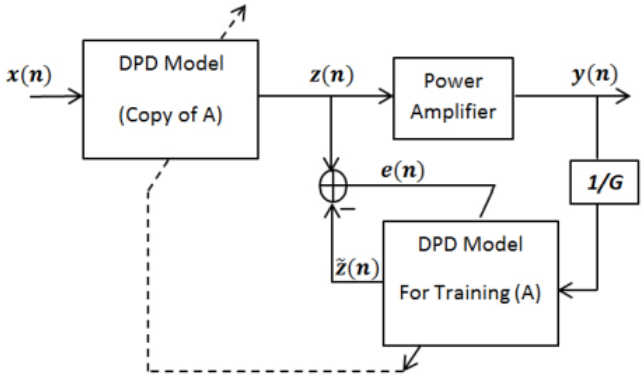

Figure 1. Indirect learning architecture

2.2. Proposed Model

To reduce the complexity of the DPD model and enhance the compensating performance of the nonlinearities with memory effects of the power amplifier, a DPD model is derived from the Volterra-series model represented in complex baseband [17] as shown in Equation (2):

$$z(n) = \sum_{k=1}^{K} \sum_{q_1=0}^{Q} \cdots \sum_{q_k=0}^{Q} h_k(q_1, \ldots, q_k) \times \prod_{j=1}^{(k+1)/2} x(n-q_j) \cdot \prod_{j=(k+1)/2+1}^{k} x^*(n-q_j) \quad (2)$$

where $z(n)$ and $x(n)$ are the complex baseband output and input signals of the Volterra-series predistorter, respectively. K is the nonlinearity order, Q is the memory depth, $h_k(q_1, \ldots, q_k)$ are the kth-order Volterra kernels, and the symbol $(\cdot)^*$ denotes the complex conjugate operator.

If the Volterra kernels are equal to zero except along the diagonal where only $q_1 = q_2 = \cdots = q_k = q$ are considered, this will reduce the model complexity without significant reduction in the linearity performance. Thus, the expression in Equation (2) is reduced to Equation (3):

$$z(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} h_k(q, q, \ldots, q)\, x(n-q)\, |x(n-q)|^{k-1} \quad (3)$$

By combining the terms of the linear memory effects (i.e. when k = 1) and separating them from the other terms, which represent the dynamic nonlinearity effects. Consequently, the linear memory effects can be efficiently compensated as shown in Equation (4):

$$z(n) = \sum_{q=0}^{Q} \left[h_1(q)\, x(n-q) + \sum_{k=2}^{K} h_k(q, \ldots, q_{k-1})\, x(n-q)\, |x(n-q)|^{k-1} \right] \quad (4)$$

Then, for properly controlling the compensation of the nonlinearity with memory effects and reducing at the same time the computational complexity of the proposed model, the effects of the dynamic low-order are split from the high-order nonlinearity effects by sorting out the nonlinearity terms of $k = 2$ from the higher nonlinearity order as illustrated in Equation (5):

$$z(n) = \sum_{q=0}^{Q} \left[h_1(q)\, x(n-q) + h_2(q, q)\, x(n-q)|x(n-q)| + \sum_{k=3}^{K} h_k(q, \ldots, q_{k-2})\, x(n-q)\, |x(n-q)|^{k-1} \right] \quad (5)$$

By changing the model coefficients $h_1(q)$, $h_2(q, q)$, and $h_k(q, \ldots, q_{k-2})$ to a_{1m}, a_{2l}, and a_{kq} respectively, the proposed method can be expressed as in Equation (6):

$$z(n) = \sum_{m=0}^{M} a_{1m}\, x(n-m) + \sum_{l=0}^{L} a_{2l}\, x(n-l)|x(n-l)| + \sum_{k=3}^{K} \sum_{q=0}^{Q} a_{kq}\, x(n-q)|x(n-q)|^{k-1} \quad (6)$$

where a_{1m} and a_{2l} are the complex coefficients of the first and second branches of the proposed model, respectively, and the a_{kq} values include the complex model coefficients of the third branch. M, L, and Q represent the memory depth for the first, second, and third branches, respectively, and K denotes the nonlinearity order for the third branch. It is worth noting that the third term starts with nonlinearity order $k = 3$ to avoid redundancy with the first and second terms.

As modern wireless systems utilize wider bandwidths with higher speed, the design for an accurately DPD model must take into account the linear memory effects and the dynamic nonlinearities. Thus, the proposed predistorter shown in Figure 2 has an important property, which is separating the purely linear memory effects (represented in the first branch) from the low-order nonlinearity dynamic one (considered in the second branch) and finally adds these branches to the high-order nonlinearity memory effects branch. Consequently, the proposed model provides an efficient way to present an effective distortion compensation approach for power amplifier linearization. Moreover, the proposed model also allows for more flexibility in modelling the memory effects in which the model dimensions of each branch are controlled separately, which reduces the model complexity while enhancing the linearity performance of PAs.

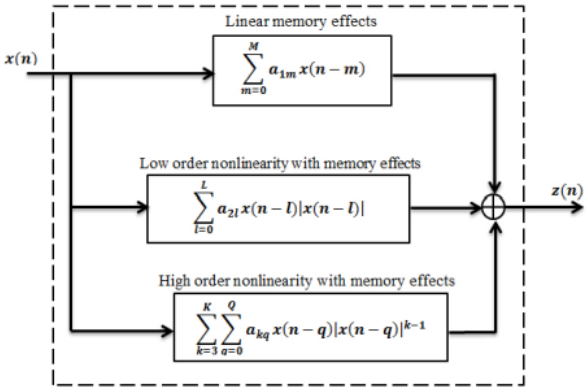

Figure 2. Basic architecture of the proposed model

2.3. Model Identification Procedure

The proposed predistorter has the property of linearity in model parameters as shown in Equation (6), which means that the model output is linear with its coefficients, since it was derived from Volterra-series model. Hence, the coefficients of the proposed model can be extracted in a direct way using the least squares (LS) technique. The identification of the proposed model is an offline procedure and all of the branches of Equation (6) are identified simultaneously as shown in Equation (7):

$$z = U w \tag{7}$$

where the z vector is the output of the three dynamic branches based on Equation (6), the U matrix includes the basis functions of the three polynomial branches, and the w vector contains the coefficients of the proposed model. The vectors z and w are defined in Equations (8) and (9) respectively, where N is the input samples length used for the identification:

$$z = [z(0), z(1), \dots, z(N-1)]^T \tag{8}$$

$$w = [a_{10}, a_{11}, \dots, a_{1M}, a_{20}, a_{21}, \dots, a_{2L}, a_{30}, \dots, a_{KQ}]^T \tag{9}$$

The matrix U is analysed into sub-matrices as shown in Equation (10):

$$U = [U_{p1} \; U_{p2} \; U_{p3}] \tag{10}$$

where the sub-matrices, U_{p1}, U_{p2}, and U_{p3}, are composed from the basis functions of the linear memory effects, low-order nonlinearity with dynamic effects, and dynamic high-order nonlinearity branches, respectively. The indirect learning architecture is used for extracting the coefficients of the proposed model as shown in Figure 1. Accordingly, a new sequence is defined in Equation (11):

$$g(n) = \frac{y(n)}{G} \tag{11}$$

where $g(n)$ is the complex baseband input signal of the predistorter during identification process, $y(n)$ is the complex baseband output signal of the PA, and G is the gain of the linearized PA. The vector u can be expressed in Equation (12):

$$u = [g(0), g(1), \dots, g(N-1)]^T \tag{12}$$

The sub-matrices U_{p1}, U_{p2}, and U_{p3} are expressed in Equations (13), (14), and (15) respectively:

$$U_{p1} = [u(n), u(n-1), \dots, u(n-M)] \tag{13}$$

$$U_{p2} = [u(n)|u(n)|, \dots, u(n-L)|u(n-L)|] \tag{14}$$

$$U_{pg} = [u(n), u(n)|u(n)|, \dots, u(n)|u(n)|^{k-1}, \dots, u(n-Q), \dots, u(n-Q)|u(n-Q)|^{k-1}] \quad (15)$$

Finally, the coefficients of the proposed model in Equation (6) can be determined using least-squares solution for Equation (7) as shown in Equation (16), where $(.)^H$ represents complex conjugate transpose:

$$w = (U^H U)^{-1} U^H z \quad (16)$$

3. EXPERIMENTAL SETUP

To demonstrate the linearization ability of the proposed predistorter, measurements was performed using the experimental setup shown in Figure 3. It consists of a personal computer (PC), Agilent - EXG vector signal generator N5172B, Agilent – PXA signal analyzer N9030A, ATM attenuator – PNR AV084-30, and PA under test. The PC contains three software, which are Agilent SystemVue 2015.01, Matlab 2014a, and Agilent 89600 VSA software. The complex input baseband signal was generated in Matlab. Then, by using SystemVue simulator, this signal was downloaded, through Local Area Network (LAN), into the EXG in order to excite the PA under test by the RF input signal. Then, the RF output from the power amplifier was attenuated by 10 dB and received by the PXA. This PXA was utilized to down-convert and demodulate the RF output signal to baseband signal cooperating with the VSA 89600 software. Then, the baseband input and output waveforms were used to extract the coefficients of the predistortion functions in Matlab. After that, synthesizing the predistorted signal and downloading this signal into the EXG were carried out using SystemVue software.

The PA under test used was the HMC-C074 single stage class AB power amplifier, from Hittite Microwave Corporation, which provides 13 dB gain and 29.5 dBm output power at 1 dB gain compression and can operate from 10 MHz to 6 GHz. The PA was operated at 2.14 GHz with an input peak power back-off of 1 dB and tested under 5-MHz bandwidth of a single-carrier WCDMA signal with peak-to-average power ratio (PAPR) of 8.7 dB and the signal was sampled at 25 MHz.

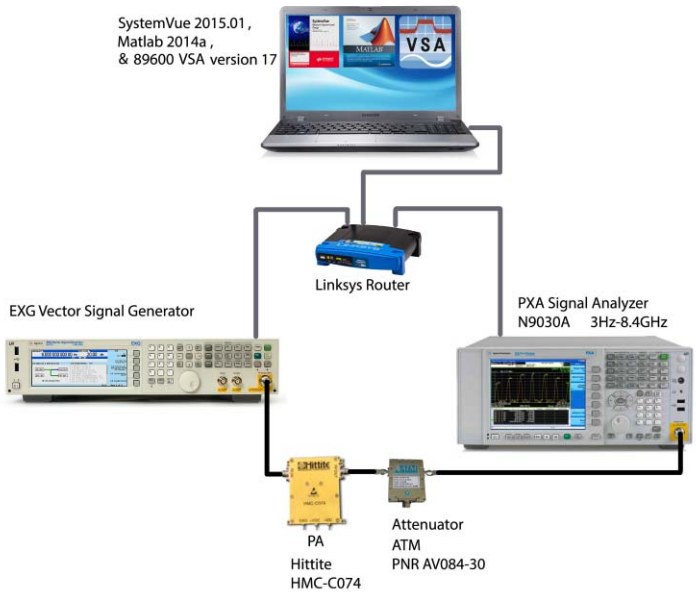

Figure 3. Measurement setup used for the proposed DPD validation

The complex input and output baseband waveforms, from the real PA, containing 20000 samples were utilized to extract the coefficients of the MP model according to Equation (1) and the proposed model based on Equation (6) using the training path shown in Figure 1. The dimensions of the models were appropriately selected to make a suitable trade-off between complexity and accuracy. The computational complexity will be discussed in section 5 and the model accuracy of the proposed and MP models were evaluated using the normalized mean squared error (NMSE) criterion, which is described in Equation (17):

$$NMSE_{dB} = 10\ log_{10}\left[\frac{\sum_{n=1}^{N}|y(n)-y_{meas}(n)|^2}{\sum_{n=1}^{N}|y(n)|^2}\right] \quad (17)$$

where $y(n)$ is the desired output waveform, $y_{meas}(n)$ is the measured output waveform, and N is the number of samples utilized in these output waveforms.

The calculated *NMSE* and model dimensions of the proposed and MP models are listed in Table 1 as well as the *NMSE* and model dimensions of the model proposed in [3]. From Table 1, it can be observed that the proposed model has higher accuracy than the accuracy of the MP model by 2.1 dB and slightly comparable accuracy with respect to the proposed model in [3].

Table 1. Comparison of model dimensions and NMSE of different DPD models

DPD model	Model dimensions	NMSE (dB)
MP [2]	$(K,Q) = (7,3)$	-34.7
DPD model [3]	$(K_{odd\ order},Q) = (11,3)$	-37.1
Proposed model	$(M)(L)(K,Q) = (3)(3)(7,2)$	-36.8

4. MEASUREMENT RESULTS

In order to assess the effectiveness of the proposed predistorter, the PA was linearized using the well-known MP model based on Equation (1) with Q =3 and K =7, and the proposed model based on Equation (6) with M = 3, L = 3, K = 7, and Q = 2. The measured output spectra of the power amplifier before and after applying the proposed and MP DPDs are shown in Figure 4 and listed in Table 2 with the measured results of the DPD model illustrated in [3]. Before applying DPD, the ACLR of the PA output was -40.5 dBc while after applying MP model, the compensation of dynamic nonlinearity was -51.3 dBc. Moreover, the model presented in [3] and listed in Table 2 has more reduction in ACLR than the MP model where -57 dBc was obtained. However, further ACLR improvement can be achieved when using the proposed model and the ACLR performance was -62.1 dBc. Therefore, the experimental results illustrate a better linearization performance using the proposed model than the performance achieved by the MP model and the model proposed in [3] by 10.8 dB and 5 dB, respectively. This achievement was obtained because of addressing the linear memory effects and separately compensating the effects of the low-order and the high-order nonlinear memory effects in the proposed model.

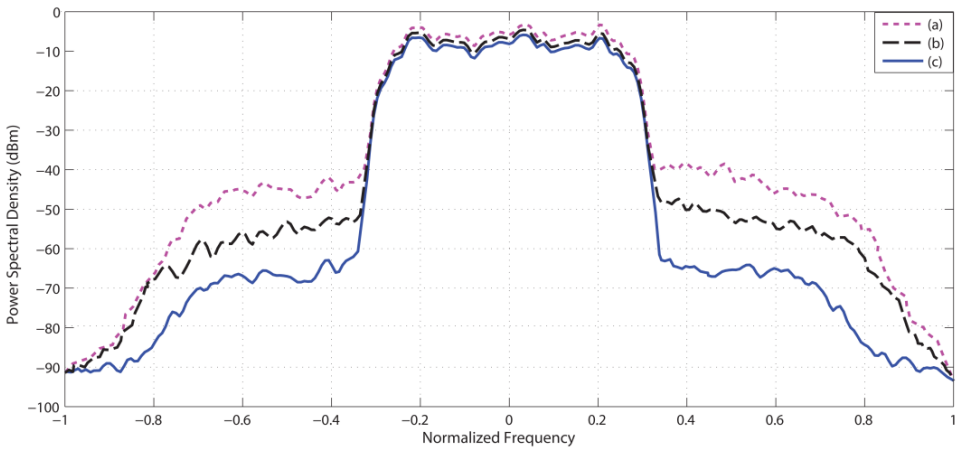

Figure 4. Measured spectra of the PA with 5-MHz WCDMA signal excitation. (a) Without DPD (b) With MP model (K= 7 and Q=3). (c) With proposed model (M=3, L=3, K= 7, and Q=2)

Table 2. Comparison of ACLR performance of the PA

DPD model	ACLR (dBc)	
	-5 MHz	+5 MHz
Without DPD	-40.5	-41
MP model [2]	-51.3	-50.5
DPD model [3]	-57	-56
Proposed model	-62.1	-61

To further demonstrate the effectiveness of the proposed predistorter, dynamic AM/AM and AM/PM characteristics of the power amplifier, driven by a single-carrier WCDMA signal with 5-MHz bandwidth, before and after applying the proposed and MP predistorters are shown in Figure 5 and Figure 6, respectively. From these figures, the dispersions and bending of the PA characteristics are shown before applying the proposed and MP models due to the electrical memory effects and nonlinearities, respectively. Figure 5 shows that the dispersions with bending of the actual PA characteristics are better compensated after applying the proposed model than the MP model. While, Figure 6, illustrates that the linearization capability on the dynamic AM/PM characteristics of the real PA of both the MP and proposed predistorters is mainly the same.

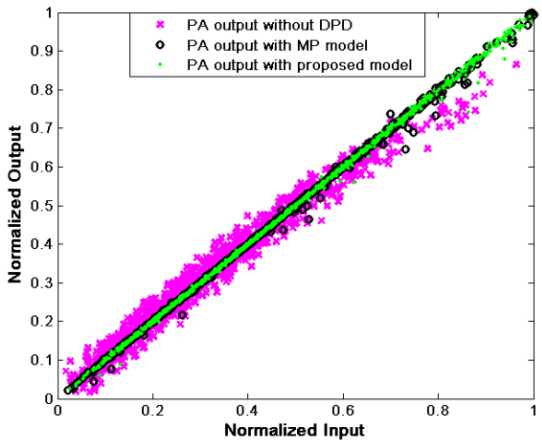

Figure 5. Dynamic AM/AM characteristics of the real PA driven by 5-MHz WCDMA signal

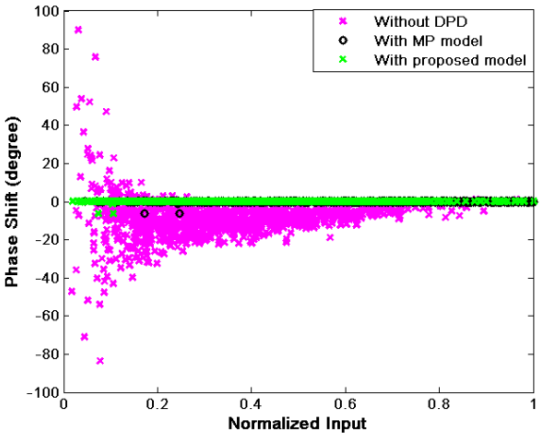

Figure 6. Dynamic AM/PM characteristics of the real PA driven by 5-MHz WCDMA signal

5. COMPUTATIONAL COMPLEXITY ANALYSIS

To evaluate the proposed predistorter in terms of computational complexity reduction, the model complexity of the proposed algorithm is determined and compared with the computational complexity of both the MP model [2] and the DPD model presented in [3]. In [18], it has been demonstrated that considering even order nonlinearities give a better model performance than using only odd order terms. Therefore, both even and odd orders of nonlinearities in the proposed model are considered in this comparison.

The complexity of the DPD models is evaluated based on the number of floating-point operations (FLOPs) and the number of model coefficients, as in [14],[19]. FLOPs are an actual measure for model complexity that gives the number of subtractions, additions, and multiplications used when the output of the DPD model is calculated. As explained in [19], the number of FLOPs required in each DPD model includes

FLOPs during the construction of the basis functions and FLOPs when these basis functions are filtered by the model coefficients.

The number of FLOPs and model coefficients of the MP, DPD model presented in [3], and proposed model are reported in Table 3. The MP model has equal nonlinearity order in all of the memory branches and MP dimensions were set to 7 and 3 for K and Q, respectively. Consequently, this results in 244 FLOPs and 28 coefficients according to Equation (1). Conversely, the use of three dynamic branches in the proposed predistorter makes it possible to reduce the memory depth of the third branch to be applied with flexibility in the other two branches as shown in Figure 2. Accordingly, the dimensions of the proposed predistorter were set to 3, 3, 7, and 2 for M, L, K started from 3, and Q, respectively. Thus, the FLOPs and number of coefficients are reduced to 204 and 23, respectively, based on Equation (6). Therefore, as shown in Table 3, it can be concluded that the proposed model has computational complexity reduction of approximately 17% in terms of FLOPs and 18% in terms of model dimensions with respect to the MP model. These complexity reduction results were achieved because the MP model is an oversized model since it uses the same high nonlinearity order in all of the memory branches. In the DPD model with single-feedback, 11th odd-order nonlinearity and memory depth of three were employed, as reported in [3]. Hence, the number of FLOPs and coefficients are slightly increased to 210 and 24, respectively, as compared with the proposed model.

Table 3. Comparison of DPD models' computational complexity and number of coefficients

DPD model	Number of model coefficients	No. of FLOPs
MP [2]	$K\,(Q+1) = 28$	$10 + 2(K-1) + 8K(Q+1) - 2 = 244$
DPD model [3]	$K_{odd\ order}\,(Q+1) = 24$	$10 + 2(K-1) + 8K(Q+1) - 2 = 210$
Proposed model	$(M+1)+(L+1)+(K-2)(Q+1) = 23$	$10 + 2(K-1) + 8[\,(M+1) + (L+1)+ (K-2)(Q+1)] -2 = 204$

In summary, the proposed model outperforms both the DPD model presented in [3] in terms of ACLR performance by 5 dB with a comparable computational complexity and MP model in terms of linearity performance by 10.8 dB with a complexity reduction of almost 17% in the FLOPs as well as a reduction of 18% in the number of model coefficients. These results demonstrates that a high linearity performance was achieved while the computational complexity of the proposed DPD model was minimized. Consequently, these improvements will lead to reduction in transmitter power consumption and also reduction in hardware resources required for DPD implementation.

6. CONCLUSION

In this paper, a DPD model with low-complexity was proposed for linearization of PAs. The proposed model consists of three parallel dynamic branches using a linear memory effects, a low-order nonlinearity memory effects, and a high-order nonlinearity memory effects functions. The linearity performance of the proposed model was validated using a class AB power amplifier driven by a single-carrier WCDMA signal and compared to the MP model as well as the DPD with single-feedback model. The experimental results clearly illustrated that the proposed model had a better performance than the previous models in reducing the ACLR by 10.8 dB and 5dB, respectively. Moreover, the computational complexity of the proposed model was reduced by 17% and 18% in terms of FLOPs and number of model coefficients, respectively, as compared to the complexity of the MP model. The enhanced performance and complexity reduction of the proposed predistorter are expected to improve the PA efficiency and reduce the overall power consumption in transmitters, respectively.

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