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A new multiplier less memcapacitor emulator with non-linear applications

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ABSTRACT

This study describes a memcapacitor emulator without a multiplier that make use of second-generation current conveyor (CCII), operational trans-conductance amplifier (OTA) and the fewest possible passive components. The proposed memcapacitor is proved mathematically and verified using several simulation approaches, such as process corner, non-volatile and hysteresis analysis. Also, provided the layout of CCII and OTA as well. The standard CMOS 90 nm technology is used in the Cadence Virtuoso tool to simulate the proposed memcapacitor emulator. This article also includes the use of memcapacitor emulator in the applications of R-C frequency selective network as well as adaptable neuromorphic structure. To investigate the experimental outcomes, an experimental setup was constructed with commercially available integrated circuits (ICs) CCII's AD844AN and OTA's CA3080EZ.

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1. INTRODUCTION

The memristor has been identified as the fourth missing component in literature since the introduction of the memristor by Professor Chua in his landmark essay [1] in 1971. His major work on the element with the memory feature has been acknowledged by the scientific community. Afterwards, the concept of the memristor is broadened to encompass two additional memory elements, the memcapacitor and meminductor [2]–[4]. These elements have the same ability to store energy as capacitance and inductance, respectively, allowing for effective data storage and computing without requirement for an external power supply. It was proposed in article [2] that the pinched hysteresis loop (PHL) for a memristor may be achieved in the voltage (v) – current (i) plane; likewise, the PHL for a memcapacitor and meminductor can be obtained in the charge (q) – voltage (v) and flux (φ) – current (i) planes, respectively. These days, a lot of attention is being paid to mem-elements (memristor, memcapacitor and meminductor) technology because of its prospective uses, which include high-density with fast non-volatile memory array [5], neuromorphic circuits [6], adaptive filters [7], chaotic circuits [8], analog [9] and digital [10] circuit designs. An extensive literature study offers a scientific framework for the development and application of these modern memory elements. The generalized SPICE model pertaining to mem-element can be found in article [11]. Additionally, the physical memristor device presented in 2008 by Williams and associates from the HP

laboratory [12] was made of titanium dioxide (TiO_2), although it is costly and has a challenging nanoscale design. In order to overcome this design complexity, researchers are using a range of techniques; as a result, their main objective is creating complementary metal-oxide-semiconductor (CMOS) based analog circuits that faithfully replicate real physical memory elements. The literature has provided excellent descriptions of the circuits constructed for memristors in recent years, but memcapacitors and meminductors have not been designed in large quantities. So, in this article proposes a memcapacitor emulator circuit, a kind of memory element that represents the relationship between the flux $\varphi(t)$ and the time integral of the charge $\sigma(t)$.

To comprehend the memcapacitor circuits found in literature, memcapacitor circuits are often categorized into two groups: electrically non-tunable [13]–[17] and tunable [18]–[24] in order to facilitate understanding of the circuits. Furthermore, in analyzing non tunable memcapacitor, the circuit [13] provide the behavior modelling of memcapacitor circuits. Moreover, there is memcapacitor circuit [14] designed using only the off the shelf components. In addition, the active element known as operational amplifier (Op-Amp) can be used to create memcapacitor circuit [15] combination with analog multipliers along with few passive components. Also, in the literature, there are mutator based memcapacitor circuits [16], [17] using memristor as part of the design along with active and passive elements. On the other side, the tunable memcapacitor circuit [18] is proposed by using multi-output operational transconductance amplifier (MO-OTA) in the design. Furthermore, various active elements are used for the proposed memcapacitor emulator circuits such as second-generation current conveyor (CCII) [19], dual X current conveyor differential input transconductance amplifier (DXCCDITA) [20], current conveyor transconductance amplifier (CCTA) [21] and voltage differencing current conveyor (VDCC) [22]. Also, there are mutator based tunable memcapacitor circuits [23], [24] and particularly the circuit voltage difference transconductance amplifier (VDTA) [23] and current derivative buffered amplifier (CDBA) [24] are proposed along with using memristor in the part of the design. As previously mentioned, the memcapacitor circuits under consideration [14], [15], [18], [19] use an additional analogue block called a multiplier in their design. However, emulator circuits employ analog multipliers increase the number of active elements, which intern makes the circuit as bulk and required large chip area, and wastes a significant amount of power [25]. Additionally, the mutator-based memcapacitor circuits suffered from matching problems and needed a bigger chip area [21], [22]. After analyzing the memcapacitor circuits that have been published in the literature, it can be concluded that there are many applications for these circuits, including neuromorphic computation [6], [17], [22] chaotic circuit [8], [16] frequency selective circuit [24] and field programmable analogue array (FPAA) [26].

As mentioned in study [19], the goal of this study is to create a multiplier-less memcapacitor emulator in which a single OTA element that operates linearly across a wider range takes the role of the multiplier unit. Moreover, by incorporating an OTA element into the design, memcapacitor emulator circuits can be made tunable. Further, without focusing on the mutator circuit, the proposed memcapacitor uses an active element known as a second-generation current conveyor (CCII) and operational trans-conductance amplifiers (OTA). Moreover, a brief comparison of proposed memcapacitor with existing memcapacitor model is presented in Table 1. The following gives a summary of the entire document: In section 2, a novel proposed memcapacitor circuit that make use of the CCII and OTA are briefly explained. Section 3 provides information on the impact of non-idealistic and parasitic elements. In section 4, the proposed design's circuit validation is investigated through simulation and experimental verification utilizing commercially available integrated circuit components, and an applications-focused perspective as a frequency selective circuit and an adaptive learning process. A conclusion is provided in section 5.

Table. 1 Comparison study of proposed memcapacitor circuit with other tunable memcapacitor circuits

Ref.	Type of memcapacitor	Simulation/ experimental	No. of active elements	No. of passive elements	Requirement of mutator/ multiplier	Frequency of operation (HZs)	Power supply
[18]	Floating	Simulation	1-MO-OTA, 1-OTA, 1-MUL	2-C, 2-R	Yes	10 Hz	1.25 V
[19]	Floating	Both	1-CCII, 1-OTA, 1-MUL	3-C, 1-R	Yes	2 kHz	4 V
[20]	Floating	Simulation	1- DXCCDITA	2-C, 1-R	No	1 MHz	1.25 V
[21]	Grounded	Simulation	1-CCTA, 1-MR	1-C	Yes	0.6 Hz-6.4 Hz	0.9 V
[22]	Floating	Both	2-VDCC	2-C, 2-R	No	1 kHz-10 kHz	1.2 V
[23]	Grounded	Both	1-VDTA, 1-MR	1-C	Yes	500 Hz	0.9 V
[24]	Floating	Simulation	1-CBTA, 1-MR	1-C	Yes	250 kHz	0.9 V
Proposed circuit	Floating	Both	1-CCII, 2-OTA.	3-C, 1-R	No	500 Hz-2 kHz	2.75 V

2. OVERVIEW OF THE PROPOSED MEMCAPACITOR EMULATOR

Beyond resistor, capacitor, and inductor, researchers are focusing on other electrical components in light of the discovery of memory elements. Flux (φ) and time integral of the charge (σ) are two concepts introduced by Biolek and colleagues [11] as shown in Figure 1. The characteristic equation of the memcapacitor element which links flux (φ) and time integral of charge (σ) can be represented as (1):

$$C_M^{-1} = \frac{d\varphi}{d\sigma} \tag{1}$$

It is possible to acquire the alternative form of the (1) by:

$$C_M^{-1} = \frac{\frac{d\varphi}{dt}}{\frac{d\sigma}{dt}} = \frac{v(t)}{q(t)} \tag{2}$$

The charge controlled memcapacitor element is represented as follows using (2).

$$v(t) = C_M^{-1}\left[\int_{t_0}^{t} q(\tau)\, d\tau\right].q(t) = C_M^{-1}\,[\sigma(t)].q(t) \tag{3}$$

The proposed memcapacitor model is constructed utilizing an analog active block called the CCII and OTA in order to get the equation for the charge-controlled memcapacitor element. The detailed descriptions of the memcapacitor emulator and its subcircuit properties as:

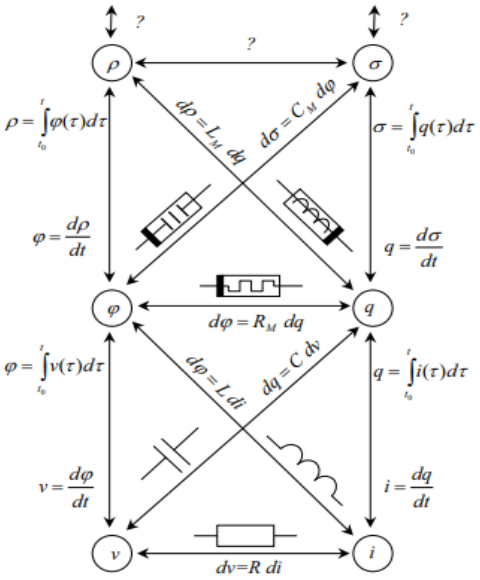


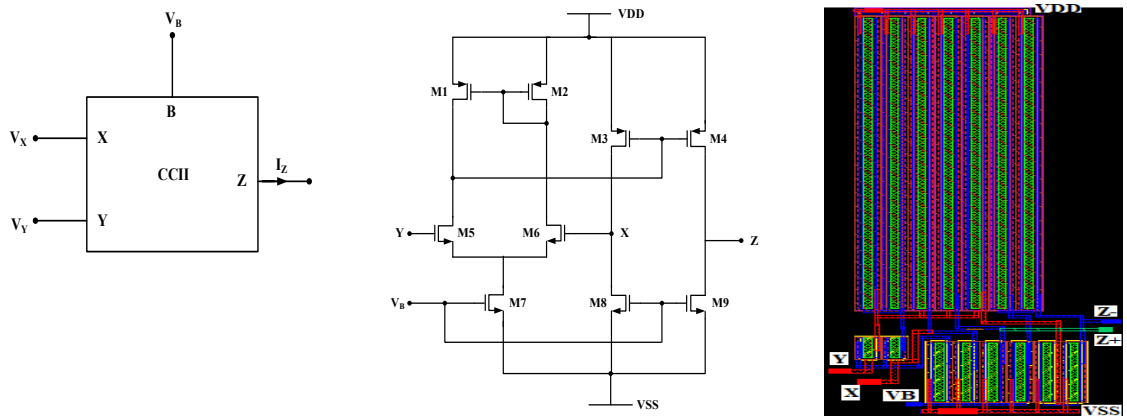
Figure 1. Memory and non-memory component's relationship [11]

2.1. CCII

An active element that can be used in both voltage mode and current mode topologies is a CCII analog building block. The symbol of circuit, realization of circuit using MOS transistor and its layout model of CCII are shown in Figure 2. The CCII features voltage-mode terminal (*Y*) which is having high input impedance, current-mode terminal (*X*) having low input impedance and a low output impedance terminal (Z) shown in the form of symbol in Figure 2(a). The characteristic properties of CCII can be defined as (4):

$$I_Y = 0,\ V_X = V_Y,\ I_Z = I_X \tag{4}$$

The implementation of CCII using MOS transistor as shown in Figure 2(b) [27]. It consists of nine transistors and their description are given in Table 2. Furthermore, the layout of the device as shown in Figure 2(c), which was produced with the Virtuoso Layout Suite tool. The area of the CCII layout is $389.58\ \mu m^2$ after the design rule checks (DRC) and layout vs schematic (LVS) inspections.



(a) (b) (c)

Figure 2. The structure of CCII: (a) symbol of a circuit, (b) MOS design [27], and (c) layout area $(30.2\ \mu m * 12.9 \mu m)$

Table. 2 Aspect ratio of transistor's in CCII

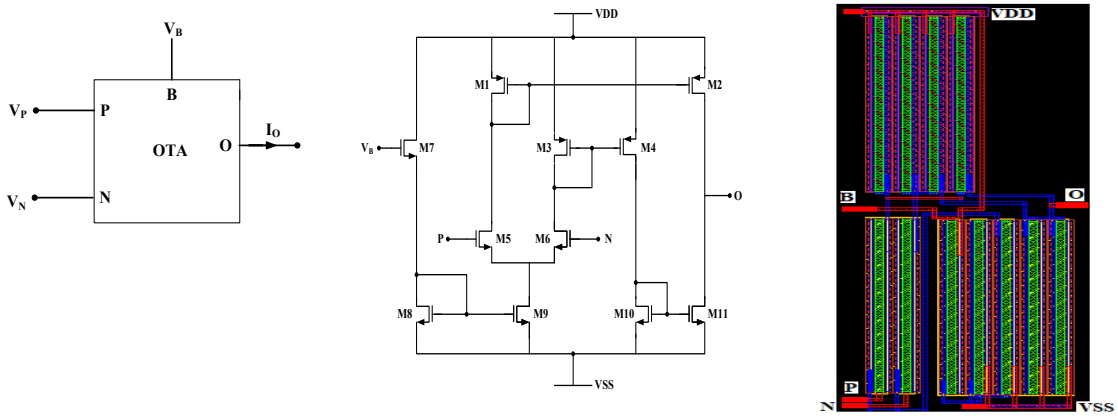
Transistors	$W(\mu m)/L(\mu m)$
M1-M4	21.6/0.36
M5-M6	1.44/0.36
M7-M9	4.32/0.36

2.2. OTA

Another active element that is utilized as a tunable is the operational transconductance amplifier (OTA). The symbol of a circuit, realization of a circuit using MOS transistor [28] and OTA layout schematic are shown in Figure 3. As shown in Figure 3(a), the output (O) port of the OTA gets a current equal to the differential input voltage $(V_P - V_N)$ and also, as a function of transconductance $(\pm gm)$. OTA properties can be defined using (5):

$$I_P = 0,\ I_N = 0,\ I_O = g_m(V_P - V_N) \tag{5}$$

The implementation of OTA using MOS transistor's as shown in Figure 3(b) [28]. It is consisting of eleven transistors and their description are listed in Table 3. In addition, the Figure 3(c) shows the device's layout, which was produced with the Virtuoso Layout Suite tool. After the successful verification of DRC and LVS, the overall area of the layout is found to be 303.43 μm^2.



(a) (b) (c)

Figure 3. The structure of OTA: (a) symbol of a circuit, (b) circuit design using MOS transistor's [28], and (c) layout area $(28.2\ \mu m * 10.76\ \mu m)$

Table. 3 Aspect ratio of transistors in OTA

Transistors	$W(\mu m)/L(\mu m)$
M1-M4	12/0.36
M5-M11	12/0.36

2.3. Proposed memcapacitor emulator

The proposed memcapacitor emulator circuit is an enhanced variant of reference [19], in which the OTA takes the role of the multiplier. With OTA, the circuit's tunability behavior was added in addition to its decreased complexity and power cost. A memcapacitor emulator as shown in Figure 4 employing one CCII, two OTA, three capacitors and one resistor to get a charge-controlled memcapacitor element. After analysis, the following equations apply to the proposed memcapacitor emulator circuit. The current on the input capacitor C_F is expressed as (6):

$$I_{in}(t) = C_F \frac{d(V_{in}(t)-V_X)}{dt} \tag{6}$$

The equation (6) is described as (7):

$$V_{in}(t) = \frac{q(t)}{C_F} + V_X \tag{7}$$

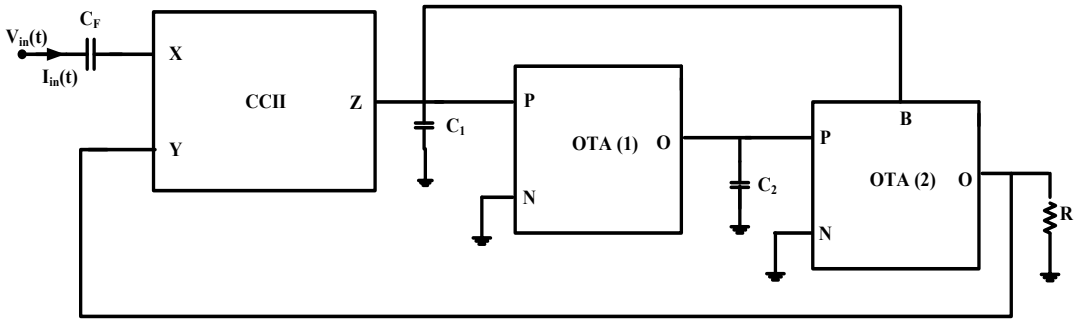


Figure 4. Proposed memcapacitor circuit

The voltage across capacitor C_1 is V_{C_1}, written using terminal relationship of CCII as (8):

$$V_{C_1} = -\frac{1}{C_1}\int_0^t I_Z\, dt = -\frac{1}{C_1}\int_0^t I_{in}(t)\, dt = -\frac{q(t)}{C_1} \tag{8}$$

Similarly, the expression of current (I_{O1}) at the output of OTA (1) is given by (9):

$$I_{O1} = g_{m1}(V_P - V_N) = g_{m1}V_{C1} = -g_{m1}\frac{q(t)}{C_1} \tag{9}$$

where g_{m1} is the transconductance gain of OTA (1). Also, the voltage across capacitor C_2 is V_{C_2}, written as (10):

$$V_{C_2} = -\frac{1}{C_2}\int_0^t I_{O1}\, dt = +\frac{g_{m1}}{C_1C_2}\int_0^t q(t)\, dt \tag{10}$$

Further, the voltage (V_Y) which is across resistor R is provided by (11):

$$V_Y = I_{O2}R = g_{m2}(V_P - V_N)R = g_{m2}V_{C2}R \tag{11}$$

where I_{o2} and g_{m2} are output current and transconductance gain of OTA (2) respectively. Here, $g_{m2} = k(V_B - V_{SS} - V_t)$, then (11) is given by:

$$V_Y = k(V_B - V_{SS} - V_t)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt = k\left(V_{C_1} - V_{SS} - V_t\right)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt$$
$$= k(-\frac{q(t)}{C_1} - V_{SS} - V_t)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t) \quad (12)$$

By considering the approximation, the (12) can be written as:

$$V_Y \approx -k\frac{q(t)}{C_1}R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt = V_X \quad (13)$$

The V_X value from the (13) is substituted in (7) and it results as (14):

$$V_{in}(t) = \frac{q(t)}{C_F} - k\frac{q(t)}{C_1}R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt$$
$$C_m^{-1} = \frac{V_{in}(t)}{q(t)} = \frac{1}{C_F} - kR\frac{g_{m1}}{C_1^2C_2}\int_0^t q(t)\,dt = \beta + \alpha\sigma(t) \quad (14)$$

The equation (14) is satisfied the equation of charge controlled memcapacitor, where α and β are specified as:

$$\alpha = -kR\frac{g_{m1}}{C_1^2C_2}, \qquad \beta = \frac{1}{C_F}$$

3. IMPACTS OF NON-IDEAL AND PARASITIC ELEMENTS

The impact of non-idealises and parasitic components on the proposed memcapacitor circuit is explained as follows:

3.1. Non-ideal analysis

When considering the non-ideal characteristics of the CCII, the correlation between voltage and current across its various ports can be restated as (15):

$$I_Y = 0,\ V_X = \alpha V_Y,\ I_Z = \beta I_X \quad (15)$$

Similarly, for an OTA is given by:

$$I_P = 0,\ I_N = 0,\ \ I_O = \gamma g_m(V_P - V_N) \quad (16)$$

where α represents non-unity voltage gain, β represents non-unity current gain and γ represents non-unity transconductance gain. After analysis, the following amended equations were produced for the suggested memcapacitor emulator circuit.

The voltage across capacitor C_1 is V_{C_1}, written using terminal relationship of CCII as (17):

$$V_{C_1} = -\frac{1}{C_1}\int_0^t I_Z\,dt = -\frac{1}{C_1}\int_0^t \beta I_{in}(t)\,dt = -\beta\frac{q(t)}{C_1} \quad (17)$$

Similarly, the expression of current (I_{O1}) at the output of OTA (1) is given by (18)

$$I_{O1} = \gamma_1 g_{m1}(V_P - V_N) = \gamma_1 g_{m1}V_{C1} = -\gamma_1 g_{m1}\frac{q(t)}{C_1} \quad (18)$$

where γ_1 is the non-unity transconductance gain of OTA (1). Also, the voltage across capacitor C_2 is V_{C_2}, written as (19):

$$V_{C_2} = -\frac{1}{C_2}\int_0^t I_{O1}\,dt = \gamma_1\frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt \quad (19)$$

Further, the voltage (V_Y) which is across resistor R is given by (20):

$$V_Y = I_{O2}R = \gamma_2 g_{m2}(V_P - V_N)R = \gamma_2 g_{m2}V_{C2}R \quad (20)$$

where γ_2 represents the non-unity transconductance gain of OTA (2). Here, $g_{m2} = k(V_B - V_{SS} - V_t)$, then the (20) is given by (21):

$$V_Y = \gamma_1\gamma_2 k(V_B - V_{SS} - V_t)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt = \gamma_1\gamma_2 k\big(V_{C_1} - V_{SS} - V_t\big)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt$$
$$= \gamma_1\gamma_2\ k(-\beta\frac{q(t)}{C_1} - V_{SS} - V_t)R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt \quad (21)$$

The equation (21) can be approximated and written as (22):

$$V_Y \approx\ -\gamma_1\gamma_2\beta k\frac{q(t)}{C_1}R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt = \frac{V_X}{\alpha} \quad (22)$$

The V_X value from the (22) is substituted in (7) and it results as (23):

$$V_{in}(t) = \frac{q(t)}{C_F} - \alpha\gamma_1\gamma_2\beta k\frac{q(t)}{C_1}R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt$$
$$C_m^{-1} = \frac{V_{in}(t)}{q(t)} = \frac{1}{C_F} - \alpha\gamma_1\gamma_2\beta kR\frac{g_{m1}}{C_1^2C_2}\int_0^t q(t)\,dt = \beta + \alpha\sigma(t) \quad (23)$$

The equation (23) is satisfied the equation of charge controlled memcapacitor, where α and β are specified as:

$$\alpha =\ -\alpha\gamma_1\gamma_2\beta kR\frac{g_{m1}}{C_1^2C_2}, \qquad \beta = \frac{1}{C_F}$$

According to (15)-(23), these non-ideal errors might not significantly affect the memcapacitor emulator's hysteresis or non-volatile properties. By operating the circuit within the appropriate frequency range, this little fluctuation can be reduced to its lowest possible amount.

3.2. Parasitic analysis

The performance of the suggested memcapacitor that is being offered is examined in this section in relation to CCII and OTA parasitic. The existence of parasitic resistors and capacitors at different port for the memcapacitor circuit are shown in Figure 5. Also, the external resistance R and parasitic resistances R_{Pi} ($i = 1,2,3$) are defined correspondingly in terms of admittances as G and G_{Pi} ($i = 1,2,3$), where $G = 1/R$ and $G_{Pi} = 1/R_{Pi}$. From the figure, the parasitic components exist in the form of resistors and capacitors which are in parallel combination at different ports as follows: at the combined ports (Z,P) and (P,B) as $C_{P1}||G_{P1}$, at combined port (O,P) as $C_{P2}||G_{P2}$, at combined ports (O,Y) as $C_{P3}||G_{P3}$ and a parasitic exists in series at port X of CCII as C_P. The practical value of parasitic capacitances (C_{Pi}) is reported within the range of fraction of picofarads and similarly, the value of parasitic admittances is calculated in the tens of micromho range. Therefore, there exists a min (C_1, C_2) >> (C_{P1}, C_{P2}, C_{P3}), min (G) >> (G_{P1}, G_{P2}, G_{P3}) and min (C_F) >> (C_P). The circuit in Figure 5 was studied again and the revised equation that follows was created to investigate the effects of different parasitic impedances on the operation of the memcapacitor circuit.

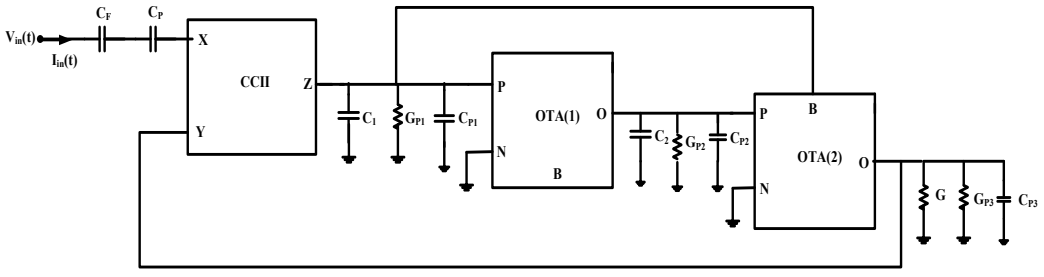


Figure 5. The parasitic components present in various ports of proposed memcapacitor emulator circuit

The current through the input capacitors C_F and C_P is expressed as (24):

$$I_{in}(t) = S(C_F + C_P)\ (V_{in}(t) - V_X) \quad (24)$$

The equation (24) is described as (25):

$$V_{in}(t) = \frac{I_{in}(t)}{C_F + C_P} + V_X \tag{25}$$

The voltage across capacitor C_1 is V_{C_1}, written using terminal relationship of CCII as (26):

$$V_{C_1} = -\frac{I_Z}{G_{P1}+SC_1} = -\frac{I_{in}(t)}{G_{P1}+SC_1} \tag{26}$$

Similarly, the expression of current (I_{O1}) at the output of OTA (1) is given by (27)

$$I_{O1} = g_{m1}(V_P - V_N) = g_{m1}V_{C1} = -g_{m1}\frac{I_{in}(t)}{G_{P1}+SC_1} \tag{27}$$

where g_{m1} is the transconductance gain of OTA (1). Also, the voltage across capacitor C_2 is V_{C_2}, written as (28):

$$V_{C_2} = -\frac{I_{O1}}{G_{P2}+SC_2} = g_{m1}\frac{I_{in}(t)}{(G_{P1}+SC_1)(G_{P2}+SC_2)} \tag{28}$$

Further, the voltage (V_Y) which is across resistor R is given by (29):

$$V_Y = I_{O2}R = g_{m2}(V_P - V_N)(G + C_{P3}) = g_{m2}V_{C2}(G + C_{P3}) \tag{29}$$

where I_{O2} and g_{m2} are output current and transconductance gain of OTA (2) respectively. Here, $g_{m2} = k(V_B - V_{SS} - V_t)$, then the (29) is given by (30):

$$\begin{aligned} V_Y &= k(V_B - V_{SS} - V_t)\, g_{m1}\frac{I_{in}(t)(G + C_{P3})}{(G_{P1}+SC_1)(G_{P2}+SC_2)} = k\big(V_{C_1} - V_{SS} - V_t\big)g_{m1}\frac{I_{in}(t)(G + C_{P3})}{(G_{P1}+SC_1)(G_{P2}+SC_2)} \\ &= k\left(-\frac{I_{in}(t)}{G_{P1}+SC_1} - V_{SS} - V_t\right)g_{m1}\frac{I_{in}(t)(G + C_{P3})}{(G_{P1}+SC_1)(G_{P2}+SC_2)} \end{aligned} \tag{30}$$

The equation (30) approximately written as (31):

$$V_Y \approx -k\left(\frac{I_{in}(t)}{G_{P1}+SC_1}\right)g_{m1}\frac{I_{in}(t)(G + C_{P3})}{(G_{P1}+SC_1)(G_{P2}+SC_2)} = V_X \tag{31}$$

The V_X value from the (31) is substituted in equation (25) and it results as (32):

$$V_{in}(t) = \frac{I_{in}(t)}{C_F + C_P} - k\left(\frac{I_{in}(t)}{G_{P1}+SC_1}\right)g_{m1}\frac{I_{in}(t)(G + C_{P3})}{(G_{P1}+SC_1)(G_{P2}+SC_2)} \tag{32}$$

Here, $(\frac{G_{P1}}{C_1}, \frac{G_{P2}}{C_2}) << \omega << (\frac{G}{C_{P3}})$ and also $C_P << C_F$, then the (32) approximated as (33):

$$\begin{aligned} V_{in}(t) &= \frac{q(t)}{C_F} - k\frac{q(t)}{C_1}R\ \frac{g_{m1}}{C_1C_2}\int_0^t q(t)\,dt \\ C_m^{-1} &= \frac{V_{in}(t)}{q(t)} = \frac{1}{C_F} - kR\frac{g_{m1}}{C_1^2C_2}\int_0^t q(t)\,dt = \beta + \alpha\sigma(t) \end{aligned} \tag{33}$$

After estimating the parasitic values for an ideal situation, the (33) is identical to (14).

4. SIMULATION AND EXPERIMENTAL RESULTS

To validate theoretical interpretations, both simulation and experimental studies are conducted. The initial step of the verification involves building CCII and OTA using MOS transistor's in 90 nm technology. The supply voltages $VDD = -VSS = 2.75$ and $V_B = -0.45\ V$ as bias voltage are employed for the design implementation and simulation. Additionally, the following values for the passive components are used: $C_F = 1.6\ \mu F, C_1 = 470\ \mu F$, $C_2 = 1\ \mu F$ and $R = 1\ k\Omega$. The calculated power consumption of the proposed memcapacitor circuit is 33.67 mW.

Initially, the simulation shown the memcapacitor's transient response to a 2 V input voltage signal at 500 Hz, as shown in Figure 6. Figure 6(a) shown with input voltage and charge waveform, and the corresponding PHL as shown in Figure 6(b). Furthermore, the circuit is also simulated by changing the frequencies from 500 Hz to 2 kHz to observe the impact of frequency fluctuation on the memcapacitor.

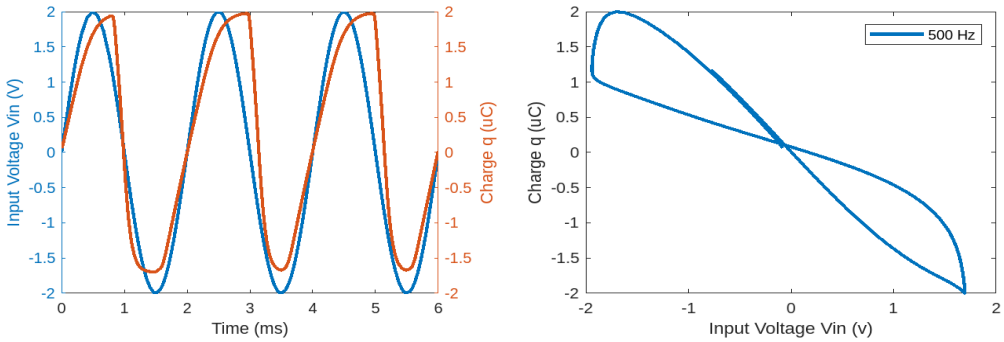


Figure 6. Transient analysis of proposed memcapacitor circuit (a) charge and voltage waveform and (b) At $f = 500\ Hz$, the pinch hysteresis curve

Further, the Figure 7 displays the PHL at several frequencies and temperature values. Figure 7(a) shown PHL at various frequencies: $500\ Hz$, $750\ Hz$, $1\ kHz$, and $2\ kHz$. According to this figure, the suggested memcapacitor operates as a linear capacitor starting at $f = 3\ kHz$ and as frequency rises, the lobe size of the PHL diminishes. In order to simulate the memcapacitor circuit at the nominal-nominal (NN) process corner, temperatures between $-40\ °C$ and $+120\ °C$ are varied, and the pinched hysteresis curve shown in Figure 7(b) for the following temperature values: $-40\ °C$, $0\ °C$, $40\ °C$, $80\ °C$ and $120\ °C$. It indicates, the memcapacitor circuit has been found to function across a wide temperature range.

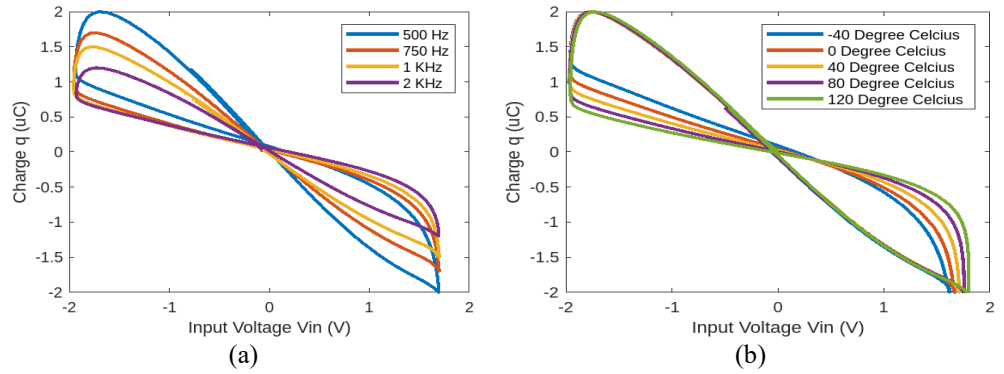


Figure 7. Graph of pinched hysteresis at different (a) frequencies and (b) temperature values

According to a similar perspective, the suggested memcapacitor model functions well at different temperatures and process corners. The analysis of process corners has a big impact on how well monolithic integration works; hence the model is carefully looked at different process corners as shown in Figure 8. As seen in Figure 8(a) through Figure 8(d), the memcapacitor circuit is emulated at many process corners including fast-fast (FF), fast-slow (FS), slow-fast (SF) and slow-slow (SS). According to the observation, flow of current in SS mode as predicted is lower than FF mode. Consequently, the suggested model performs admirably over a wide range of process corners and temperatures.

Additionally, the non-volatility test is demonstrated as shown in Figure 9. A square input voltage was provided to the circuit input terminal; the signal has the amplitude of $200\ mV$ at $1\ kHz$. Figure 9 displays the input signal and charge. When the input signal is changed from a lower to a higher value, the charge resumes where it left off. The fact that the starting and termination points of the successive pulses coincide suggests that the circuit that was built has memory capabilities. Further, the electronic tunability aspect of the memcapacitor is investigated by varying the g_m values while maintaining a constant frequency value and its associated PHL, as illustrated in Figure 10. Conversely, the proposed memcapacitor emulator may require connection in either series or parallel configurations within various electronic circuits. Consequently, the memcapacitor is linked in series, parallel, and singular arrangements, and the resulting PHL is examined. As anticipated, memcapacitors arranged in parallel yield a higher quantity of capacitor charge values compared to those connected individually and in series, as demonstrated in Figure 11.

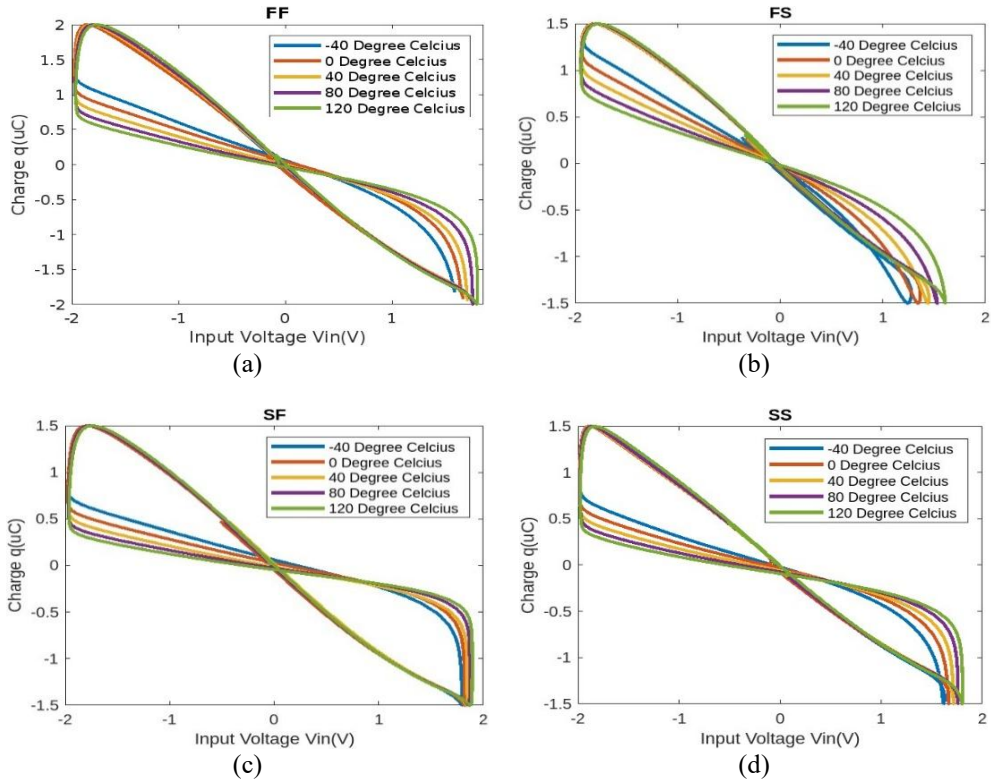


Figure 8. Variation in process corner: (a) fast-fast (FF), (b) fast-slow (FS), (c) slow-fast (SF) and (d) slow-slow (SS) process corners

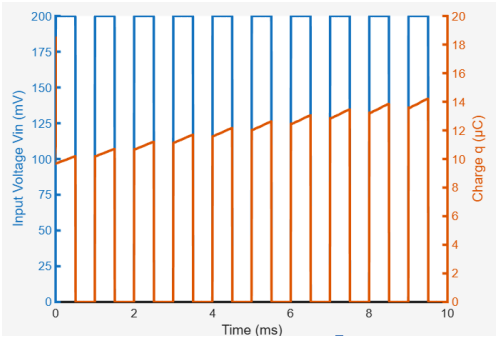


Figure 9. Observation of non-volatility in the proposed memcapacitor circuit

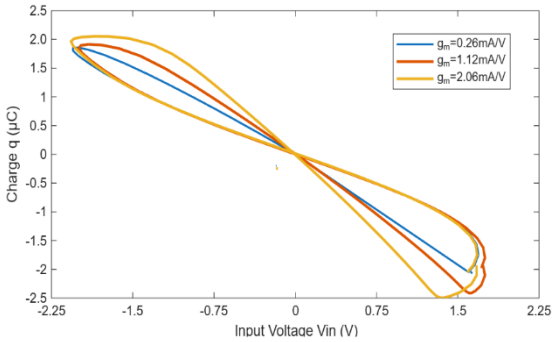


Figure 10. The PHL of memcapacitor for various values of g_m

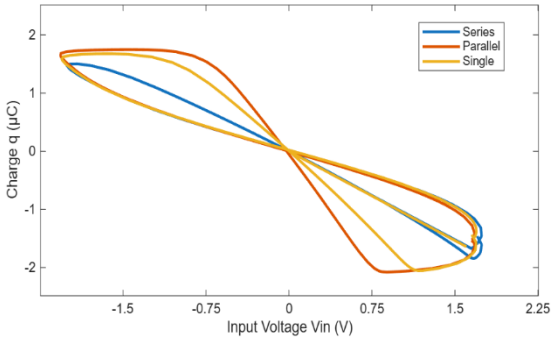


Figure 11. The PHL of memcapacitor connected in single, series and parallel configurations

The next stage verification of the proposed memcapacitor design is experimentation, which comprehensively evaluates the memcapacitor employing integrated circuits (ICs) component CCII's AD844 and OTA's CA3080 together with a smaller number of passive components that are easily available in the market. In order to accomplish experimental findings, the memcapacitor design circuit schematic as shown in Figure 12 is built on a breadboard utilizing one AD844AN, two CA3080DE, one resistor, and three capacitors. For the active components to function properly, the DC power supply voltages used are $\pm 10\ V$. The values of the passive components are $R = 1\ k\Omega,\ C_F = 0.01\ \mu H, C_1 = 10\ \mu F$ and $C_2 = 10\ \mu F$. Figure 13 displays the results of experimentation of the suggested memcapacitor circuit, particularly the whole hardware configuration with input voltage and charge waveform as shown in Figure 13(a), the circuit's top view as shown in Figure 13(b), and the pinched hysteresis curve at $f = 2\ kHz$ as shown in Figure 13(c). In this case, taking into account (8), the charge on the C_1 capacitor is precisely proportional to the voltage. The charge was acquired by the multiplication of the negative V_{C_1} voltage and the values of the C_1 capacitor. It should be noted that by inverting the voltage on the C_1 capacitor, the charge variation can be seen on the oscilloscope. Also, the PHL in Figure 14 at different frequencies experimentally are shown in Figures 14(a), 14(b), and 14(c). Again, the PHL narrows with increasing frequency. It can be shown from the test findings that the suggested memcapacitor design is a good fit for usage as a memcapacitor.

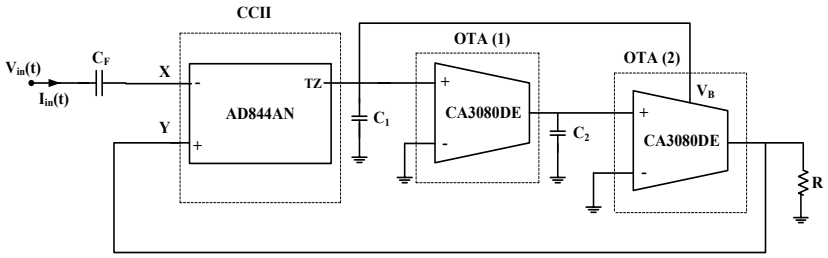
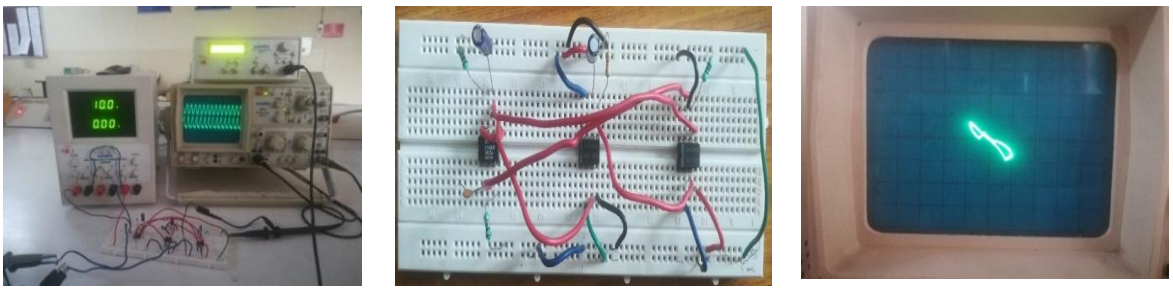
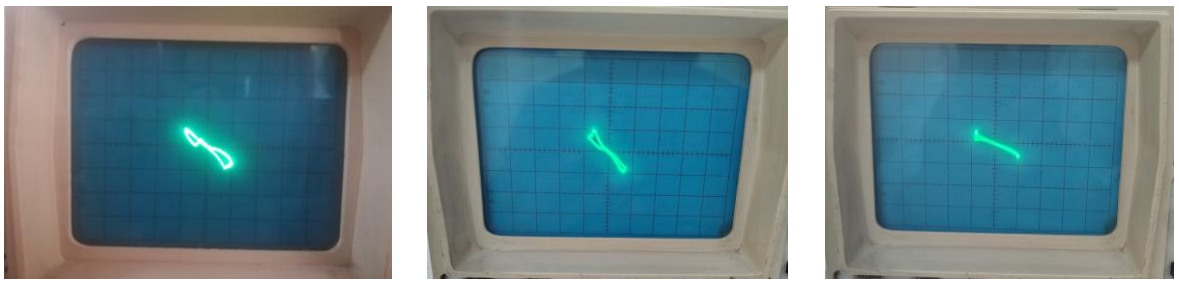


Figure 12. The proposed memcapacitor schematic diagram make use of the commercially available ICs $AD844$ and $CA3080$



(a) (b) (c)

Figure 13. Proposed memcapacitor experimentation, (a) setup for the experiment, (b) the circuit implementation shown in top view, and (c) At $f = 2\ kHz$, the pinched hysteresis curve



(a) (b) (c)

Figure 14. Experimental results of the frequency-dependent pinched hysteresis loop at: (a) $f = 2.2\ kHz$, (b) $f = 2.5\ kHz$, and (c) linear nature of proposed model at $f = 2.8\ kHz$

Lastly, the practicality of the proposed memcapacitor is demonstrated using in $R-C$ frequency selection network as shown in Figure 15. Figure 15(a) shows an example of a $R-C$ frequency selection network and given the assumption that the input voltage V_i is set up as $A_m\ sin(2\pi ft)$, the input–output characteristics of this network indicate that when f is small and $1/2\pi fC_P >> R_P$, the output voltage V_f will be phase-ahead of the input voltage V_i. However, voltage V_f lags behind the phase of the voltage V_i when f is high and $1/2\pi fC_P << R_P$. As a result, a frequency f_o is required to ensure that the phases of V_f and V_i are the same [29]. As shown in Figure 15(b), an RC_m network is created by substituting the proposed emulator for linear capacitor C_S in order to verify the memcapacitor emulator's practical availability. In order to examine the emulator dynamic performance, the circuit parameters are set as follows: $V_i = 4sin(2\pi ft)$, $R_S = R_P = 1\ k\Omega$, and $C_P = 1\ nF$. The Figure 16 shows the time-domain waveforms of the voltage V_i, the voltage across R_S (V_{Rs}), the voltage across memcapacitor V_C and the output voltage V_f. Figure 16(a) shows waveforms at $f = 750\ Hz$ and it is clear that the output voltage V_f is phase-ahead of the voltage V_i. However, the experimental waveforms at $f = 1.5\ kHz$ are shown in Figure 16(b), which shows that the output voltage V_f clearly lags behind the voltage V_i in phase. Due to the impact of suggested nonlinear memcapacitor, the output voltage V_f is now a multi-component frequency waveform instead of a single, normal sinusoidal waveform. Therefore, the phase-difference characteristic of this RC_m circuit, which was previously discussed is only useful for qualitative analysis and should not be utilized to pick a specific frequency. In reality, as Figure 16 demonstrate, voltage V_{Rs} has phase ahead of V_C because it is proportional to the current flowing through the memcapacitor emulator with coefficient R_S. In technical terms, the phase difference between V_C and V_{Rs} with respect to each frequency component is of $\pi/2$ as they are both non-standard sinusoidal waveforms. Therefore, the proposed memcapacitor design makes sense from an application perspective.

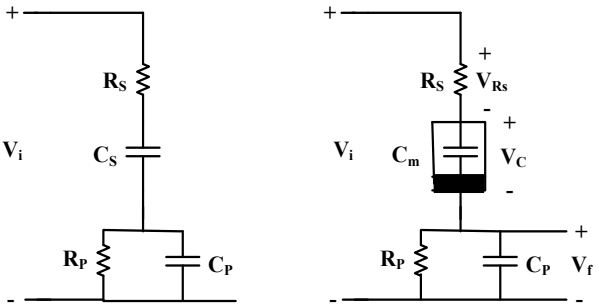


Figure 15. $R-C$ frequency selection network (a) an example of a linear $R-C$ frequency selection network and (b) an RC_m network created by substituting the proposed memcapacitor emulator for linear capacitor C_S

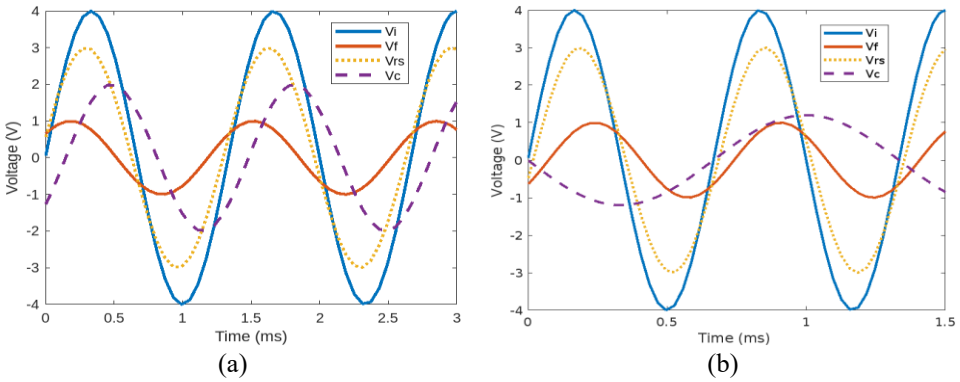


Figure 16. Waveforms of V_i, V_{Rs}, V_C and V_f at (a) $f = 750\ Hz$ and (b) $f = 1.5\ kHz$

Moreover, an adaptive neuromorphic structure is explored as an additional application of the proposed memcapacitor model. According to general research based on the memristive system demonstrates how well-known associative behavior is implemented and how the system may mimic the nature of synapses

in the brain. The aforementioned assertion is supported by a Pavlovian experiment using a memristor. This experiment contributes to our understanding of how living things evolve. The simplest unicellular creature, amoeba, has been studied recently. Its existence dates back to the origin of life on Earth. Amoeba has been shown to be sensitive to changes in humidity and temperature in its surroundings. In another way, both the ambient temperature and humidity affect the amoeba's locomotive speed. Amoeba slows down its pace in response to temperature drops and also predicts when these drops will occur in the future. The implementation of this behavior, which demonstrates the amoeba's adaptive behavior, uses a resistor, meminductor, and capacitor [30]. Adaptive behavior circuit as shown in Figure 17, which comprises of resistor, inductor and memcapacitor is utilized in a similar circuit instead of a simple capacitor.

In a typical RLC circuit, the inductor and capacitor will contribute to the resonant frequency ($f = 1/(2\Pi\sqrt{LC})$), but the resistor's power consumption causes the oscillation to decrease with time. Here, the input voltage ($(V_{in}(t))$) represents the temperature variations in the surrounding environment, while the output voltage ($(V_{out}(t))$) represents the amoeba's locomotive speed in response to temperature variations. For adaptive learning, the following component values are considered as follows: $R = 0.5\ k\Omega$ and $L = 10\ mH$ and the memcapacitor component value as $C_F = 1.6\ \mu F, C_1 = 470\ \mu F,\ C_2 = 1\ \mu F$ and $R = 1\ k\Omega$. The Figure 18 illustrates how the locomotive speed varies in response to changes in the surrounding temperature. As we can see, the voltage that corresponds to a locomotive's speed decreases at each temperature drop supporting the idea of adaptive learning. Therefore, the suggested memcapacitor design is appropriate for real-time applications.

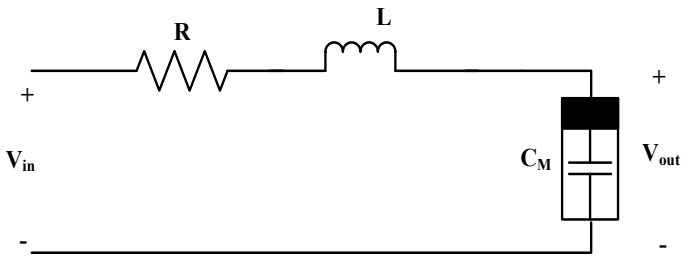


Figure 17. Circuit for adaptive learning with a memcapacitor [30]

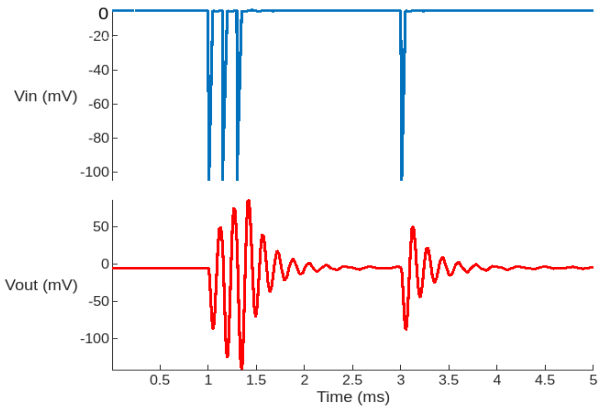


Figure 18. The output response of the adaptive learning process

5. CONCLUSION

In this work, a straightforward multiplier-less memcapacitor emulator circuit without the need for a memristor mutator technique is provided. The circuit is implemented using the fewest active and passive components, and the device layout is also shown for further verification. Additionally, the circuit functions well between 500 Hz and 2 kHz, beyond which the memcapacitor functions as a linear capacitor. Also, calculated the power consumption 33.67 mW which is comparatively low as expected. Further, the circuit's validity is confirmed by a number of simulation outcomes including the process corner, non-volatile behaviour and hysteresis curve. Additionally, the circuit is electronically controllable which is verified well

by varying g_m values. For functional verification of the circuit both parallel and series combinations of memcapacitor have been done and simulation is carried out in Cadence virtuoso and results are compared. In addition, an experimental hysteresis curve has been generated using a hardware model of the proposed memcapacitor that uses commercially available integrated circuits (ICs) AD844AN and CA3080DE. Furthermore, the proposed memcapacitor is well applicable for $R-C$ frequency selection network as well as neuromorphic application. The theoretical aspects of memcapacitors are well-verified by the results of both simulations and experiments. Because of its simplicity, the circuit can be manufactured into monolithic integrated circuits and is interoperable with other circuits, potentially enabling future extensions of the mem-system based application.

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AUTHOR CONTRIBUTIONS STATEMENT

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Rudraswamy S. B.		✓			✓					✓	✓	✓	✓	✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest. We declare that we do not have any commercial or associative interest that represents a conflict of interest in connection with the work submitted.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study.

ETHICAL APPROVAL

Authors state no use of people or animals in this study.

DATA AVAILABILITY

The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

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