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Low-power and reduced delay in inverter and universal logic gates using Hvt-FinFET technology

Veerappa Chikkagoudar[1], G. Indumathi[2]
[1]Department of Electronics and Communication Engineering, Visvesvaraya Technological University, Belagavi, Karnataka, Cambridge Institute of Technology, K.R Puram, Bengaluru, India
[2]Department of Electronics and Communication Engineering, Cambridge Institute of Technology, K.R Puram, Bengaluru, India

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ABSTRACT

The rapid scaling of conventional complementary metal–oxide–semiconductor (CMOS) metal–oxide–semiconductor field-effect transistors (MOSFETs) led to significantly increasing power dissipation, delay, and short channel effects (SCEs). Fin field-effect transistor (FinFET) technology is a better alternative to MOSFETs with superior electrostatic control, low power, and reduced leakage current. FinFETs have been chosen for their efficiency in overcoming these issues. This work focuses on the design of high-threshold voltage fin field-effect transistor (Hvt-FinFET) 18 nm technology-based inverter with optimized parameters and implementing universal gates NAND and NOR in Cadence Virtuoso tool. These three gates are basic building blocks for any complex digital system design. The results demonstrate significant improvement in power and reduced propagation delay in comparison with conventional CMOS technology. The Hvt-FinFET inverter obtained power dissipation and delay reduction of 13.63% and 33.33%, respectively. Power and delay optimization of 29.10% and 11.8% have been obtained in the NAND gate and 31.28% and 29.08% in the NOR gate when compared to conventional CMOS circuits. The results demonstrate significant improvements in power savings, reduced propagation delay, and superior energy efficiency, validating the effectiveness of Hvt-FinFET technology for next-generation very large scale integration (VLSI) applications.

Corresponding Author:

Veerappa Chikkagoudar
Department of Electronics and Communication Engineering, Visvesvaraya Technological University, Belagavi, Cambridge Institute of Technology, K.R Puram
Bengaluru – 560036, India
Email: veerappa.ece@cambridge.edu.in

1. INTRODUCTION

The rapid scaling of complementary metal–oxide–semiconductor (CMOS) processing technology has led to significant challenges, particularly in mitigating short channel effects (SCEs), power leakage, and reduced drive strength. Fin field-effect transistor (FinFET) device is emerging alternative to conventional complementary complementary metal–oxide–semiconductor field-effect transistors (MOSFETs), offering better gate control and improved overall performance. As demand for low-power and reduced delays in digital systems grows, there is a need to use FinFET-based circuit designs that enhance power efficiency and reduced delay in very large scale integration (VLSI) circuits.

The existing studies indicate that due to constant scaling, the complementary MOSFET (CMOS) circuits suffer from excessive leakage currents and short channel effects leading to increased power

dissipation [1]. Existing research on FinFET-based circuits has highlighted various limitations and gaps that need to be addressed [2]. Additionally, FinFET's, despite their superior electrostatic control, face challenges such as increased contact resistance at sub-10nm nodes, which affects performance [3], [4]. Studies have also stated that independent-gate FinFET architectures reduce power consumption but at the cost of more propagation delay [5]. Further, conventional FinFET's struggle with manufacturability issues due to high process variation, making their large-scale adoption challenging [6]. These research challenges highlight the need for optimized high-threshold voltage fin field-effect transistor (hvt-FinFET) based logic designs that reduce power, delay, and scalability compared with conventional complementary MOSFET's.

Research has shown that by optimizing device parameters like fin-height, fin-width, and higher-k gate dielectric material, FinFET's achieve better control over threshold voltage variations, reducing leakage power and improving switching performance. It has been observed that the significant control over gate and higher Ion/Ioff ratio and improved subthreshold slope [7]–[12]. FinFET-based CMOS inverters achieve a maximum voltage gain, confirming their suitability for high-speed and low power semiconductor applications [13], [14]. In digital logic design, FinFET based NAND and NOR gates have demonstrated better improvements in power reduction and delay reduction compared to conventional CMOS logic gates. Better electrostatic control of FinFETs minimizes leakage current, enhancing memory stability and efficiency [15]–[18]. Low-threshold voltage (LVT) FinFET and low-power stacked (LPS) FinFET domino design reduces standby power by 63.3% and improves power–delay product (PDP) by 81.97% for 8-input OR gates, making it a suitable option for energy-efficient VLSI implementations [19]–[21]. The introduction of a selective epitaxial process for merging individual fins enhances series resistance reduction, improving FinFET scalability for future technology nodes [22]–[25]. Overall literature review tells that FinFET technology is a need of hour for advanced semiconducter based design compared to planar CMOS with respect to high performance, low power and area [26]–[34].

This research work focuses on designing of a FinFET-based inverter using a high-threshold voltage (HVT) 18 nm node FinFET which acts as a basic building block for further design of logical and arithmetic circuits. The objective is to construct universal logic gates using FinFET based inverter, and compare their performance with conventional CMOS circuits. The study aims to analyze critical performance parameters such as power dissipation, propagation delay by taking advantage of FinFET technology for energy-efficient digital system design. The expected outcome of this work includes a comprehensive performance evaluation of FinFET-based logic gates, demonstrating improvements over conventional complementary MOSFET circuits. This work aims to establish Hvt-FinFET technology as a viable alternative for next-generation low-power digital circuits.

This work is detailed as follows: Section 1 introduction, discusses motivation for the selection of problem statement with related work, highlighting prior research on FinFET applications. Section 2 method, details the methodology, including the Hvt-FinFET inverter, NAND and NOR gate designs. Section 3 results and discussion, details simulation results and performance analysis, section 4 conclusion and further enhancement conclusion of the work and future research.

2. METHOD

Hvt-FinFET devices, based on 18 nm technology, feature a fin-shaped structure and high-k dielectric to enhance gate control and reduce leakage. Simulation setup includes schematic design with Hvt-FinFET device with optimized parameters calculated from mathematical model, testbench, and waveforms in cadence virtuoso tool. Their use in inverter, NAND, and NOR gate designs lead to lower power consumption, reduced propagation delay, and better suitability for advanced VLSI applications.

2.1. Device structure and parameters

The major geometric parameters of this FinFET as shown ini Table 1 include a fin width of 8 nm, a fin height of 20 nm, and a gate width of 20 nm, with a supply voltage V_{DD} of 0.9 V to ensure reduced power dissipation and high-speed operation. Further, the device incorporates a load capacitance C_L of 1.0fF, which plays a critical part in determining delay and power consumption.

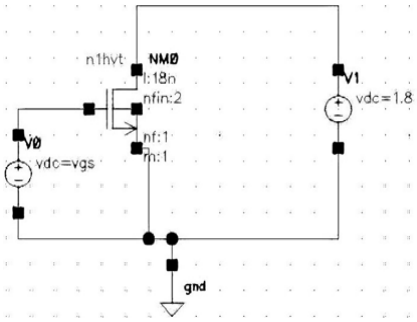
2.2. FinFET electrical characteristics

2.2.1. N-channel FinFET

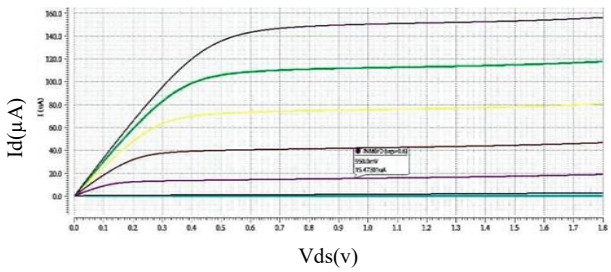
The electrical characteristics of the n-channel Hvt-FinFET is analyzed by its drain and transfer characteristics. The characteristics from Figures 1(a) to (c) provide information about drain current variation with bias voltages, threshold voltage variation, and overall device performance under different bias conditions.

Table 1. Geometric and operating parameters of the 18 nm Hvt-FinFET

Parameter	Value
Fin height (H_{fin})	20 nm
Fin width (W_{fin})	8 nm
Oxide thickness (t_{ox})	1.5 nm
Supply voltage (V_{DD})	0.9 V
Gate width (W_{gate})	20 nm
Load capacitance (C_L)	1.0 fF



(a)



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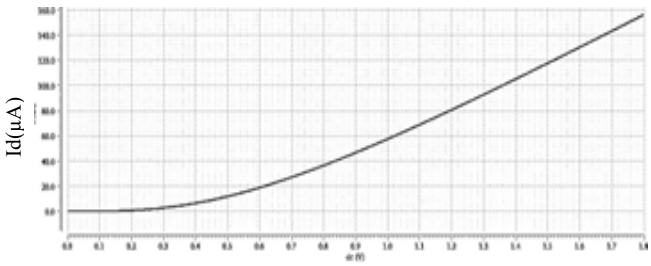


(c)

Figure 1. Drain current variation (a) schematic for N channel Hvt-FinFET drain and transfer characteristics, (b) I_d vs V_{ds} for various $V_{gs,}$ and (c) I_d vs V_{gs}

2.2.2. P-channel FinFET

The p-channel Hvt-FinFET exhibits complementary behavior to its n-channel counterpart as shown in Figures 2(a) to (c), crucial for designing efficient CMOS logic circuits. The drain and transfer characteristics provide information about performance parameters such as mobility μ, threshold voltage Vt, and leakage current.

2.3. FinFET inverter design

The FinFET inverter consists of a high-threshold voltage (Hvt) PMOS and NMOS FinFET in a complementary structure, designed to achieve enhanced gate control, low leakage current and better switching performance compared to traditional CMOS inverters is as shown in Figure 3. From a performance perspective, Hvt-FinFET inverter demonstrates a higher I_{on}/I_{off} ratio compared to traditional CMOS inverters. Further, propagation delay(τ) plays an important role in determining speed of digital logic circuits.

Hvt-FinFET inverter displays a propagation delay of 25 ps, which is three times less than the 75 ps delay observed in traditional 45 nm CMOS inverters. This reduction in delay directly contributes to faster signal transitions, enhancing the overall speed of digital circuits.

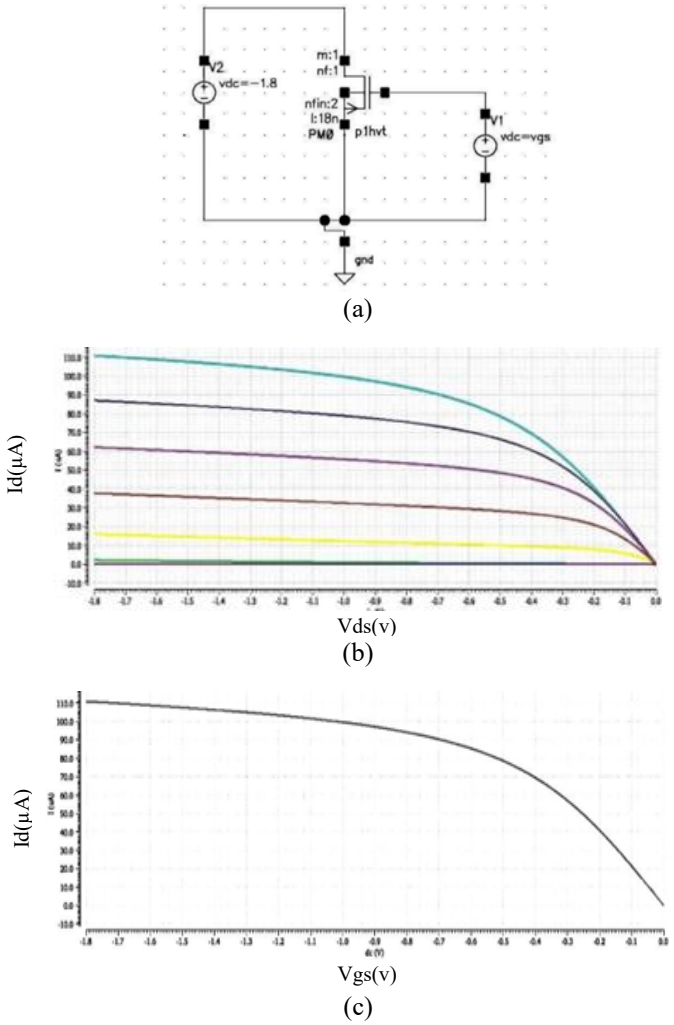


Figure 2. The p-channel Hvt-FinFET exhibits complementary behavior to its n-channel counterpart: (a) schematic for P channel Hvt-FinFET (b) Id vs Vds for various Vgs (c) Id vs Vgs drain and transfer characteristics

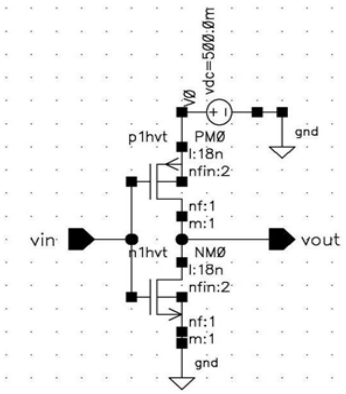


Figure 3. Schematic of the FinFET inverter

2.4. NAND and NOR gate design using Hvt-FinFET

The design of NAND and NOR gates use the advantages of high-threshold voltage Hvt-FinFET technology to improve switching performance, minimize leakage currents, and reduce power dissipation.

2.4.1. FinFET NAND gate design

The Hvt-FinFET based NAND gate comprises two series-connected nFinFET's in the pull-down network and 2 parallel-connected pFinFET's in the pull up network as shown in Figure 4. Output is false only when both inputs are true; otherwise, it remains true, ensuring minimal static power dissipation. The key parameters which affect electrical characteristics of Hvt-FinFET based NAND gate are presented in Table 2.

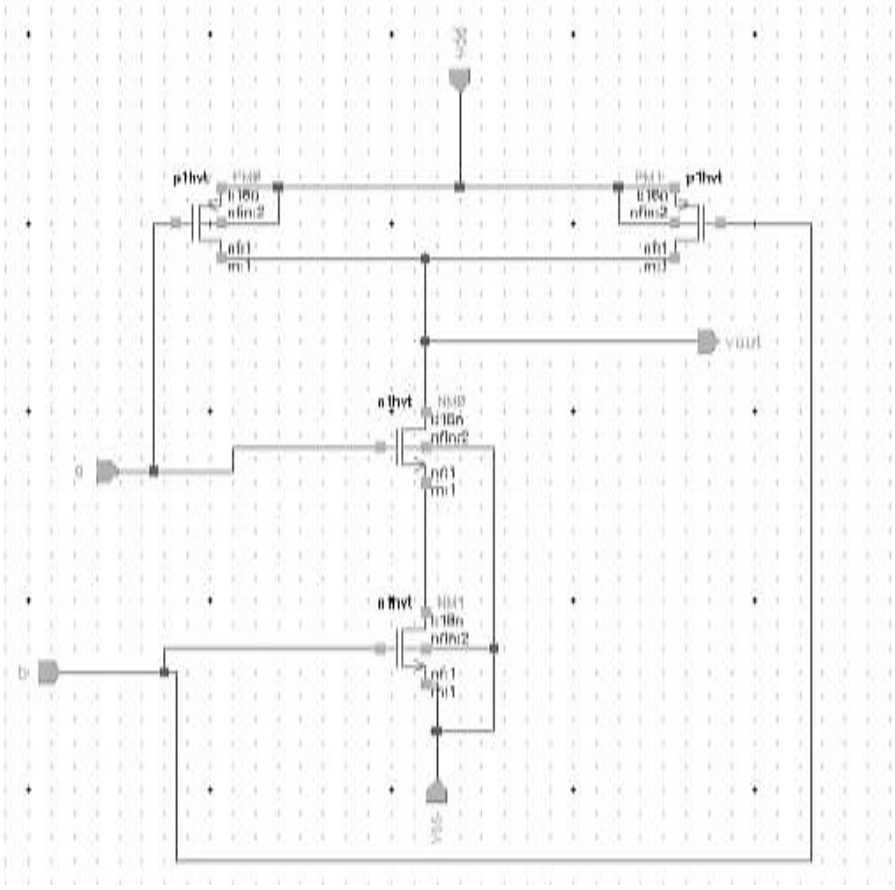


Figure 4. Schematic of the FinFET NAND gate

Table 2. Electrical parameters of the FinFET NAND gate

Parameter	Value
Supply voltage (V_{DD})	1.2 V
Threshold voltage (V_{th})	0.5 V
Subthreshold slope (S)	60 mV/decade
Effective width (W_{eff})	80 nm
Channel length (L)	18 nm
Load capacitance (C_L)	10 fF

2.4.2. FinFET NOR gate design

The Hvt-FinFET based NOR is as shown in Figure 5. The output remains logic level high only when all inputs are logic level low; otherwise, it remains logic low value(false). This complementary arrangement results in reduced static power consumption. The key parameters which affect the electrical characteristics of Hvt-FinFET based NOR gate are presented in Table 3.

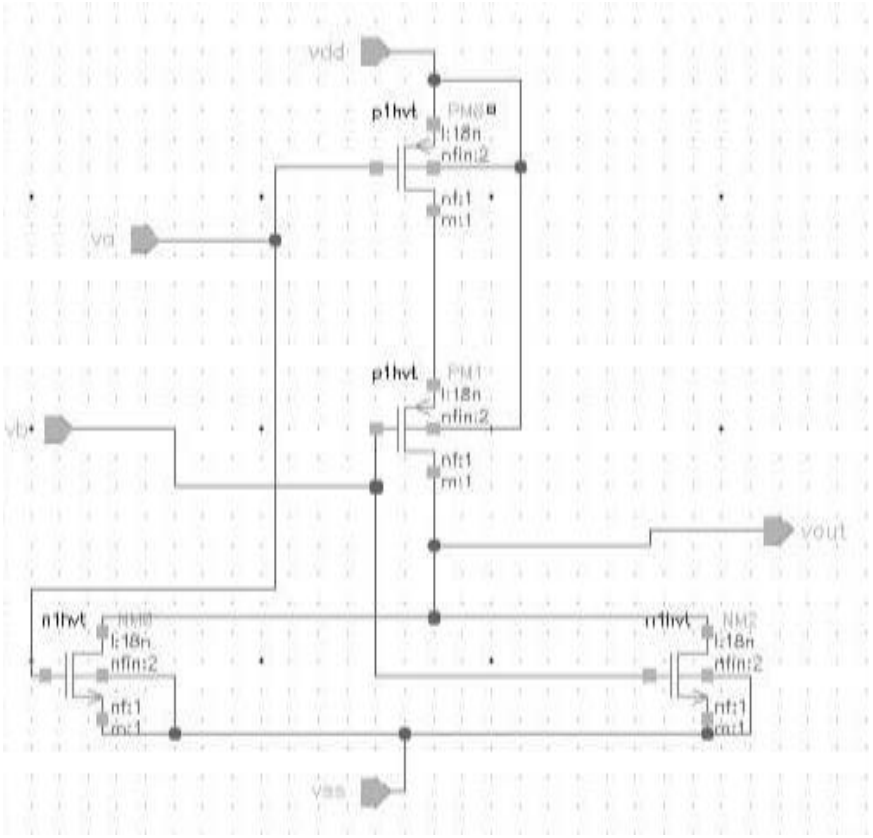


Figure 5. Schematic of the FinFET NOR gate

Table 3. Electrical parameters of the FinFET NOR gate

Parameter	Value
Supply voltage (V_{DD})	1.0 V
Load capacitance (C_L)	1 pF
Activity factor (α)	0.2
Operating frequency (f)	100 MHz
Total resistance (R_{total})	500 Ω
Internal capacitance	3 pF

2.5. Mathematical model for power and delay analysis

This section presents an in-depth analysis of power and delay characteristics for the high-threshold voltage (Hvt) FinFET based inverter, NAND, and NOR gates at the 18 nm technology node.

2.5.1. Propagation delay analysis

Propagation delay is influenced by three key parameters: load capacitance (CL), which determines the charge required for state switching; supply voltage (VDD), which governs power delivery; and ON current (Ion), where a higher Ion leads to faster switching and reduced delay. Mathematically, the propagation delay is expressed as:

$$\tau = \frac{C_L \times VDD}{I_{on}} \quad (1)$$

where τ= Propagation delay, C_L=Total load capacitance, I_{on}=ON current.

For High-threshold voltage FinFET based inverter, the design parameters include a load capacitance of 1.0 fF, a supply voltage of 0.9 V, and an ON current of 2.94 μA. Substituting these values into the equation:

$$\tau = \frac{(1.0\times10^{-15}\text{F})\times(0.9\text{V})}{2.94\times10^{-6}\text{A}} = 25\text{ps}$$

2.5.2. Power consumption analysis

Dynamic power calculated using the following equation:

$$P_{dynamic} = \alpha \times C_L \times VDD^2 \times f \quad (2)$$

whereas α is the switching activity factor normally 0.2 for inverters, CL is 1.0 fF, VDD is 0.9 V, and f is 1.0 GHz. Substituting these values:

$$\mathrm{P_{dynamic}} = (0.2) \times (1.0 \times 10^{-15}\mathrm{F}) \times (0.9\mathrm{V})^2 \times (1.0 \times 10^{9}\mathrm{Hz}) = 0.35\mu\mathrm{W}.$$

Static power dissipation is calculated as:

$$\mathrm{P_{static}} = \mathrm{I_{off}} \times \mathrm{VDD} \quad (3)$$

For the HVT FinFET inverter, where the off-state leakage current (Ioff) is 100 nA and VDD is 0.9 V, the static power dissipation is:

$$\mathrm{P_{static}} = (100 \times 10^{-9}\mathrm{A}) \times (0.9\mathrm{V}) = 0.1\mu\mathrm{W}$$

2.5.3. Hvt-FinFET NAND gate analysis

In this design of High-threshold voltage FinFET based NAND gate, the optimized design parameters used are, supply voltage of 1.2 V, a load capacitance of 10 fF, and an ON current of 2.94 μA. The propagation delay (τ) is determined using the equation (1):

$$\tau = \frac{C_{load} \times VDD}{I_{on}} = \frac{(1.0\times10^{-15}F)\times(1.2V)}{2.94\times10^{-6}A} = 4.08ns$$
$$P_{dynamic} = \alpha \times C_{load} \times VDD^2 \times f = 0.2 \times (1.0 \times 10^{-15}F) \times (1.2V)^2 \times (1 \times 10^{9}Hz) = 2.89\mu W$$
$$P_{static} = I_{off} \times VDD = (100 \times 10^{-9}A) \times (1.2V) = 120nW$$

2.5.4. Hvt-FinFET NOR gate analysis

For the Hvt-FinFET NOR gate, the propagation delay is calculated using the Elmore delay model, given by:

$$\mathrm{t_{delay}} = 0.69 \times \mathrm{R_{total}} \times \mathrm{C_{total}} = (0.69) \times (500\Omega) \times (4 \times 10^{-12}\mathrm{F}) = 1.38\mu\mathrm{s}$$
$$\mathrm{P_{dynamic}} = \alpha \times \mathrm{C_{load}} \times \mathrm{VDD^2} \times \mathrm{f} = (0.2) \times (4 \times 10^{-12}\mathrm{F}) \times (1.2\mathrm{V})^2 \times (1 \times 10^{9}\mathrm{Hz}) = 20\mathrm{mW}.$$
$$P_{static} = I\mathrm{leakage} \times VDD = (133.42 \times 10^{-9}\mathrm{A}) \times (1.2\mathrm{V}) = 160.10\mathrm{nW}. \quad (4)$$

3. RESULTS AND DISCUSSION

In this study, the propagation delay, transient and DC power consumption of Hvt-FinFET-based inverters, NAND, and NOR gates are evaluated and compared with conventional CMOS counterparts. The analysis includes both simulated and theoretical results, highlighting the impact of parasitic effects and process variations.

3.1. Propagation delay of Hvt-FinFET inverter

The delay of the Hvt-FinFET inverter as shown in Figure 6 was measured to be 27.2 ps in cadence virtuoso, whereas the theoretically calculated value was 25 ps. This slight deviation arises due to parasitic resistances, interconnect capacitances, and process variations in the simulation environment. Unlike CMOS inverters, which suffer from higher parasitic capacitance and increased leakage currents, FinFET inverters maintain a stable threshold voltage (Vth) ensuring consistent and efficient performance.

3.2. Transient and DC power consumption of Hvt-FinFET inverter

The Hvt-FinFET inverter transient and DC response is shown in Figures 7(a) and 7(b). The transient and DC power consumption measured from Figures 7(c), and 7(d) was recorded as 694.295 nW, while the DC power consumption was found to be 137.594 nW. The theoretical values for dynamic and static power were calculated as 0.35 μW and 0.1 μW, respectively.

	Expression	Value
1	27.2E-12	27.20E-12

Figure 6. Delay of Hvt-FinFET inverter

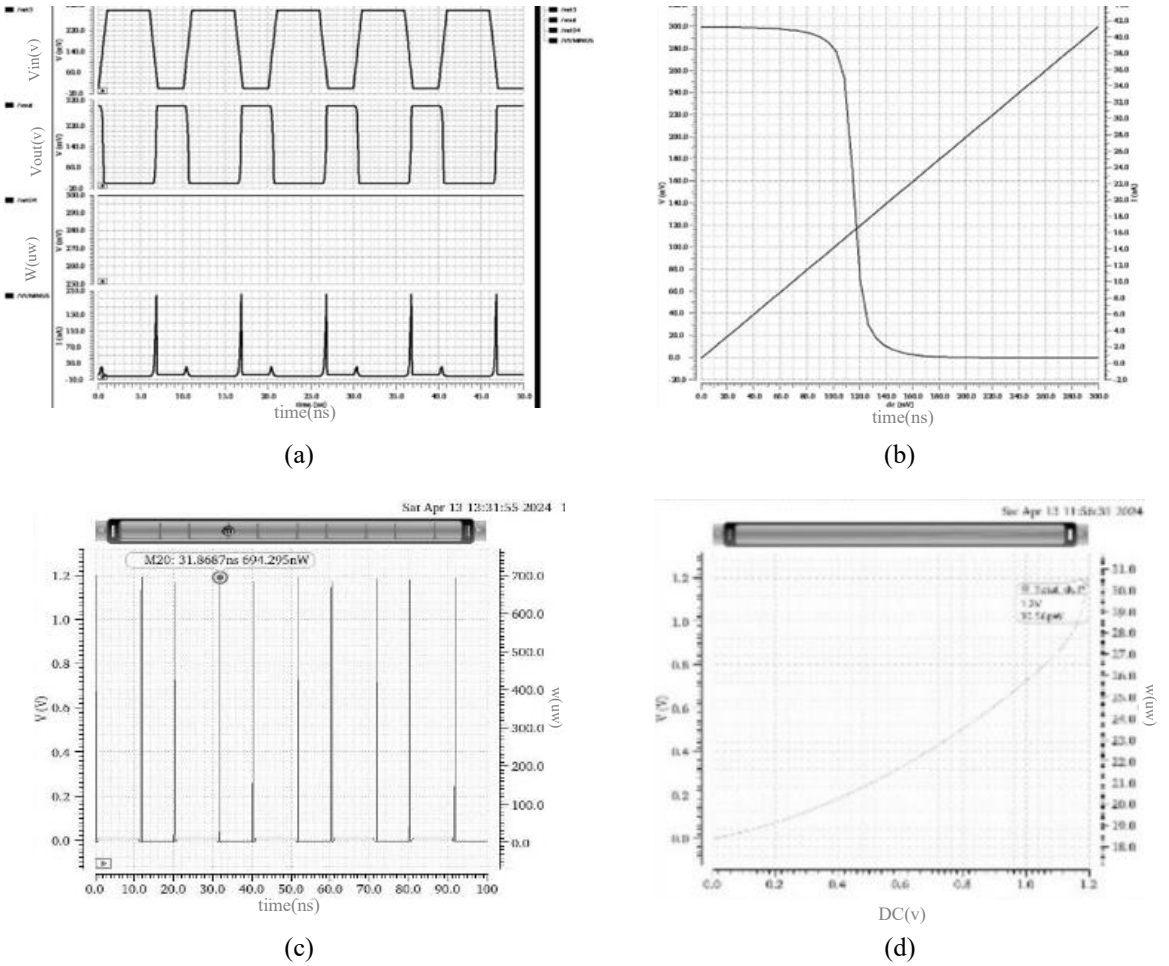


Figure 7. Hvt-FinFET inverter (a) transient response (b) DC response (c) transient power (d) DC power

3.2.2. Hvt-FinFET NAND gate performance

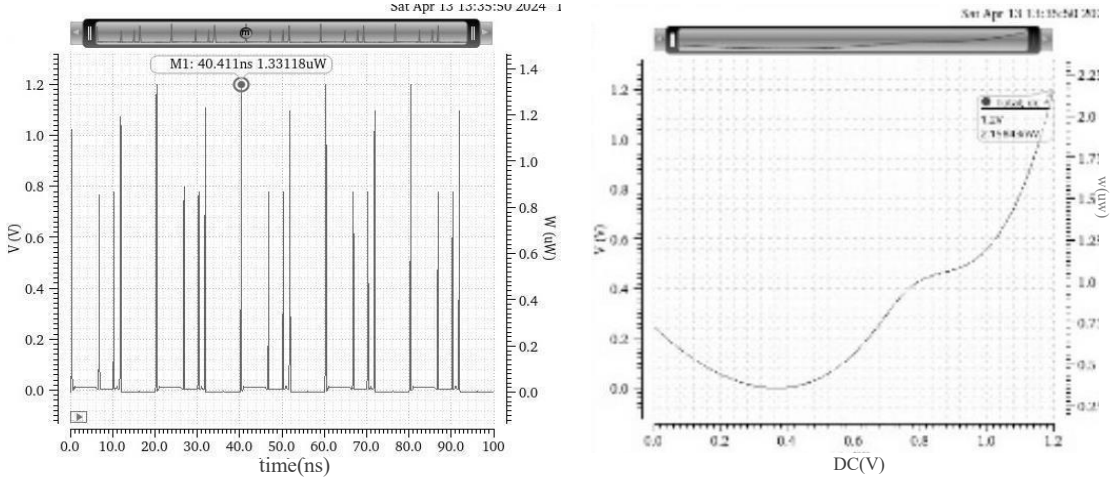
The propagation delay of the FinFET NAND gate was measured as 4.92 ns, whereas the theoretical delay was 4.08 ns. The extracted delay value is presented in Figure 8(a), confirming the expected variation in delay under practical conditions. The dynamic power consumption recorded in simulations was 1.33 µW, compared to the theoretical value of 2.88 µW. The transient power characteristics are illustrated in Figure 8(b). The static power dissipation was measured at 2.15 nW, aligning closely with the theoretical estimation of 120 mW. The DC power dissipation curve is presented in Figure 8(c).

3.2.3. Hvt-FinFET NOR gate performance

Hvt-FinFET based NOR gate exhibited propagation delay of 2.85ps, while the theoretically calculated delay was 1.38µs. The extracted delay value is presented in Figure 9(a), confirming the delay characteristics. in practical conditions. The transient power consumption was measured as 1.22 µW, compared to the theoretical value of 20 mW. This transient power behavior is illustrated in Figure 9(b). The DC power dissipation was measured at 133.42 nW, slightly lower than the theoretical estimation of 160.1 nW. The DC power dissipation curve is presented in Figure 9(c).

	Expression	Value
1	4.922E-9	4.922E-9

(a)

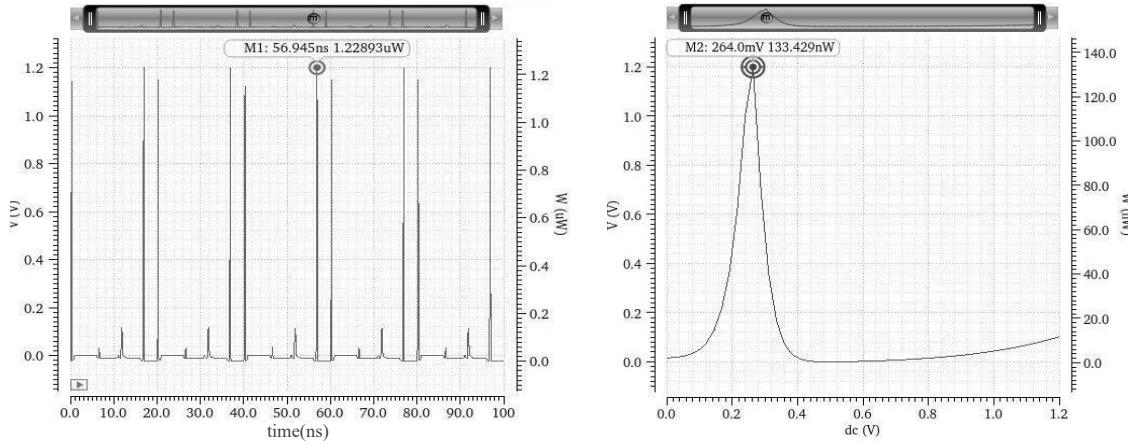


(b) (c)

Figure 8. Hvt-FinFET NAND gate (a) delay, (b) transient power, and (c) DC power

	Expression	Value
1	2.854E-12	2.854E-12

(a)



(b) (c)

Figure 9. Hvt-FinFET NOR gate (a) delay, (b) transient power, and (c) DC power

3.3. Performance comparison of Hvt-FinFET and CMOS logic gates

Hvt-FinFET 18nm technology demonstrates significant improvements over CMOS 45nm inverters and logic gates in terms of power efficiency and reduced delay as shown in Table 4. The measured propagation delays and power dissipation values closely match theoretical predictions, with minor deviations due to parasitic and process-related factors. Further, these universal gates have much lower propagation delays, indicating improved switching performance as indicated in Table 5.

Table 4. Inverters

Metric	Hvt-FinFET	CMOS
Supply Voltage (VDD)	0.9V	1.1V
Dynamic Power	0.35µW	2.5µW
Static Power	0.1µW	0.8µW
Propagation Delay (τ)	27.2ps	75ps
Ion/Ioff Ratio	~10^6	~10^4
Supply Voltage (VDD)	0.9V	1.1V

Table 5. NAND and NOR gates

Logic Gate	Metric	CMOS	HVT FinFET
NAND	Total Power	4.57µW	1.33 µW
	Propagation Delay	41.7ps	4.92 ps
NOR	Total Power	3.9µW	1.22 µW
	Propagation Delay	9.8ps	2.85 ps

4. CONCLUSION AND FURTHER ENHANCEMENT

FinFET technology with high threshold voltage variation has proved to be an efficient alternative to conventional CMOS. Compared with CMOS technology, Proposed Hvt-FinFET inverter obtained power and propagation delay reduction of 13.63% and 33.33% respectively. The power and delay optimization of 29.10% and 11.8% have been observed in the low power NAND gate. NOR gate exhibits reduction of power consumption and delay by 31.28% and 29.08% respectively. The results demonstrate that FinFET-based circuits consume substantially less power, making them ideal for low-power, high-performance VLSI applications when compared to CMOS 45nm technology. The Ion/Ioff ratio of Hvt-FinFET ($\approx 10^6$) is significantly higher than CMOS ($\approx 10^4$), ensuring better drive current and reduced leakage. These advancements confirm Hvt-FinFET's superior electrostatic control and energy efficiency, positioning it as a key enabler for next-generation VLSI circuits, AI accelerators, and IoT devices.

Future research should focus on further optimizing FinFET architectures to enhance performance and scalability. Potential improvements include hybrid FinFET-Gate-All-Around (GAA) designs, dynamic threshold tuning, strain engineering, and 3D FinFET stacking to further minimize leakage and improve switching efficiency. Continued advancements in FinFET fabrication and integration techniques will drive scalability, cost-effectiveness, and widespread adoption in modern electronic systems.

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AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Veerappa Chikkagoudar	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
G. Indumathi		✓		✓	✓		✓			✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, VC, upon reasonable request.

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BIOGRAPHIES OF AUTHORS

Veerappa Chikkagoudar received the B.Eng. degree in electronics and communication engineering from PES College of Engineering, Mandya, Mysore University Karnataka, India 2001 and the M.Tech. in Digital Electronics, B V Bhoomaraddi College of Engineering and Technology in Hubballi, Visvesvaraya Technological University, Belagavi, Karnataka., and currently pursuing Ph.D. under Visvesvaraya Technological University. Currently, he is an associate professor at the Department of Electronics and Communication Engineering, Cambridge Institute of technology, Bengaluru. His research interests include academic interests include analog circuits, digital circuits, hardware description language, CMOS VLSI, microprocessor, microcontroller, and embedded systems. Doing research in the area of digital circuit design in VLSI technology. He can be contacted at email: veerappa.ece@cambridge.edu.in.

G. Indumathi holds a Ph.D. in VLSI technology from Dr. M.G.R University Chennai, India. She is currently Principal of Cambridge Institute of Technology, Bengaluru, Karnataka, India. She received B.Eng. degree in Electronics and Communication Engineering from SJCE Mysore, Mysore University in the year 1987. M.Tech. Industrial Electronics from SJCE Mysore under VTU in the year 2003. Received Women of the year award at CITECH in 2019, CESEM Award in 2010 by DST G.O. K, along with the team received best science tech award from DST G.O. I in 2000. Educators Award during 2024 and has developed processes and systems for accreditation and teaching learning. Conducted several faculty development programs towards accreditation and TLP. The academic interest includes computer networks, VLSI, multimedia communication, computer architecture, SOC design, HPCN, embedded systems, and internet of things. She can be contacted at email: indumathi.ece@citech.edu.in and principal@cambridge.edu.in.