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Improving time-domain winner-take-all circuit for neuromorphic computing systems

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ABSTRACT

With the rapid advancements of information processing systems, winner-take-all (WTA) circuits have emerged as essential components in a wide range of cognitive functions and decision-making applications. Neuromorphic computing systems, inspired by the biological brain, utilize WTA circuits as selective mechanisms that identify and retain the strongest signal while suppressing all others. In this study, we present an effective time-domain WTA circuit with optimized multiple-input NOT AND (NAND) gate and delay circuit for neuromorphic computing applications. The circuit is evaluated using sinusoidal current inputs with varying phase delays, which successfully demonstrating precise winner selection. When applied to neuromorphic image recognition task, the enhanced time-domain WTA achieves an improvement of 0.2% in precision while significantly reducing power consumption, yielding a low figure of merit (FoM) of 0.03 µW/MHz, compared to the previous study with FoM of 0.25 µW/MHz. The optimized WTA circuit is highly promising for large-scale neuromorphic applications.

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1. INTRODUCTION

Recently, artificial neural networks (ANNs) have achieved remarkable successes in edge computing and internet of things (IoT) applications [1]–[3]. However, ANNs require huge computational task and memory resources, presenting challenges for their implementation in resource-constrained edge devices [4]. To address this, implementing biologically inspired mechanisms on hardware, known as neuromorphic computing systems, offers a promising path toward more efficient computation [5]. Neuromorphic computing systems, inspired by the biological brain, utilize winner-take-all (WTA) circuits as selective mechanisms that identify and retain the strongest signal while suppressing all others.

WTA circuit, which is widely known for its capability to identify the maximum voltage (or current) among multiple inputs, mimicking the competition mechanism in biological brain [6]–[8]. The WTA circuits are utilized in various fields, such as competitive learning, signal processing, and neuromorphic computing [9]. WTA can be classified into current conveyor-based WTA, binary tree-based WTA, and time-domain WTA.

Current conveyor-based WTA circuits utilize current-mode circuits to compare input signals represented by the input currents [10]–[14]. These circuits typically employ a second-generation current conveyor to enhance speed and precision. The principle of operation relies on transconductance elements that compete to determine the highest input current. Current conveyor-based WTA circuits excel in precision and speed, making them ideal for high-performance analog processing applications. However, they can be complex and consume moderate power.

Binary tree-based WTA circuits use a hierarchical structure where inputs are recursively compared in pairs, forming a tree topology [15]–[17]. Each level of the tree eliminates weaker inputs until the largest input propagates to the output. This structure ensures logarithmic comparison complexity, improving scalability for large input sets. Binary tree-based WTA circuits offer excellent scalability due to their hierarchical structure, making them suitable for large-scale competitive neural networks. However, they consume higher power due to the number of transistors required for pairwise comparisons.

Time-domain-based WTA circuits exploit delay elements and time-encoding mechanisms to determine the winner [18]–[21]. Inputs are converted into timing signals, where the first arriving pulse signifies the maximum input. This approach leverages the time-domain properties of signals, reducing power consumption and area requirements compared to traditional voltage- or current-mode circuits. Time-domain-based WTA circuits stand out in low-power applications due to their reliance on time-encoding rather than direct voltage or current comparison. They are highly area-efficient but may suffer from precision limitations due to variations in delay elements. Time-domain solutions are becoming more popular due to their compatibility with low-voltage complementary metal oxide semiconductor (CMOS) technology. One of the most notable time-domain WTA implementations was presented by Rahiminejad *et al.* [21], demonstrating competitive performance in terms of power efficiency and precision. The proposed WTA consumes less power and produces high precision. However, it utilizes a three-input NOT AND (NAND) gate to compare the input voltage with each other, as the number of inputs increases, the number of input gates increases too, leading to the complexity in the design of multiple input NAND gate. Although their detailed circuit structure is beyond the scope of this paper, their reported results provide a valuable reference for evaluating our proposed improvements.

In this work, we present an improved time-domain WTA circuit that addresses both scalability and performance limitations of previous designs. By optimizing the multi-input NAND logic and refining the delay circuit structure, our proposed design achieves better timing precision, reduced power consumption, and enhanced area efficiency. To evaluate its effectiveness, we compare our results with those reported in the time-domain WTA by Rahiminejad *et al.* [21] and other conventional implementations. This design aims to meet the energy constraints and performance demands of modern neuromorphic systems.

The rest of the paper is organized as follows: Section 2 describes the proposed time-domain WTA circuit, including the architecture of the 10-input NAND gate and the improved current-controlled delay cell. Section 3 presents the simulation results and performance evaluation, including comparisons with previous implementations in terms of precision, power consumption, and figure of merit (FoM). Section 4 concludes the paper and suggests directions for future research.

2. METHOD

The WTA circuit is essential for neuromorphic computing, as it enables the selection of the best-matching input pattern from a set of stored patterns. To achieve this, the circuit determines the most dominant input signal among multiple current inputs in a neuromorphic computing context. As shown in Figure 1, the circuit architecture includes two primary components: i) a current-controlled delay cell that converts analog current magnitude into time delay, and ii) a multi-input NAND gate that detects the earliest arriving signal, thereby determining the winner.

It is composed of current-controlled delay circuits, followed by multiple-input NAND gates. The analog currents are first converted to the delay times by the delay circuits and the multiple-input NAND gates generate the winner output while suppressing the others. The previous design was implemented and fabricated with only three inputs, relying on a three-input NAND gate. As the number of inputs increases, the design of multiple-input NAND gate may experience significant overhead. In this work, we enhance the performance of the time-domain WTA circuit for a ten-output neuromorphic computing system. A simplified 10-input NAND gate is introduced, along with a novel delay circuit that reduces the number of transistors, thereby optimizing area efficiency. The conceptual schematic of the improved WTA circuit is presented in Figure 1, where the current-controlled delay circuits and the 10-input NAND gates are optimized to improve power and area efficiency. In Figure 1, the blue region contains current-controlled delay cells that convert input current magnitudes into time delays. The lower red region comprises multi-input NAND gates and inverters that detect the earliest signal arrival and determine the winner.

The number of inputs in the NAND gates directly corresponds to the number of outputs in time-domain WTA circuits. Previous work demonstrated the superior performance of a time-domain WTA circuit with three outputs. However, as the number of outputs increases, the number of inputs for each NAND gate must also increase, thereby requiring a higher fan-in. Designing conventional NAND gates with a large fan-in necessitates additional CMOS transistors, which adversely affects power consumption, circuit area, and delay.

The number of outputs in the time-domain WTA circuit is extended to associate with neuromorphic computing applications for multiple-class classification. To simplify the circuit, we propose an optimized multi-input NAND gate design that employs a network of pMOS transistors combined with a pull-down nMOS transistor, as illustrated in Figure 2. When any input is pulled down to 0, the output V_{out} is driven to V_{DD}. Conversely, when all inputs are high, no pMOS transistor is activated, causing the output to be pulled down to 0, implementing the NAND operation. The optimized 10-input NAND gate utilizes fewer transistors compared to the conventional implementation, which is typically constructed by stacking 2-input NAND gates in a tree structure.

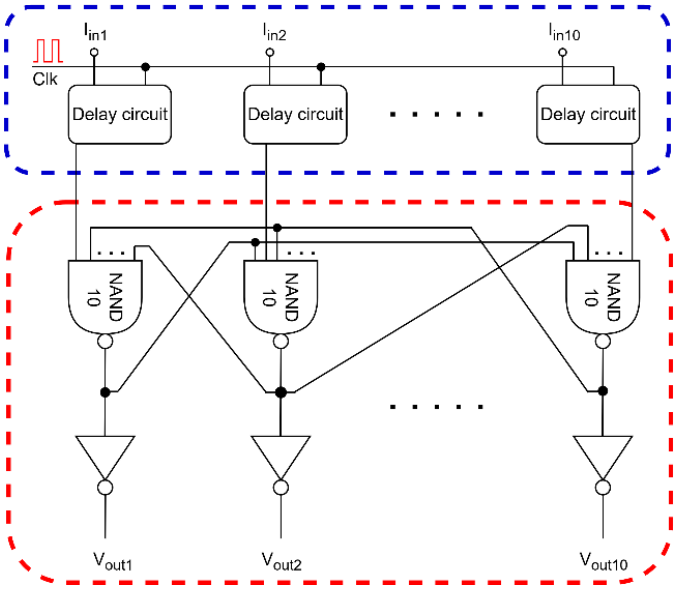

Figure 1. Architecture of the proposed WTA circuit with 10 current inputs

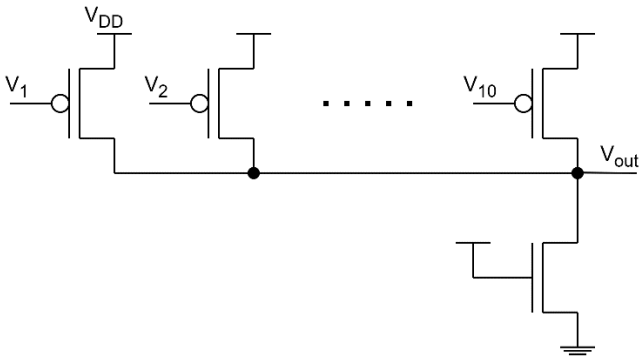

Figure 2. The simplified NAND gate with fan-in of 10

The number of outputs in the time-domain WTA circuit is extended to associate with neuromorphic computing applications for multiple-class classification. To simplify the circuit, we propose an optimized multi-input NAND gate design that employs a network of pMOS transistors combined with a pull-down nMOS transistor, as illustrated in Figure 2. When any input is pulled down to 0, the output V_{out} is driven to V_{DD}. Conversely, when all inputs are high, no pMOS transistor is activated, causing the output to be pulled down to 0, implementing the NAND operation. The optimized 10-input NAND gate utilizes fewer transistors compared to the conventional implementation, which is typically constructed by stacking 2-input NAND gates in a tree structure.

The time-domain WTA circuit operates based on a delay circuit that amplifies the time delay difference induced by the input signals. This delay, in conjunction with the simplified 10-input NAND gate, facilitates the selection of the winner output, as illustrated in Figure 1. The delay circuit is a critical

component of the time-domain WTA, as it converts the voltage or current value into a corresponding time delay representation. In this work, we propose a current-controlled delay circuit, which can serve as a termination element for columns in a crossbar circuit to identify the maximum current in neuromorphic computing systems. In the proposed design, each input current is fed into a dedicated delay circuit, where higher current results in shorter delay. The delay cell consists of a current mirror, followed by a clock-controlled inverter and an output inverter, as depicted in Figure 3. The circuit demonstrates the delay generation mechanism in relation to the input clock pulse. When the clock pulse is applied, the conductivity of the nMOS transistor is regulated by I_{in}, which is determined by the magnitude of the input current. As I_{in} increases, the resulting delay decreases, whereas a lower I_{in} leads to an increased delay. This behavior is attributed to the operating principle of the current mirror circuit [22].

To enhance the sensitivity of the WTA circuit, additional delay cells are cascaded in series, as shown in Figure 4. This configuration extends the delay at the output pulse when the input current is lower than the saturation threshold of the nMOS transistor. Cascading multiple delay cells not only increases the temporal resolution of the WTA circuit but also reduces the influence of device variations. In scaled CMOS technologies, individual transistors may exhibit mismatch in threshold voltage, current drive, or delay characteristics due to manufacturing variations. When only a single delay cell is used, these mismatches can significantly affect the timing, especially when input currents are close in magnitude. By cascading several delay stages, the total delay becomes a summation of multiple sub-delays, which helps average out random variations and amplify the timing differences between competing inputs. This makes it easier for the circuit to detect small differences in input strength, even if the chip has slight imperfections from fabrication.

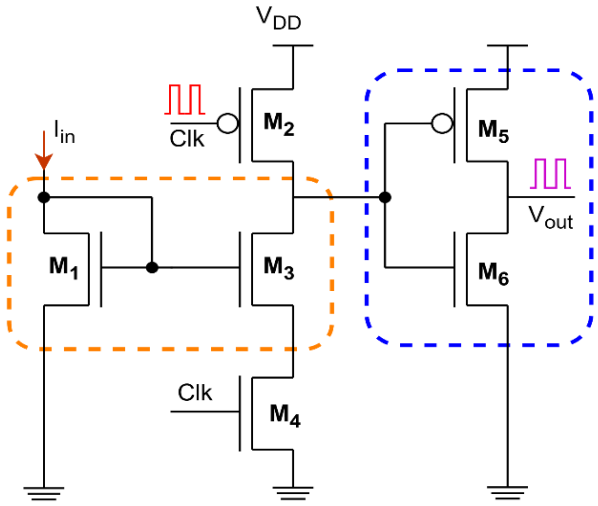

Figure 3. The proposed current-controlled delay cell. The orange region represents the current mirror, the blue region shows the output inverter, and transistors M2 and M4 form the clock-controlled inverter

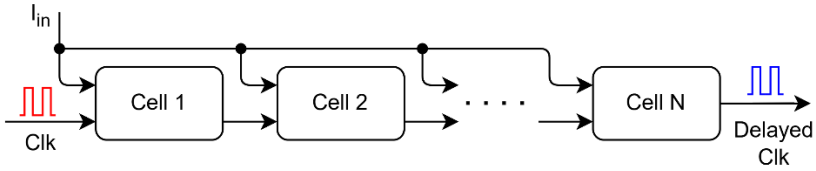

Figure 4. Delay circuit with many delay cells connected in series

3. RESULTS AND DISCUSSION

The improved time-domain WTA circuit is designed to support 10 parallel input currents and generate 10 corresponding output voltages, enabling competition among multiple neuromorphic signals. To validate its performance, the circuit is simulated using the Cadence Specter 90 nm CMOS technology process. The simulation focuses on evaluating timing accuracy, power consumption, and functional correctness across all inputs, confirming the ability of the circuit to consistently identify the dominant signal.

To simulate a competitive input scenario, the WTA circuit is driven by 10 sinusoidal current sources, each configured with a distinct phase shift. This arrangement ensures that, at any given moment, only one input current reaches its peak value, allowing clear identification of the dominant signal, as illustrated in Figure 5. The sinusoidal inputs operate at a frequency of 1 MHz, while the global clock signal controlling the circuit logic runs at 10 MHz.

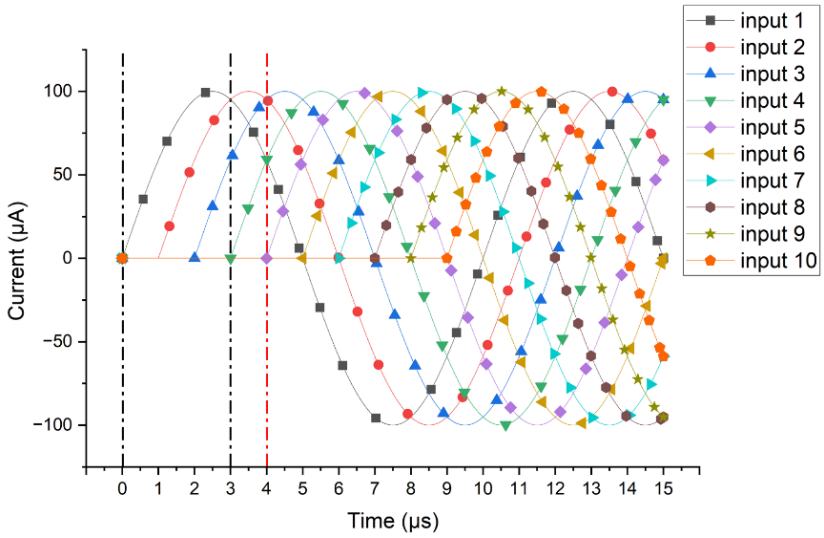

Figure 5. Ten sinusoidal current sources for testing the time-domain WTA

Figure 6 presents the output pulses of the 10-output time-domain WTA circuit, corresponding to the 10 sinusoidal input currents with different phases. The bottom waveform represents the system clock operating at 10 MHz. During the time interval from 0 µs to 3 µs, the input current i_1, shown as the black line in Figure 5, reaches its maximum value. Consequently, the WTA circuit generates an output pulse at V_1, represented by the brown signal, indicating that i_1 is the dominant input. Similarly, during the time interval from 3 µs to 4 µs, i_2 attains the highest current value, resulting in an output pulse appearing at V_2. The simulation results confirm that the WTA circuit accurately generates output pulses in real time, precisely corresponding to the maximum input current at each moment.

The proposed time-domain WTA is then applied to memristor-crossbar-based neuromorphic computing for pattern recognition using the exclusive-NOR (XNOR) operation [23]. The memristor crossbar has been effectively demonstrated in neuromorphic image recognition by measuring the similarity between the input image and the stored images [24]. Figure 7 conceptually illustrates a memristor-based neuromorphic circuit for image recognition, leveraging the XNOR operation. The XNOR function is decomposed into OR and AND operations, which can be implemented using two memristor crossbars and Kirchhoff's current law [25]. The output column current represents the similarity score between the input image and each stored image in the crossbar. A WTA circuit is placed at the crossbar's terminal to generate the output pulse, identifying the best-matching pattern.

The crossbar circuit is designed to store 10 Modified National Institute of Standards and Technology (MNIST) images representing the digits 0 to 9, as illustrated in Figure 8. Each grayscale image is flattened into a binary vector of 784 elements, where each pixel is quantized by thresholding at the mid-range intensity value; pixel values above this threshold are set to 1, and those below to 0. In this binary representation, 0 corresponds to a voltage of 0 V, while 1 corresponds to V_{DD}. The crossbar M+ consists of 10 columns to store the original images, while M− includes 10 columns to store the inverted versions of these images [25].

Figure 9 illustrates the output currents generated by the crossbar when 10 input images, corresponding to digits 0 through 9, are sequentially applied. For each input image, the crossbar produces 10 output currents (i_0 to i_9), one for each stored class. The results show that, in each case, the highest current consistently appears at the output line corresponding to the input image label. For example, i_0 peaks when Image #0 is applied, and i_9 peaks when Image #9 is applied. This behavior demonstrates that the crossbar successfully performs similarity matching between the input and stored images, effectively encoding class similarity as current magnitude. These output currents are then fed into the WTA circuit, which selects the winner based on the highest current value.

Figure 10 presents the output of the WTA circuit when 10 images are sequentially applied to the crossbar. When Image #0 is used as the input, the WTA generates a pulse at Output 0, indicating that the input image best matches the image stored in the first interval from 0 µs to 1 µs. Overall, the WTA circuit successfully produces output pulses corresponding to the input images, verifying its proper functionality within the neuromorphic crossbar circuit.

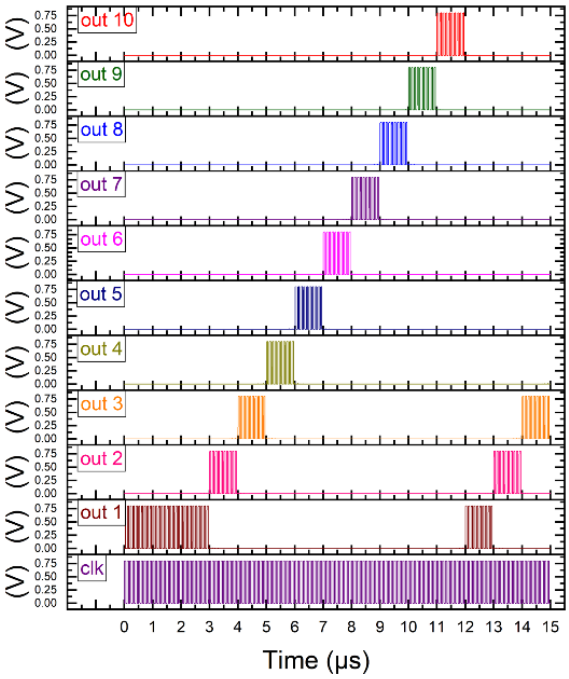

Figure 6. The output signal of the time-domain WTA when testing with 10 sinusoidal signals in Figure 5

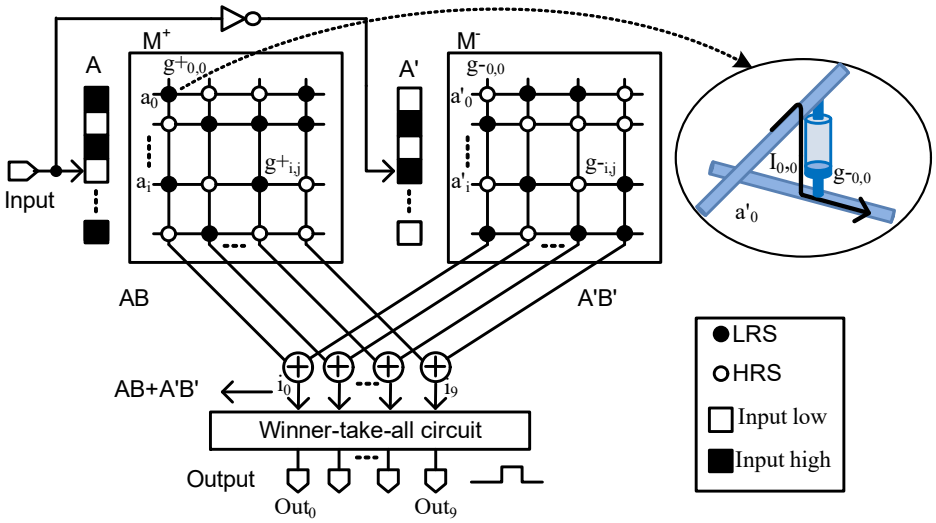

Figure 7. The conceptual of memristor crossbar circuit [25]

Figure 8. Ten MNIST samples used to test the neuromorphic circuit

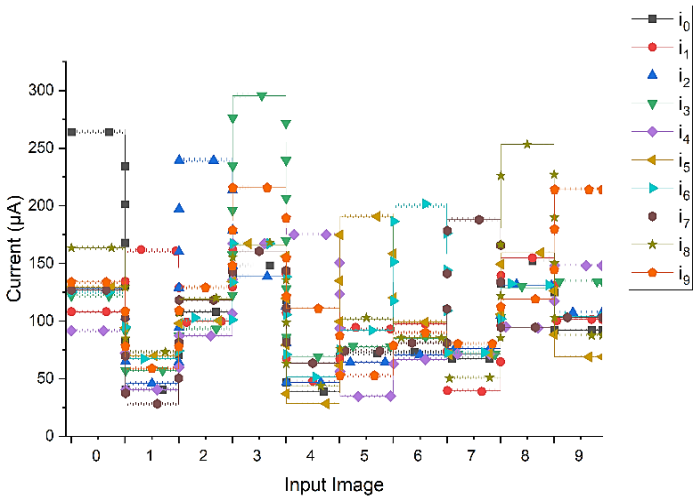

Figure 9. Output currents from the memristor crossbar for 10 distinct MNIST input images. For each input, the current corresponding to the correct image class is maximized, demonstrating successful similarity matching by encoding the result as current magnitude

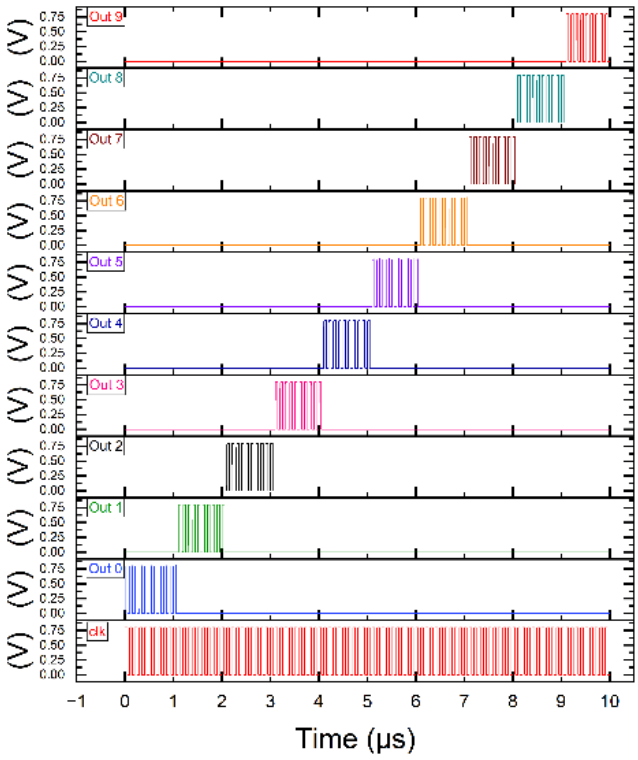

Figure 10. Output response of the WTA circuit to a sequence of 10 input MNIST images. The output pulses at Out 0 to Out 9 are generated sequentially, with each pulse corresponding to an input image within a 1 μs interval, demonstrating the circuit's sequential pattern-matching capability

To enable a fair comparison with previous work, we reproduced a time-domain WTA circuit presented in [21], which has demonstrated low power consumption and high accuracy using a 90 nm CMOS process. The 10-input NAND gate is designed by cascading a series of 2-input NAND gates to balance the delay paths. The performance of WTA circuit was evaluated in terms of the precision and FoM using (1) and (2):

$$precision = 1 - \frac{r}{R}, \quad (1)$$

$$FoM = \frac{P}{f \times N}, \quad (2)$$

where r and R represent the resolution and dynamic input voltage range of the circuit, respectively. P, f, and N denote the power consumption, the system clock frequency, and the number of input signals, respectively.

The proposed circuit improves resolution and power efficiency by simplifying the delay path and NAND gate. Specifically, by directly applying the regulated voltage to the gate terminal of M_3, generated by input current I_{in}, as presented in Figure 3, and removing the pulled-up transistors, the circuit operates effectively with a minimum resolution of 0.03 V, while V_{DD} is 0.8 V and the dynamic input range from 0.2 V to V_{DD}. The precision is calculated using (1). The previous work achieved a precision of 99.3%, whereas the proposed design attains a precision of 99.5% due to the simplification of the NAND gate and delay circuits. FoM can be calculated using (2). The previous WTA circuit achieves an FoM of 0.25 µW/MHz, while the proposed design yields an FoM of 0.03 µW/MHz. The lower FoM indicates a significant reduction in power consumption in the improved WTA circuit.

Compared to current conveyor-based and binary-tree-based WTA circuits, the proposed time-domain design offers better area and power efficiency, making it a strong candidate for large-scale neuromorphic systems where energy constraints are critical. While current conveyor-based approaches often deliver higher accuracy, they rely on complex analog components and consume more power. In contrast, our circuit uses simpler, digitally compatible structures, which are easier to scale and integrate. These advantages suggest that the proposed design could serve as a foundation for future research and development in neuromorphic systems.

Despite the improvements, the proposed WTA circuit still faces several limitations. First, the design and evaluation are based on simulations using ideal current sources, which do not fully capture the variability, noise, and non-linearity present in real-world analog input signals. This may result in degraded performance when deployed in practical systems. Second, although the circuit works well with a basic pattern-matching task on binarized MNIST images, this dataset is relatively simple and does not reflect the complexity of modern AI workloads. Real-world neuromorphic applications often involve high resolution data, time varying signals, or even multimodal inputs. As such, the current design still needs to be improved in terms of robustness, scalability, and hardware integration before it can be effectively used in practical systems. In future work, we will continue to simulate and improve the circuit design with the goal of reducing sensitivity to noise and device mismatch.

4. CONCLUSION

In this work, we optimize the time-domain WTA circuit by simplifying the multi-input NAND gate and the delay circuit, making it well-suited for neuromorphic computing applications. The circuit is tested using sinusoidal input currents with different phase shifts and accurately determines the winner output. The improved time-domain WTA is applied to neuromorphic systems for image recognition, achieving a 0.2% improvement in precision while reducing power consumption and yielding a FoM of 0.03 µW/MHz, compared to 0.25 µW/MHz in the previous study. The optimized WTA design shows great promise for large-scale neuromorphic applications.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Son Ngoc Truong	✓	✓			✓	✓	✓	✓		✓		✓		
Tu Tien Ngo			✓	✓	✓	✓	✓	✓	✓		✓			

C : **C**onceptualization
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So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, SNT, upon reasonable request.

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