

Simulation and experimental validation of modular multilevel converters capable of producing arbitrary voltage levels using the space vector modulation method

Tran Hung Cuong¹, Pham Chi Hieu², Pham Viet Phuong²

¹Faculty of Electrical and Electronic Engineering, Thuyloi University, Hanoi, Vietnam

²Department of Automation Engineering, School of Electrical and Electronic Engineering, Hanoi University of Science and Technology, Hanoi, Vietnam

Article Info

Article history:

Received Apr 29, 2025

Revised Aug 18, 2025

Accepted Sep 15, 2025

Keywords:

Experiments for MMC
Modular multilevel converter
Optimal switching
Space vector modulation
Sub module

ABSTRACT

Modular multilevel converters (MMC) used for DC-AC energy conversion are becoming popular to connect distributed energy systems to the power systems. There are many modulation methods that can be applied to the MMC. The space vector modulation (SVM) method can produce a maximum number of levels, *i.e.*, $2N+1$, in which N is the number of sub-modules (SMs) per branch of the MMC. The SVM method can generate rules to apply to MMCs with any number of levels. The goal of this proposal is to easily expand the number of voltage levels of the MMC when necessary while still ensuring the quality requirements of the system. The proposed SVM method only selects the three nearest vectors to generate optimal transition states, therefore making the computations simpler and more efficient. This has reduced the computational load when compared to the previously applied SVM methods. This advantage ensures an optimal switching process and harmonic quality which will significantly improve the effectiveness of the proposed method was demonstrated through simulations on MATLAB/Simulink and experimental tests on 13-levels voltage MMC converter system using a 309 field-programmable gate array (FPGA) kit.

This is an open access article under the [CC BY-SA](#) license.



Corresponding Author:

Pham Viet Phuong

Department of Automation Engineering, School of Electrical and Electronic Engineering, Hanoi University of Science and Technology

1 Dai Co Viet Road, Bach Mai ward, Hanoi, Vietnam

Email: phuong.phamviet@hust.edu.vn

1. INTRODUCTION

Nowadays, solar power plants with large capacity always create challenges in converting electricity from direct current (DC) to alternating current (AC) with high capacity and high voltage. Conventional power electronic converters cannot meet the conversion requirements at high voltage levels due to the limited tolerance of semiconductor valves. Therefore, new converters, specifically multilevel converters, are needed to perform these conversion tasks. Some multi-level converters can meet high voltage power conversion requirements such as neutral-point clamped (NPC), cascaded H-bridge (CHB), clamp diode [1], [2]. However, these converters have many structural limitations and apply control solutions when the voltage level is too high. At that time, voltage level expansion will become difficult, and the converter will be cumbersome, making the application of the valve opening and closing laws by conventional methods difficult when using microprocessor devices [3]. The modular multilevel converter (MMC) multilevel converter has a lot of advantages that can overcome the disadvantages of the above multilevel converters as: has a simple

configuration and easy to scale to any voltage level without interfering with modulation and control process [4]. Therefore, this converter is easily applied to large-capacity, high-voltage solar power plants to convert electricity from DC to AC directly connected to the grid [5]. The structural feature of the MMC converter is that it does not require a filter or an intermediate transformer on the output side, the system connecting the converter to the grid becomes very compact and does not incur any costs [6]. Thanks to these characteristics, in recent years, MMC converters have always been interested in research by scientists.

The main topics researched are the modulation and control algorithms applied to the three-phase MMC converter to generate good quality AC voltage and current. A few modulation and control algorithms have been applied to MMC such as: pulse width modulation (PWM), space vector modulation (SVM), nearest level modulation (NLM), proportional–integral (PI), model predictive control (MPC) [7]–[11]. In which the modulation algorithms aim to solve the problem of generating switching pulse widths for the insulated-gate bipolar transistor (IGBT) valves of the MMC converter, control algorithms in closed-loop circuits aim to improve the quality of the AC current and voltage of the MMC in cases where the current and voltage parameters experience large variations outside the allowable range [12], [13]. NLM modulation has many advantages over PWM modulation because it does not need to use many carriers and the valve switching frequency is low [14]. Compared with the above-mentioned modulation methods, the SVM modulation method has many advantages and can improve the performance when applied to MMC. However, this method is computationally complex and requires the establishment of a voltage vector state table on the output side and must compute a large number of switching states [15]. On the other hand, during the modulation process, the SVM method uses 4 vertices of the parallelogram to calculate the switching state, which increases the number of calculations for the microcontroller and slows down the signal response of the MMC [15].

The problem here is that it is necessary to apply the SVM modulation method but reduce the number of calculations without having to list the state table in detail. Therefore, in this study, the general SVM method for MMC with any number of levels will be proposed to overcome the disadvantages of conventional SVM methods. The process is performed by using the three vertices of the triangle to calculate the IGBT valve switching state. In addition, this method also uses the coefficient k as a factor to create the law to expand the SVM modulation capability with any number of levels when the MMC expands the module to increase the number of levels. This will reduce the IGBT valve switching state and minimize the computational pressure on the microprocessor. Given the control requirements for the MMC, the proposed SVM method has advantages such as it can generate a maximum number of voltage levels of $2N+1$, generate the maximum number of residual states to balance the capacitor voltage, and switching state optimization, can be easily extended to MMC with any number of levels and optimal computing power. The principle of the method is to detect a hexagon with two levels in the large hexagon to select type 1 and type 2 triangles, thereby modulating the voltage vector by the closest vectors in the triangle, detectable without looking up the built-in state table. Compared with previous studies on SVM modulation, this method only performs the state switching process of the valves on 3 vertices of a triangle instead of 4 vertices of a parallelogram like the previous method [15], [16], which means reducing the number of calculations for the microcontroller and making the impact process faster. In addition, this method also creates a rule to create any number of levels when the configuration of the MMC converter is expanded to the corresponding number of levels. This process will save time and effort when implementing specific projects in practice. The obtained results are proved by simulation on MATLAB/Simulink software and experimental model of three-phase MMC converter system based on Verilog programming language and field-programmable gate array (FPGA) microcontroller kit.

The following sections of the paper will clearly present some of the contents of the proposed modulation algorithm and verify the results of the algorithm. Specifically: in section 2, the structure and operating principle of MMC are presented. Section 3 presents the SVM modulation method that can create rules applicable to MMC with any number of levels. Section 4 performs verification of the results on simulation software. Section 5 verifies the algorithm on an experimental model. Finally, the conclusion.

2. PRINCIPLE OF OPERATION AND DESCRIPTION OF THE MMC CONVERTER

Figure 1 describes the three-phase structure of the MMC. Each phase has $2N$ SMs. The SMs in the upper arm are denoted from $SM_{j,1}$ to $SM_{j,N}$ ($j = A, B, C$), the SMs in the lower arm are denoted from $SM_{j,N+1}$ to $SM_{j,2N}$. The DC side of the MMC is connected to a single VDC source with the corresponding i_{DC} current. In each branch of the MMC, there exist upper branch currents denoted $i_{j,H}$ and lower branch currents denoted $i_{j,L}$. The AC side current denoted i_j is drawn at the midpoint of the inductor L_o of the upper and lower arms in each phase. This inductor has the effect of limiting the working transients of the MMC. The losses in each branch of the MMC are described by the resistor R_o [17], [18]. MMC converter works on the principle of VSM voltage accumulation of SMs to generate AC voltage in each phase.

For each SM, the output voltage will be associated with one of two opposite states and is defined as inserted or bypassed based on the switching states of the valves in the direction of the current in the circuit as shown in Figures 2, in which: Figure 2(a) shows the current going in the positive direction, Figure 2(b) shows the current going in the negative direction. For MMC, voltage is distributed across the capacitors of each SM in all valve arms in each phase.

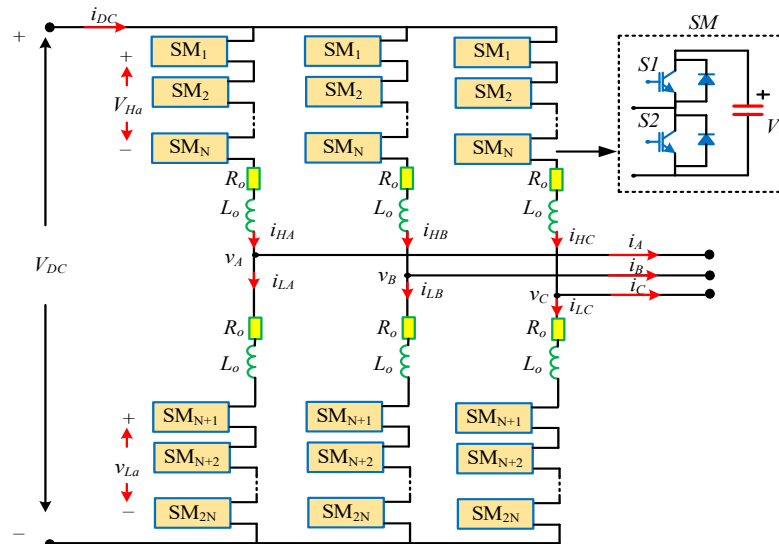


Figure 1. Three-phase structure diagram of MMC converter

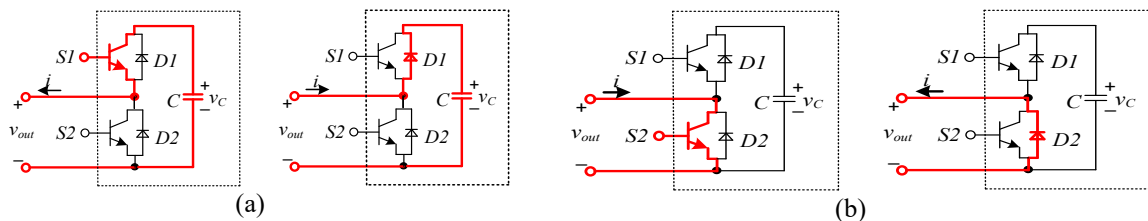


Figure 2. Definition of the inserted and bypassed states for a submodule (SM) based on the switching states of its valves in the current direction: (a) inserted state of SM and (b) bypass state of SM

If the total voltage of the SMs is inserted on each arm is different, the current will be generated from the voltage imbalance across the capacitors. If instantaneous current from the AC connection point flows into the MMC Converter and splits into the upper and lower arms side DC, then the capacitors of each SM inserted in the upper arms will be in the discharge state, in the lower arms will be in the charging state. If the direction of the AC current is in the opposite direction, the discharge and charge states will correspond to the capacitors in the lower and upper arms, respectively. Because of the phase difference between the three AC currents, the discharge and charge states of the capacitors on each phase are continuously changed from phase to phase. Since the total number of SMs inserted in a branch is constant, the total voltage across a branch in one cycle is a value that oscillates at the same frequency as the ac side. However, this value fluctuates asynchronously in the arms of the converter, creating a voltage imbalance between the inserted voltages in each arm, causing current to flow in the arms of the MMC. This current is called the circulating current i_v . The current i_v has no effect on the outside of the MMC on both the AC and DC sides. However, the current i_v is the cause of the loss of the MMC [19], [20]. The inductance on each arm has the role of reducing the effect of current i_v [21], [22]. If the inductance L_o of each arm is large, the amplitude of the circulating current will be small. However, when the value of L_o is large, the response time of the system increases, the converter will not be able to quickly change the current value, so the calculation and selection of the inductance value should match the response of the system [23]. Apply Kirchhoff's law to Figure 1, we have system of (1).

$$\begin{cases} v_{AC} = -v_H - L_o \frac{di_H}{dt} + \frac{1}{2} V_{DC} \\ v_{AC} = v_L + L_o \frac{di_L}{dt} - \frac{1}{2} V_{DC} \\ i = i_L - i_H \\ V_{DC} = v_L + v_H + L_o \frac{d(i_L + i_H)}{dt} \end{cases} \quad (1)$$

From (1) adding the first two equations together, the output voltage is expressed as (2).

$$v_{AC} = \frac{1}{2}(v_L - v_H) + \frac{L_o}{2} \frac{di}{dt} \quad (2)$$

Therefore, the AC electromotive force of the MMC is written as (3).

$$v_{Ace} = \frac{1}{2}(v_L - v_H) \quad (3)$$

If the symbols k_H , k_L are SM numbers in the upper and lower arms are inserted, the corresponding voltage is written as (4).

$$v_H = k_H V_C, v_L = k_L V_C \quad (4)$$

Where $V_C = V_{DC}/N$ is the voltage per step on each capacitor of SM assuming that the voltage across each capacitor is the same. The number of voltage levels on each upper arm and each lower arm is $N+1$. From (3) and (4), the output voltage scale will have the same level as (5).

$$V_{Ce} = \frac{1}{2} V_C = \frac{1}{2} \frac{V_{DC}}{N} \quad (5)$$

Then, the output voltage has the form as (6).

$$v_M = (k_L - k_H) \frac{1}{2} V_C = k_M V_{Ce}; k_M = k_L - k_H \quad (6)$$

To make a voltage level k_M , the corresponding levels of k_H , k_L are calculated according to (7).

$$k_L = \left\lfloor \frac{N+1+k_M}{2} \right\rfloor; k_H = \left\lfloor \frac{N+1-k_M}{2} \right\rfloor \quad (7)$$

3. SVM MODULATION FOR MMC WITH ANY NUMBER OF LEVELS

SVM modulation for MMC can be done by adjusting the output voltage across the load, which is called the modulation voltage. To generate the modulated voltage, the first thing to do is to define the space of operating states of the voltage vector in the coordinate system abc. When MMC has N number of active SMs in each phase, the number of MMC levels will be $M = 2N + 1$ and the reference voltage vector of the MMC is synthesized from the coordinates of the vector space and is expressed by (8).

$$V = \frac{2}{3}(v_A + a \cdot v_B + a^2 \cdot v_C) \quad (8)$$

$$\text{In there: } \begin{cases} v_A = k_A \cdot V_{DC} \\ v_B = k_B \cdot V_{DC}; a = e^{j\frac{2\pi}{3}}; a^2 = e^{j\frac{4\pi}{3}} \\ v_C = k_C \cdot V_{DC} \end{cases} \quad \text{With } k_A, k_B, k_C \in \left\{ -\frac{M-1}{2}, \dots, -1, 0, 1, \dots, \frac{M-1}{2} \right\}$$

Voltage vector representation on the plane $\alpha\beta$:

$$V = v_\alpha + jv_\beta;$$

in there

$$v_\alpha = v_A; v_\beta = \frac{1}{\sqrt{3}}(v_B - v_C) \quad (9)$$

Representing the voltage vector in the coordinate system gh will be the system of (10).

$$\begin{cases} v_\alpha = v_g + \frac{1}{2}v_h \\ v_\beta = \frac{\sqrt{3}}{2}v_h \end{cases} \Rightarrow \begin{cases} v_g = v_\alpha - \frac{1}{\sqrt{3}}v_\beta \\ v_h = \frac{2}{\sqrt{3}}v_\beta \end{cases} \quad (10)$$

The relationship between the coordinate systems is shown by (11).

$$\begin{cases} v_g = v_\alpha - \frac{1}{\sqrt{3}}v_\beta = v_A - \frac{1}{3}(v_B - v_C) = \frac{2}{3}(v_A - v_B) \\ v_h = \frac{2}{\sqrt{3}}v_\beta = \frac{2}{3}(v_B - v_C) \end{cases} \quad (11)$$

From (11) see that:

$$v_A - v_B = V_{DC}(k_A - k_B); v_B - v_C = V_{DC}(k_B - k_C)$$

Therefore

$$v_g = \frac{2}{3}V_{DC}(k_A - k_B); v_h = \frac{2}{3}V_{DC}(k_B - k_C) \quad (12)$$

If $2/3V_{DC}$ is taken as the base length of the state vectors k_A, k_B, k_C as integers, the coordinates of the $[k_g, k_h] = [(k_A - k_B), (k_B - k_C)]$ vectors are integers. Then the vertex coordinates of the vectors will create equilateral triangles with side 1 as shown in Figure 3. Each vector can correspond to different level states, called residual states. For each state vector, a combination of state levels as (13).

$$\begin{bmatrix} k_g \\ k_h \end{bmatrix} \Leftrightarrow \begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix} = \begin{bmatrix} k \\ k - k_g \\ k - k_g - k_h \end{bmatrix} \quad (13)$$

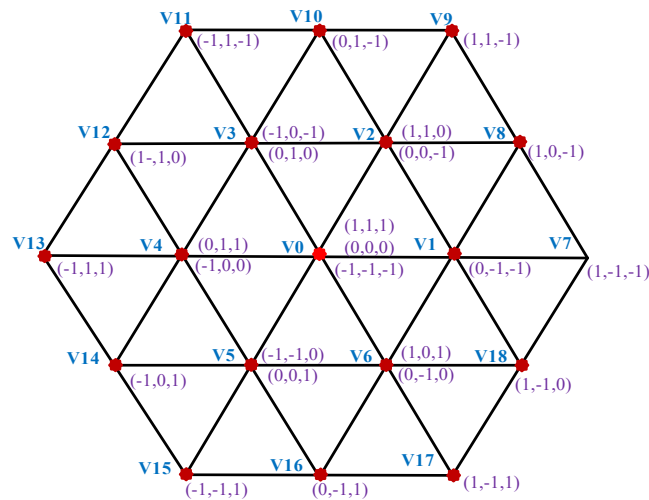


Figure 3. Switching state in vector space of multilevel converter

In the first sixth corner, vectors lying on the outermost hexagon have $k_g + k_h = M-1$, with only one suitable value of $k = (M-1)/2$. In the next hexagon inside $k_g + k_h = M-2$, k has two values: $(M-1)/2-1$ and $(M-1)/2$, meaning that each vector has two residual states. In this way, the zero-vector k will have M values, from $-(M-1)/2$ to $(M-1)/2$, so the zero vector will have M residuals. From this, it is possible to compute all combinations of state vectors in vector space. Determine the modulation factor from the three nearest vectors: The NVM method will generate the desired output vector located in any triangle synthesized from the three vectors that are the vertices of this triangle, which can ensure the best harmonic composition for the output

voltage waveform [6]. The equilateral triangles join together to create an equilateral rhombus, whose sides are parallel to the gh axis, the vertices are the state vectors p_1, p_2, p_3, p_4 , as shown in Figure 4.

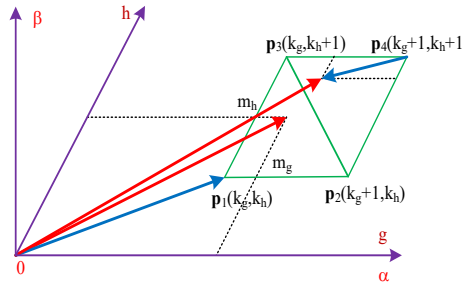


Figure 4. Synthesis of the output voltage vector from the three vertex vectors of the triangle

The desired output voltage vector is also linearly normalized to $2/3 V_{DC}$ and linearly converted to the gh coordinate system according to (14).

$$\begin{bmatrix} v_{rg} \\ v_{rh} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} v_{r\alpha} \\ v_{r\beta} \end{bmatrix} = M_1 \begin{bmatrix} v_{r\alpha} \\ v_{r\beta} \end{bmatrix} \quad (14)$$

where M_1 is the transformation matrix. Let m_g, m_h be the decimal parts apart from the integer part of the coordinates v_{rg}, v_{rh} respectively as (15).

$$\begin{cases} m_g = v_{rg} - \lfloor |v_{rg}| \rfloor = v_{rg} - k_g \\ m_h = v_{rh} - \lfloor |v_{rh}| \rfloor = v_{rh} - k_h \end{cases} \quad (15)$$

where $k_g = \lfloor |v_{rg}| \rfloor, k_h = \lfloor |v_{rh}| \rfloor$ is the smallest integer of the corresponding absolute values. The figure shows that two triangles containing vectors V_1, V_2 have the same integer coordinates $[k_g, k_h]$.

It can be seen that the line $m_g + m_h = 1$ divides the rhombus in Figure 5 into two triangles, where vector V_1 belongs to domain $m_g + m_h \leq 1$ and vector V_2 belongs to domain $m_g + m_h > 1$. V_1 is synthesized from 3 vectors p_1, p_2, p_3 as (16).

$$V_1 = p_1 + m_g(p_2 - p_1) + m_h(p_3 - p_1) = (1 - m_g - m_h)p_1 + m_g p_2 + m_h p_3 \quad (16)$$

V_2 is synthesized from 3 vectors p_2, p_3, p_4 as (17).

$$\begin{aligned} V_2 &= p_4 + (1 - m_g)(p_3 - p_4) + (1 - m_h)(p_2 - p_4) \\ &= (m_g + m_h - 1)p_4 + (1 - m_g)p_3 + (1 - m_h)p_2 \end{aligned} \quad (16)$$

Since the coefficients corresponding to the vectors are all positive and sum to 1, these will be the coefficients for the modulation process. Equations (16), (17) also show that the calculation of the modulation coefficients is very simple, through the calculation of v_{rg}, v_{rh} , the integer parts k_g, k_h and the odd parts m_g, m_h through the (15).

3.1. Locate the vector v in the large sector

When the MMC converter grows with any number of levels M then the number of sub-triangles on the vector plane will increase rapidly. The calculation becomes simpler if we use the symmetry of the space vector system in each of the sixths. Show on the vector plane three coordinate systems of the hexagonal angle $(Z_{1x}, Z_{1y}), (Z_{2x}, Z_{2y}), (Z_{3x}, Z_{3y})$, as shown in Figure 5. First, it is necessary to determine the projection of the desired output voltage vector onto the two boundary vectors of the sixth angle by projecting the coordinates $v_r = [v_{r\alpha}, v_{r\beta}]^T$ onto the corresponding coordinate system Z_1, Z_2, Z_3 . This can be done with transformation matrices of the coordinate system M_1, M_2, M_3 like (18).

$$M_1 = \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix}; M_2 = \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ -1 & \frac{1}{\sqrt{3}} \end{bmatrix}; M_3 = \begin{bmatrix} 0 & \frac{2}{\sqrt{3}} \\ -1 & -\frac{1}{\sqrt{3}} \end{bmatrix} \quad (18)$$

Through an intermediate variable $t_{mp} = v_{\beta}^*/\sqrt{3}$, the remaining components can be immediately defined as (19):

$$\begin{cases} z_{1x} = v_{\alpha}^* - t_{mp} \\ z_{1y} = 2t_{mp} \end{cases}; \begin{cases} z_{2x} = z_{1x} + z_{1y} \\ z_{2y} = -z_{1x} \end{cases}; \begin{cases} z_{3x} = z_{1y} \\ z_{3y} = -z_{2x} \end{cases} \quad (19)$$

After determining the z_{ij} coordinates, the sector determination algorithm is shown in Figure 6.

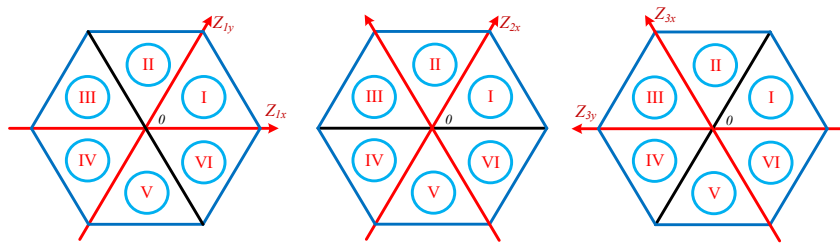


Figure 5. Three non-perpendicular coordinate systems that make up the hexagons (sectors)

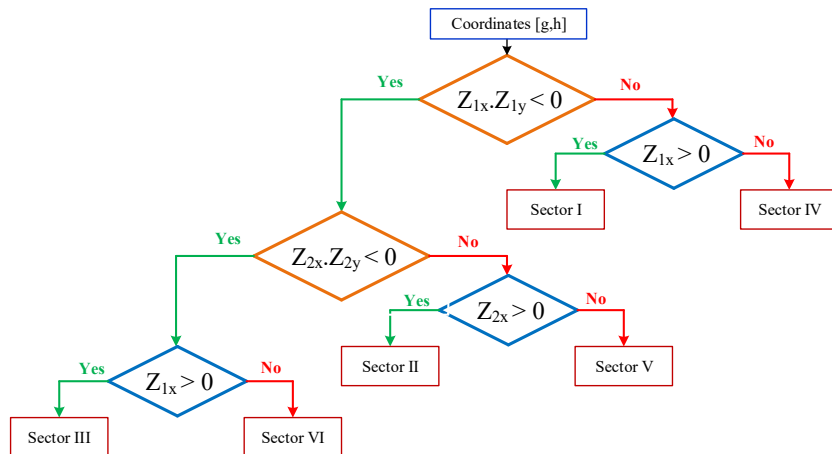


Figure 6. Algorithm to determine large sector

3.2. Determine the state vectors in sectors

3.2.1. Define state vectors at sector I

The sixth angle I, the coordinate system is Z_1 , from (20) we have:

$$\begin{cases} z_{1x} = v_g = \frac{2}{3}V_{DC}(k_A - k_B) \\ z_{1y} = v_h = \frac{2}{3}V_{DC}(k_B - k_C) \end{cases} \text{ Then } \begin{bmatrix} k_{1x} \\ k_{1y} \end{bmatrix} = \begin{bmatrix} (k_A - k_B) \\ (k_B - k_C) \end{bmatrix} \quad (20)$$

If taking the coordinates $k_A = k$ then the word (20) will be obtained on the abc coordinate system, then the state vector coordinates will be:

$$\begin{bmatrix} k_{1x} \\ k_{1y} \end{bmatrix} \Leftrightarrow \begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix} = \begin{bmatrix} k \\ k - k_{1x} \\ k - k_{1x} - k_{1y} \end{bmatrix} \text{ So that: } -\frac{M-1}{2} \leq k, k - k_{1x}, k - k_{1x} - k_{1y} \leq \frac{M-1}{2} \quad (21)$$

3.2.2. Define state vectors at sector II

Second sixth angle, coordinate system is Z_2 , from (19) we have:

$$\begin{cases} z_{2x} = z_{1x} + z_{1y} = \frac{2}{3}V_{DC}(k_A - k_B) \\ z_{2y} = -z_{1x} = \frac{2}{3}V_{DC}(k_B - k_A) \end{cases} \text{Then: } \begin{bmatrix} k_{2x} \\ k_{2y} \end{bmatrix} = \begin{bmatrix} (k_A - k_C) \\ (k_B - k_A) \end{bmatrix} \quad (22)$$

Choose $k_B = k$ to satisfy the condition (21), the remaining coordinates in sector II are determined as (23).

$$\begin{bmatrix} k_{2x} \\ k_{2y} \end{bmatrix} \Leftrightarrow \begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix} = \begin{bmatrix} k - k_{2y} \\ k \\ k - k_{2x} - k_{2y} \end{bmatrix} \quad (23)$$

3.2.3. Define state vectors at sector III

The third sixth angle, the coordinate system is Z_3 , from (19) we have:

$$\begin{cases} z_{3x} = z_{1y} = \frac{2}{3}(v_B - v_C) \\ z_{3y} = -z_{2x} = \frac{2}{3}(v_C - v_A) \end{cases} \text{Then } \begin{bmatrix} k_{3x} \\ k_{3y} \end{bmatrix} = \begin{bmatrix} (k_B - k_C) \\ (k_C - k_A) \end{bmatrix} \quad (24)$$

Choose $k_C = k$ to satisfy the condition (21), the remaining coordinates in sector III are determined as (25).

$$\begin{bmatrix} k_{3x} \\ k_{3y} \end{bmatrix} \Leftrightarrow \begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix} = \begin{bmatrix} k - k_{3y} - k_{3x} \\ k \\ k - k_{3x} \end{bmatrix} \quad (25)$$

Since the space vectors are symmetrical, it is obvious that sector IV is symmetrical with sector I. Sector V is symmetrical with sector II. Sector VI is symmetrical with sector III. Therefore, the way to determine the state vectors is done similarly.

3.3. Optimal order for number of switches

When space vector modulation for a two-level inverter, Symmetrical triangle modulation uses only two edge vectors and zero vectors, such that the time using the zero-vector divided equally into two parts, At the beginning and end of each modulation half cycle, in the other half the order of vector execution is reversed. This will optimize the harmonic component on the output voltage [24]. This modulation is called SVM modulation with active vectors placed between each half-cycle of the modulation. This method is equivalent to SPWM by inserting a zero-order component, as follows [25].

$$V_{off} = -\frac{\max(V_{a,ref}, V_{b,ref}, V_{c,ref}) + \min(V_{a,ref}, V_{b,ref}, V_{c,ref})}{2} \quad (26)$$

In there $V_{a,ref}$, $V_{b,ref}$, $V_{c,ref}$ are the desired sinusoidal settings, V_{off} is the zero-order component added to the settings. The modulated signals will have the form as (27).

$$V'_{k,ref} = V_{k,ref} + V_{off}, k = a, b, c. \quad (27)$$

The SPWWM modulation and switching process in SVM modulation is shown in Figure 7. The signal at the PWM output through the comparator with the sawtooth voltage in one modulation cycle is shown in Figure 7(a). The addition of the zero-order component like (26) is to determine the zero vector at the beginning of the modulation cycle. However, in a multi-level inverter it is not possible to have a zero vector to arrange the signals as shown in Figure 7(a). Instead, if a modulation method is used with the three nearest vectors in each modulation half-cycle, one vector will be used as vector zero, *i.e.* the time spent using this vector is divided into two equal halves, equally divided for the beginning of the half cycle T_s and the end of the half cycle T_s . To apply the same two-level inverter to a multi-level inverter, it can be imagined that the spatial vector of a multi-level inverter has as many small hexagons as that of a two-level inverter, and the vector at the center of this small hexagon has role as zero vector. Consider specifically when the voltage vector moves from triangle 2 to triangle 3 as shown in Figure 7(b).

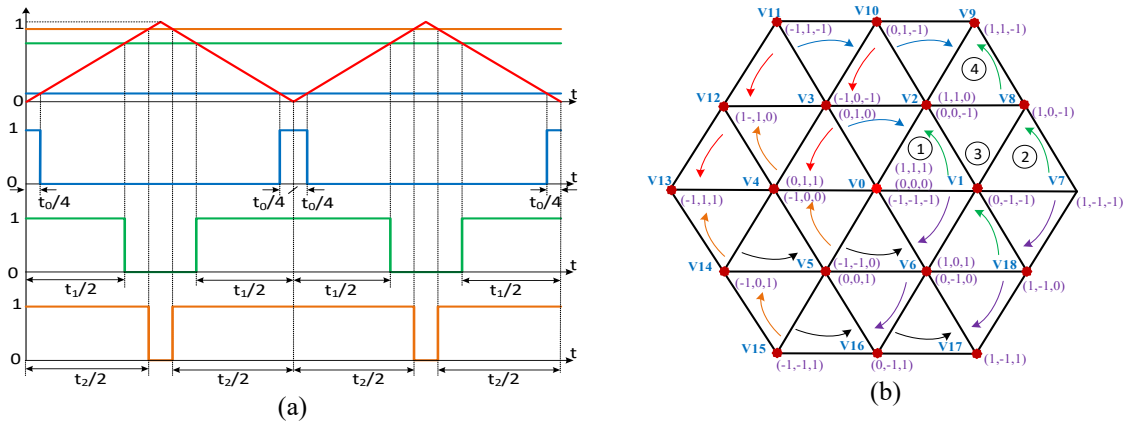


Figure 7. The SPWWM modulation and switching process in SVM modulation: (a) PWM output signal and times using positive and zero vectors and (b) optimal switching order for three-phase 3-level inverters

4. SIMULATION RESULTS

In this section, the author will present simulation results when performing SVM modulation for an MMC converter consisting of 12 SMs per phase. The simulation parameters are presented in Table 1. The output parameters of the AC side of the MMC converter are shown in Figure 8. Figures 8(a) and (b) are the results of phase voltage and current on phases A, B, C of the MMC converter when applying the SVM modulation method with the selection of the nearest voltage vector. The picture shows current voltage without going through the filter gives normal sinusoidal results, which are obtained in the first cycle and no transients occur during the simulation. Performing evaluation of total harmonic distortion THD for voltage and current as shown in Figure 9, the results Figures 9(a) and 9(b) show that the THD index of current and voltage is very small. Specifically, the THD index of the output voltage in the period 0.02 to 0.08 s is 1.85%, the THD index of the current on the load is 1.01%. This result shows that the power quality corresponding to the proposed SVM modulation algorithm is guaranteed as required, with the results of the THD index showing that this method can be used for MMC to connect directly to the grid to transmit power to the grid without the need for voltage filters and without the need for transformers. This is very important to reduce equipment costs, reduce investment costs for the project while still ensuring technical conditions according to regulations.

Table 1. MMC parameters used for simulation

Parameter	Symbol	Value
Voltage of DC power supply	V_{DC}	6000 V
Capacitor voltage	V_C	1000 V
Arm inductance	L_o	5 mH
Capacitance of the capacitor SM	C_{SM}	3000 μ F
Number of SMs per phase	$2N$	12
Frequency	f	50 Hz

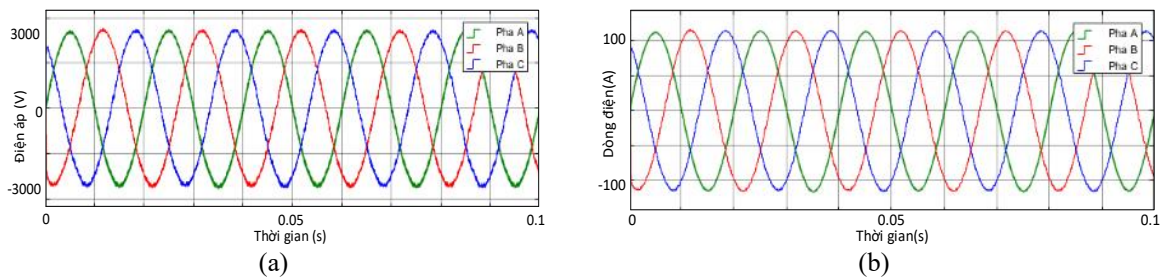


Figure 8. The output parameters of the AC side of the MMC converter: (a) phase voltage on the AC side of the MMC converter and (b) current on the AC side of the MMC converter

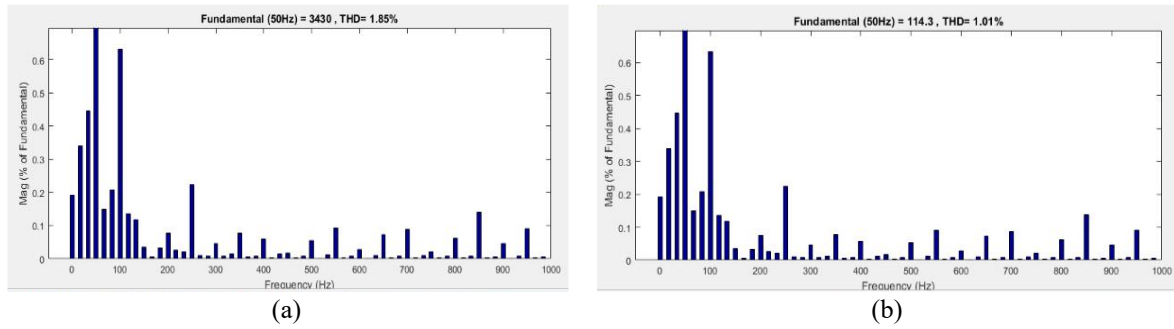


Figure 9. Performing evaluation of total harmonic distortion THD for voltage and current: (a) THD index for AC voltage and (b) THD index for AC load current

These results prove that the switching optimization process of the method is guaranteed to be in accordance with the set objectives and always ensures the operation quality of the MMC converter when applying the proposed SVM modulation algorithm. Based on the comparison of voltage and current THD indexes of PWM methods when applied to MMC converters with corresponding number of levels in the document [16], we find that the THD index of the proposed method in this paper is always lower in value. The details are shown in Table 2.

Table 2. Comparison of THD of voltage between modulation methods

Modulation method	THD index for voltage
PSC-PWM	8.25%
NLC	17.2%
NLC+PWM	9.7%
NLC+CRC	17.6%

Figure 10 is the voltage of capacitors in phase A. Figures 10(a) and 10(b) are the capacitor voltages of the SM of the upper and lower arms on phase A. Observing the capacitor voltage values of SMs of the upper and lower arms of phase A shows that the MMC converter capacitor voltage always fluctuates around the equilibrium position of 1000 V, the maximum fluctuation value of the capacitor voltage when reaching the equilibrium position is 25 V, *i.e.* 2.5%. This result will help the capacitor operate stably for a long time to help increase the life of the MMC and improve the performance of the MMC.

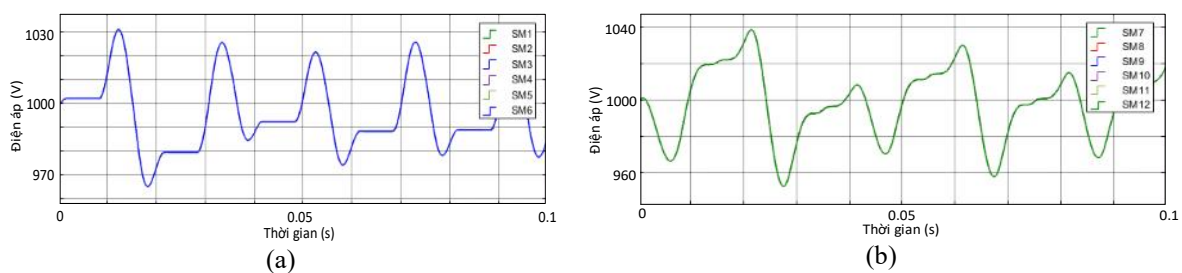


Figure 10. The voltage of capacitors in phase A: (a) voltage of upper and lower arm capacitors in phase A and (b) voltage of the lower arm capacitors in phase A

5. EXPERIMENTAL SYSTEM AND RESULTS

5.1. Structure of the experimental system of the MMC converter

The experimental model of the MMC system is presented in Figure 11. The experimental system is built based on the structure of the MMC converter with 12 SMs per phase and is described by the structural diagram as shown in Figure 11(a).

In which: MMC converter is the main structure to convert energy from DC to AC according to the proposed SVM algorithm; The measurement block is responsible for measuring, collecting, and extracting samples of signals from the MMC controller to serve the signal processing system; With the characteristics of

the MMC converter, which has a large number of measured signals to implement the control algorithm, it requires a microprocessor device with many inputs/outputs and fast action [26]. Therefore, in this article, the author used Xilinx FPGA AX306 Kit as the main tool for the controller. The reason for choosing this device is because of its fast signal processing speed, which can accommodate many I/O ports for controlling IGBT valves. of the MMC converter, and at the same time can create programmable logic circuits that cannot be implemented by other microcontroller devices. Therefore, the SVM modulation algorithm, pulse generation, sine wave generation, and calculation process are all done in this device. The working sequence of programming on the FPGA is shown in Figure 12.

First, a signal needs to be generated to start and synchronize all the signals on the FPGA (here selected as the reset signal, this signal is assigned to the reset key on the FPGA). Then, conduct communication between the FPGA and the Mcp3208 to read the required values from the MMC in turn. Simultaneously generate a 3-phase sine wave, placed at an angle of 120 degrees from the DDS core on the FPGA. After reading all the voltage and capacitor values on the phases, we create a start signal to arrange the voltage value of the capacitors on the corresponding phase branch based on the capacitor voltage balancing algorithm, at the same time determine the number of SMs inserted on that branch according to the SVM algorithm and generate the corresponding pulse to the MMC converter. The overall diagram of the experimental system of MMCs with 6SMs on each branch is presented as shown in Figure 11(b).

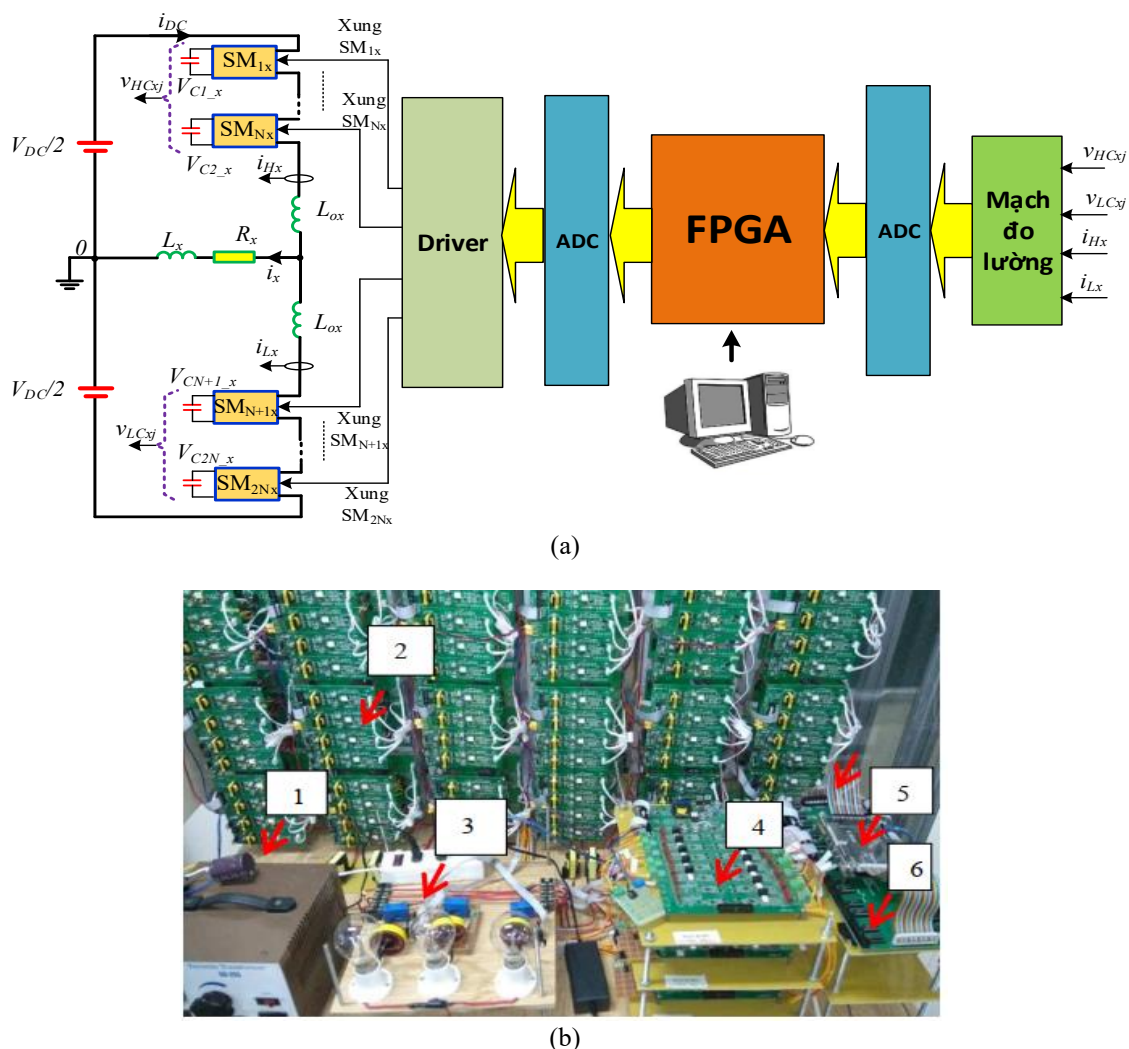


Figure 11. The experimental model of the MMC system: (a) structure diagram of single-phase experimental system of MMC and (b) overall model of the experimental system of the MMC converter (1) driver, (2) V_{DC} , (3) load, (4) measure circuit, (5) FPGA, (6) ADC

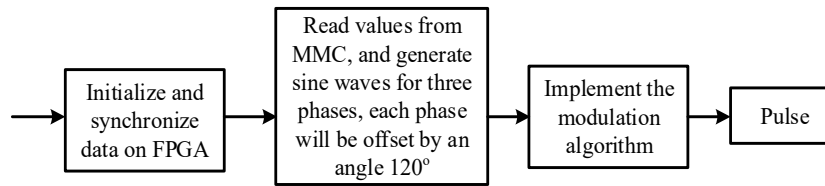


Figure 12. Sequence diagram for programming on FPGA

The main equipment of the experimental system:

- Power circuit: including 72 semiconductor valves type IGBT SKM50GB063D 600V/50A type; 36 capacitors, 72 diodes, a 400VDC DC voltage source, AC side RL loads, a number of circuit protection components.
- Measuring circuit: current measuring circuit using 9 current measuring sensors type LEM LA55-P, of which 6 LEMs are used to measure the current on each arm, the remaining 3 LEMs are used to measure the current on the AC load. Voltage measuring circuit includes 36 INA128 and 36 HCPL-7800 to measure capacitor voltage, amplify signal, and convert to control signal.
- The ADC circuit uses 36 MCP3208 with 16 pins responsible for converting analog signals to digital signals for input into the microprocessor and vice versa.
- Driver circuit: using a series of IRF21531 components to generate AC voltage through a pulse transformer and a diode bridge rectifier circuit to generate voltages of 15V and -5V. The PWM signals from the ADC circuit are fed into the HCPL316J ICs. IC HCPL 316J has the function of generating pulses to control the IGBT valve.

+The Xilinx FPGA AX309 80-pin I/O microprocessor is responsible for processing the ADC measurement signal, implementing the SVM modulation algorithm that has been output. The signals are taken as a digital signal and converted to an analog signal when pulses are applied to the valves of the MMC.

Experimental results in Figure 13 when implementing the SVM modulation method show that the MMC converter works well with the SVM modulation principle. Specific: Figure 13(a) is the output AC voltage of phases A, B, and C. The results show that the phase voltages have a sinusoidal shape with 13 levels, which is consistent with the principle of generating $2N+1$ voltage levels of the SVM modulation algorithm (here $N = 6$). This result has proven the correctness of the rule for selecting the coefficient k according to the proposed SVM modulation algorithm, and at the same time proves the accuracy of the SVM modulation process for MMC according to the experiment compared with the simulation results obtained. The output current on the load phases A, B, C shown in Figure 13(b) has a sinusoidal form, the working process is stable without any transients, this has met the necessary requirements of the MMC converter when operating in DC/AC mode. The current results have demonstrated the power quality of MMC when applying the proposed SVM modulation algorithm when implemented with FPGA 309AX microprocessor.

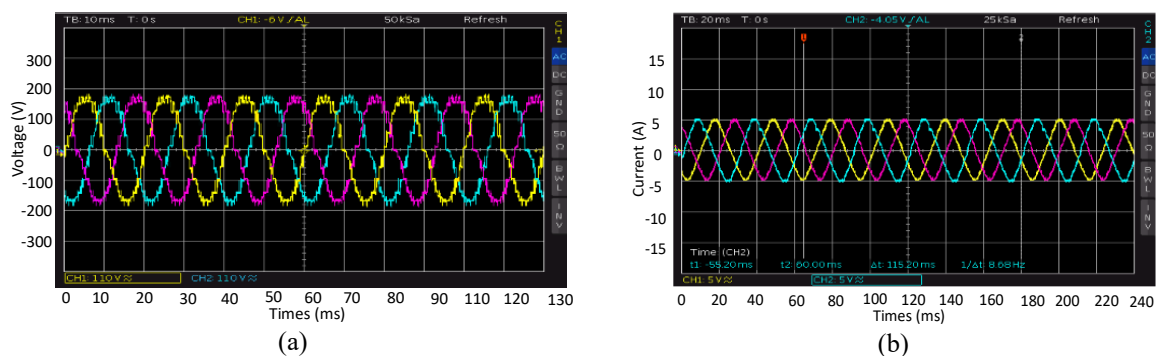


Figure 13. Experimental results (a) output AC voltage shape of phase A, B, C and (b) current shape on AC load of phase A, B, C

Figure 14 shows the capacitor voltage results in SM1 of phases A, B, C. The image shows that the oscillation amplitude of the capacitor is 9 V. With the rated value of the capacitor according to the experimental scenario of 67 V, the corresponding oscillation level of the capacitor is 13%. For the normal

operation of the MMC, this value is small and acceptable so that the capacitor can operate for a long time as desired. The results of the capacitor voltage have demonstrated that the SVM method has met the requirement of balancing the voltage in the capacitors of the SM on all three phases, which will help the MMC converter to operate stably for a long time with the proposed method.

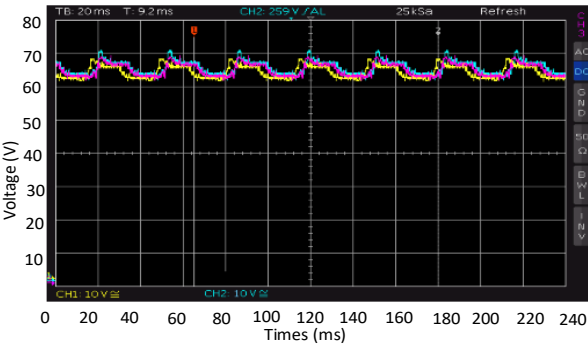


Figure 14. Voltage shape on the capacitor of SM1 phase A, B, C

6. CONCLUSION

The paper has implemented an improved space vector modulation law for multilevel MMC with any number of levels. The new modulation law is implemented by choosing the voltage vector in any triangle of the vector space, in this way the switching law will be shortened and simplified. The results are to create an optimal switching law and can be extended when necessary. This work will make a new contribution to improving the efficiency and quality of operation for MMC. The paper has performed simulations for MMC converters with 12 SMs in one phase. When using the proposed law, the principle of the proposed method has been proven to be correct and creates 2N+1 voltage levels, minimizing voltage fluctuations on capacitors. From the simulation results, the author has demonstrated on the corresponding experimental model that the experimental results are similar to the simulation results. This is the basis for developing practical applications of MMC converters.

FUNDING INFORMATION

This research is funded by Hanoi University of Science and Technology (HUST) under project number T2023-PC-025.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Tran Hung Cuong	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓		
Pham Chi Hieu			✓	✓			✓	✓		✓				
Pham Viet Phuong		✓		✓		✓	✓	✓			✓	✓	✓	✓

C : Conceptualization	I : Investigation	Vi : Visualization
M : Methodology	R : Resources	Su : Supervision
So : Software	D : Data Curation	P : Project administration
Va : Validation	O : Writing - Original Draft	Fu : Funding acquisition
Fo : Formal analysis	E : Writing - Review & Editing	

CONFLICT OF INTEREST STATEMENT

The authors certify that they have no known financial or personal interests that could be interpreted as influencing or compromising the integrity of the work presented in this paper.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, PVP, upon reasonable request.

REFERENCES

- [1] Z. Jiang, N. Beniwal, S. Ceballos, J. Pou, H. D. Tafti, and G. G. Farivar, "Analysis of the average neutral-point current limits of the neutral-point-clamped converter under three-level modulation," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2020, pp. 4079–4084. doi: 10.1109/iecon43393.2020.9255382.
- [2] M. Tayari, A. Guermazi, and M. Ghariani, "Cascaded H-bridge inverter for an application of active filtering in electric vehicles," in *2015 16th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)*, Dec. 2015, pp. 540–544. doi: 10.1109/sta.2015.7505132.
- [3] V. Eslampanah, R. Ebrahimi, M. Azizian, and H. M. Kojabadi, "Artificial neural networks for control of three phase grid connected T-type inverter," in *2020 28th Iranian Conference on Electrical Engineering (ICEE)*, Aug. 2020, pp. 1–6. doi: 10.1109/icee50131.2020.9260655.
- [4] J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5063–5073, Nov. 2013, doi: 10.1109/TPEL.2013.2243758.
- [5] Y. Tian, H. R. Wickramasinghe, Z. Li, J. Pou, and G. Konstantinou, "Review, classification and loss comparison of modular multilevel converter submodules for HVDC applications," *Energies*, vol. 15, no. 6, p. 1985, Mar. 2022, doi: 10.3390/en15061985.
- [6] S. Coffey, V. Timmers, R. Li, G. Wu, and A. Egea-Álvarez, "Review of MVDC applications, technologies, and future prospects," *Energies*, vol. 14, no. 24, p. 8294, Dec. 2021, doi: 10.3390/en14248294.
- [7] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electronics*, vol. 6, no. 1, pp. 96–107, Jan. 2013, doi: 10.1049/iet-pel.2012.0228.
- [8] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2734–2745, May 2016, doi: 10.1109/tie.2016.2514346.
- [9] L. K. Ramasamy, S. Kadry, Y. Nam, and M. N. Meqdad, "Performance analysis of sentiments in Twitter dataset using SVM models," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 11, no. 3, p. 2275, Jun. 2021, doi: 10.11591/ijece.v11i3.pp2275-2284.
- [10] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836–1842, Apr. 2015, doi: 10.1109/TPEL.2014.2325875.
- [11] S. Isik, M. Alharbi, and S. Bhattacharya, "An optimized circulating current control method based on PR and PI controller for MMC applications," *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 5074–5085, Sep. 2021, doi: 10.1109/tia.2021.3092298.
- [12] J. Freytes, F. Gruson, F. Colas, P. Rault, H. Saad, and X. Guillaud, "Simplified model of droop-controlled MTDC grid-influence of MMC energy management on DC system dynamics," in *2018 Power Systems Computation Conference (PSCC)*, Jun. 2018, pp. 1–7. doi: 10.23919/pssc.2018.8442751.
- [13] H. B. Gobburi, V. B. Borghate, and P. M. Meshram, "A level enhanced nearest level control for modular multilevel converter without using sensors," *IEEE Transactions on Industry Applications*, vol. 59, no. 4, pp. 4364–4374, Jul. 2023, doi: 10.1109/tia.2023.3270113.
- [14] J. Xu, M. Odavic, Z.-Q. Zhu, Z.-Y. Wu, and N. Freire, "A novel space vector PWM technique with duty cycle optimization through zero vectors for dual three-phase PMSM," *IEEE Transactions on Energy Conversion*, vol. 37, no. 4, pp. 2271–2284, Dec. 2022, doi: 10.1109/tec.2022.3171705.
- [15] W. Wang, Q. Xiao, H. Liu, Y. Jin, Y. Mu, and H. Jia, "Simplified carrier-based space vector modulation scheme for the modular multilevel converter," in *2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, Oct. 2022, pp. 1–6. doi: 10.1109/itecasia-pacific56316.2022.9942165.
- [16] M. Rejas *et al.*, "Performance comparison of phase shifted PWM and sorting method for modular multilevel converters," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–10. doi: 10.1109/epe.2015.7311700.
- [17] S. Thakur, M. Odavic, A. Allu, Z. Q. Zhu, and K. Atallah, "Analytical modelling and optimization of output voltage harmonic spectra of full-bridge modular multilevel converters in boost mode," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3403–3420, 2022, doi: 10.1109/TPEL.2021.3108877.
- [18] X. Xi, X. Gao, W. Huang, S. Li, Y. Zhao, and C. Lv, "Application analysis of resistor superconducting fault current limiter in MMC-HVDC system," in *2019 IEEE Sustainable Power and Energy Conference (iSPEC)*, Nov. 2019, pp. 2260–2264. doi: 10.1109/ispec48194.2019.8974866.
- [19] Z. Yang, P. Song, J. Song, X. Wang, and X. Li, "An MMC circulating current suppressing controller based on bridge arm common-mode voltage," *IEEE Access*, vol. 8, pp. 189471–189478, 2020, doi: 10.1109/access.2020.3031307.
- [20] S. Isik, M. Alharbi, and S. Bhattacharya, "Optimized circulating current control method based on proportional resonant and proportional integral controllers for modular multi-level converter applications," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2020, pp. 5709–5715. doi: 10.1109/ecce44975.2020.9235884.
- [21] M. Alharbi, S. Isik, and S. Bhattacharya, "Control of circulating current to minimize the rating of the energy storage device in modular multilevel converters," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 6041–6045. doi: 10.1109/ECCE.2019.8912773.
- [22] W.-S. Do, S.-H. Kim, T.-J. Kim, and R.-Y. Kim, "A study of circulating current in MMC based HVDC system under an unbalanced grid condition," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2014, pp. 4146–4152. doi: 10.1109/iecon.2014.7049125.
- [23] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and experiment on an optimal carrier frequency of a modular multilevel cascade converter with phase-shifted PWM," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3456–3471, May 2016, doi: 10.1109/tpe.2015.2464694.
- [24] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1873–1886, Mar. 2016, doi: 10.1109/tpe.2015.2429595.
- [25] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003, doi: 10.1109/tpe.2003.818827.

BIOGRAPHIES OF AUTHORS

Tran Hung Cuong    received his engineer (2010). M.Sc. (2013) degrees in industrial automation engineering from Hanoi University of Science and Technology and completed Ph.D. degree in 2020 from Hanoi University of Science (HUST). Now, he is a lecturer of Faculty of Electrical and Electronic Engineering under Thuylai University s (TLU). His current interests include power electronic converters, electric motor drive, convert electricity from renewable energy sources to the grid, and saving energy solutions applied for grid and transportation. He can be contacted at email: cuongth@tlu.edu.vn.



Pham Chi Hieu    received the B.Sc. degrees in control and automation engineering from Hanoi University of Science and Technology, Hanoi, Vietnam, in 2024. He is currently studying M.Sc. in control and automation engineering in Hanoi University of Science and Technology, Hanoi, Vietnam. His research interests consist of large-capacity power electronics converters and application of power electronics for power systems. He can be contacted at email: chihieu.hust@gmail.com.



Pham Viet Phuong    was born in Hanoi, Vietnam, on December 24th, 1980. He received the B.S. degree in Industrial Automation from Hanoi University of Science and Technology, Hanoi, Vietnam, in 2003, the M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2006 and 2009, respectively. Since 2004, he has been a lecturer at the Department of Automation Engineering, School of Electrical and Electronic Engineering, Hanoi University of Science and Technology. His research interests consist of large-capacity power electronics converters, application of power electronics for power systems, and high-power ac motor drives. Email: phuong.phamviet@hust.edu.vn.