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FinFET technology: a comprehensive review on materials, structures, fabrication, and device performance

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ABSTRACT

As semiconductor devices become smaller, FinFETs have replaced traditional planar MOSFETs. Planar devices face issues like weak electrostatic control and high leakage current at small sizes. FinFETs solve these problems with a three-dimensional structure and multigate design. This improves gate control and reduces short-channel effects. This paper explains FinFET design, materials, and fabrication methods. It highlights how fin geometry affects current flow and device performance. Gate-source voltage (VGS) and drain-source voltage (VDS) are important parameters. These control the device operation in the lin-ear, saturation, and pinch-off regions. Performance factors such as on/off current ratio *(I_{ON} /I_{OFF})*, subthreshold swing (SS), and drain-induced barrier lowering (DIBL) show that FinFETs work well for low-power and high-speed uses. Achieving uniform doping below 5 nm remains difficult. Atomic layer deposition (ALD) helps improve doping control. In summary, FinFETs play a key role in modern semiconductor design by improving scalability and efficiency.

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1. INTRODUCTION

The semiconductor industry is moving toward faster, smaller, and more energy-efficient integrated circuits. This progress follows Moore's law, which predicts that the transistor count on very-large-scale integration (VLSI) chips doubles about every two years as transistor size decreases as shown in Figure 1. As scaling continues, traditional MOSFETs face major drawbacks like higher leakage currents and stronger short-channel effects. Leakage becomes significant below the 14 nm technology node, increasing by about 30 percent when scaled under 10 nm [1]. Device performance also degrades as the node size shrinks [2]. FinFETs yield improved scalability, better electrostatic control and lower leakage, making them suitable for high-performance circuits [3].

This review connects FinFET materials, gate stacks, spacer design, device geometry, and fabrication flows to measurable figures of merit, including I_{ON} /I_{OF} F, subthreshold swing, drain-induced barrier lowering, variability, and electrothermal limits, and it provides a normalized comparison to bulk complementary metal oxide semiconductor (CMOS) so that the operating regions where FinFETs lead or lag are explicit for measurement and control applications. To do this, we followed a structured narrative approach, curating recent peer-reviewed articles from reputable journals lectin studies with explicit device

context, geometry, bias, and target metrics, extracting reported and plot-read values, and comparing FinFET and bulk CMOS under matched bias and contacted gate pitch.

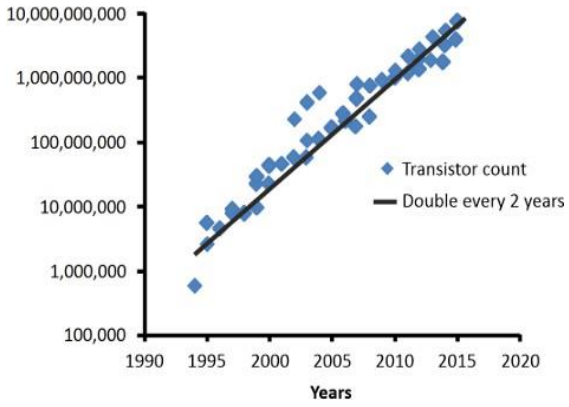

Figure 1. Last 30 years chronological depiction of Moore's Law, demonstrating the transistor count on VLSI chips doubling approximately every two years as transistor dimensions continually shrink. Adapted from Petrosyants *et al.* [4]

At nanoscale dimensions, FinFETs use a 3D gate that cloaks a narrow fin made of silicon reducing short-channel effects [5]. FinFETs supply higher drive current while keeping leakage low making them suitable for both low-power and high-performance devices. Careful design of the source-drain extension (SDE) region, improves cutoff frequency intrinsic gain. The spacer width and lateral straggle design optimizations make FinFETs effective for ultra-low-voltage analog applications [6].

Many multi-gate transistor structures have been developed to reduce short-channel effects and gain better electrostatic control, but they are harder to fabricate than standard planar or silicon-on-insulator (SOI) devices [7]. Examples include double-gate FinFETs, tri-gate FinFETs, and gate-all-around (GAA) nanowire MOSFETs. Advanced types such as GAA nanosheet and GAA nanowire FETs offer better gate control and scaling; nanosheet FETs use stacked horizontal channels, while nanowire FETs use cylindrical gates that fully surround the channel, improving electrostatic integrity and scalability. A key limitation of standard MOSFETs is the subthreshold swing (SS), which is limited to 60 mV/decade [8]. To overcome this, ferroelectric field-effect transistors (Fe-FETs) use negative capacitance (NC) from a ferroelectric (FE) layer added to the gate oxide stack. This approach allows Fe-FETs to achieve a sub-60 mV/decade SS, improving power efficiency and increasing the I_{ON} /I_{OF} F ratio [8].

Modern semiconductor manufacturing companies such as Apple, Intel, AMD, TSMC, NVIDIA, and Samsung use FinFETs in chips, advanced processors, graphics units, and memory devices. These manufacturers have successfully applied FinFETs in nodes at 7 nm and below [9]. Recent improvements in fin shape and material selection have enhanced electrostatic control and subthreshold performance, making FinFETs effective for ultra-low-voltage applications [10]. However, scaling below the 5 nm node introduces new challenges, leading the industry to explore advanced architectures such as nanosheet transistors and gate-all-around FETs (GAAFETs) [11], [12]. These reviews list major process and device developments but also highlight remaining issues in variability, integration, and electrothermal behavior that are not consistently compared under the same bias, geometry, or pitch conditions. The connection between fabrication factors—such as atomic-layer-deposited high-k gate stacks, inner and outer spacer design, and fin or sheet shape—and device-level performance like electrostatics and thermal stability is still not well established [13], [14].

The goal of this review is to study how FinFET materials, gate stacks, spacer design, device geometry, and fabrication steps affect key performance parameters, including I_{ON} / $I_{OF\ F}$, subthreshold swing (SS), drain-induced barrier lowering (DIBL), threshold voltage (V_{th}), and electro-thermal behavior. It also aims to provide a normalized comparison with bulk CMOS under similar bias and pitch conditions to identify where FinFETs perform better or worse. The analysis also provides fabrication-based guidance for measurement and device control. This study also includes a review of logic MOSFET structures to show how transistor designs have evolved over time to follow Moore's law 1. Figure 2 illustrates how each new transistor generation has improved the ratio of drive current (I_{ON}) to leakage current (I_{OF} F), supporting the ongoing trend of device scaling. The major contributions of this research include but not limited to:

a. Thermal behavior.
b. It defines a normalized comparison framework against bulk CMOS under matched bias and contacted-gate-pitch to enable fair, reproducible benchmarking.
c. It quantifies FinFET versus bulk CMOS performance across I-V behavior, $I_{ON}/I_{OF\ F}$ versus V_{DD}, DIBL, SS, V_{th}, and temperature dependence using the conditions reported in the sources.
d. It converts these results into process aware guidance by linking specific fabrication levers to metric shifts and by identifying operating regions where FinFETs lead or lag.

In this paper, section 2 presents the detailed review methods approach, section 3 reviews FinFET structure and design considerations, Section 4 describes materials, deposition techniques, and fabrication including ALD, bulk-Si flow, and SOI device specifications, section 5 presents operation and performance metrics, section 6 reports the results and discussions, and section 7 provides the conclusions.

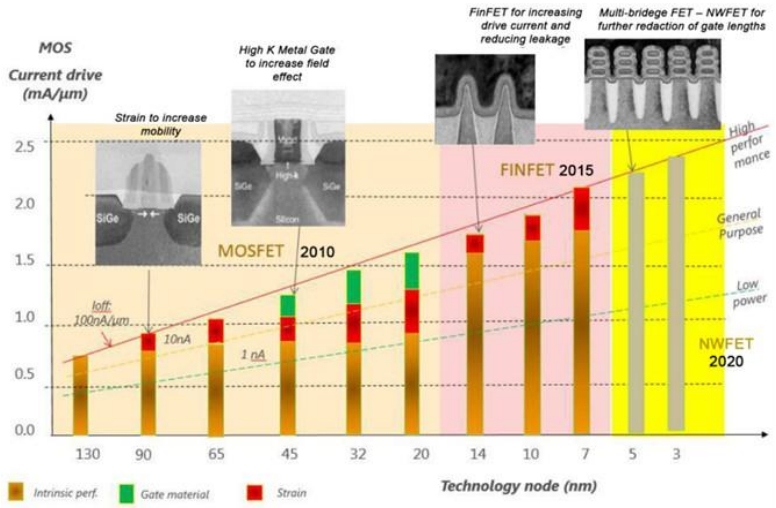

Figure 2. Retrospective review of MOSFET structure scaling, illustrating a consistent increase in the ratio of drive current (I_{ON}) to leakage current (I_{OFF}) with each successive transistor generation. Adapted from Petrosyants *et al.* [4]

2. METHOD

This paper follows a structured narrative review approach. It studies recent progress in FinFET technology. The focus is on materials, structures, fabrication steps, and device performance. The goal is to summarize and explain the main findings from previous research. Journal articles and conference papers were collected from reliable databases. These include IEEE Xplore, ScienceDirect, SpringerLink, and MDPI. The search covered studies published between 2015 and 2025. The selected papers discussed FinFET materials, fabrication methods, and device modeling. Studies that reported key parameters such as subthreshold swing (SS), drain-induced barrier lowering (DIBL), and on/off current ratio (I_{ON}/I_{OF} F) were included. About 150 papers were checked, and 70–80 of the most relevant were used for this review.

The information from these papers was organized and compared. Data trends were studied based on fin size, gate length, dielectric materials, and channel design. The results helped to understand how these factors affect device control and leakage. Figures showing simulation and fabrication setups, such as oxide-isolated Bulk-Si FinFETs and 3-Fin SOI FinFETs, were taken or redrawn from existing studies. These help make the process clear and reproducible. All figures and schematics were properly cited. This paper does not include new experiments. It does not involve any living subjects. Therefore, no ethical approval was needed. The findings come only from trusted and published research to ensure honesty and accuracy.

3. DESIGN AND STRUCTURAL CHARACTERISTICS OF FINFETS

In the three-dimensional FinFET structure, the fin-shaped semiconductor channel rises above the substrate and is covered by the gate on three sides. The main parts of a FinFET are the fin-shaped channel, source/drain contacts, and gate dielectric.

a. Fin Geometry: Fin is the gateway for the drain and source current. A thinner fin reduces short-channel effects and improves electrostatic control. A taller fin increases the drive current [15]. Figure 3 shows

that DC performance depends on both fin width and channel length. Shortening the channel length boosts efficiency but increases the risk of isolation and short-channel issues at 7 nm.

b. Gate: In FinFETs, the gate wraps around three sides of the fin. This structure gives stronger control of the channel compared to planar transistors. The tri-gate design allows better modulation of the channel, reducing leakage current and increasing drive current. Depending on the design, the gate can be tri-gate, double-gate, or single-gate, based on how many sides it covers.
c. Parasitics: Parasitic resistance and capacitance in FinFETs depend on the fin geometry. Variations in fin height, fin width, and gate spacing affect these parasitic elements. High parasitics can lower performance, especially in advanced nodes. Proper optimization of these dimensions helps reduce parasitic effects, improving speed, power efficiency, and high-frequency performance.
d. Fin Spacing and Layout Density: Transistor performance and integration density are affected by 'fin pitch'. It is the distance between fins. Smaller spacing allows more fins per chip, increasing device density. However, it can also raise parasitic capacitance, which lowers efficiency. Balancing fin spacing and parasitic control is important for FinFET design. At very small nodes, such as 15 nm, junction-based isolation becomes less effective. To prevent leakage, a dielectric layer is often added below the channel for better isolation and stable operation.

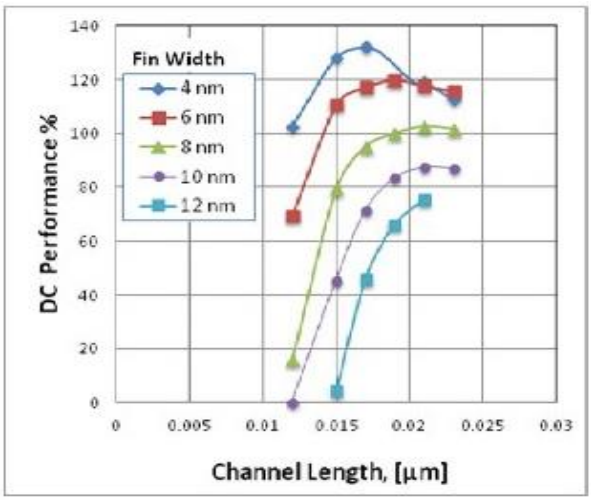

Figure 3. Drive current variation with length of the gate and width of the fin in bulk Silicon FETs. Adapted from Maszara *et al.* [16]

FinFETs are mainly available in two types: SOI and bulk. Bulk FETs are fabricated directly on a substrate made of silicon [17]. At smaller nodes, bulk FinFETs can face substrate coupling and higher parasitic capacitance [1]. SOI FinFETs, on the other hand, have a thin silicon layer over oxide layer insulation, usually silicon dioxide. The insulation lowers leakage current and parasitic effects. It also improves power efficiency and supports faster operation. The extra thermal isolation in SOI FinFETs makes them suitable for high-performance and low power designs at advanced nodes.

Many multi-gate transistor designs have been created to improve electrostatic control and reduce short-channel effects. However, these designs are more complex to fabricate than planar or SOI technologies [18]. Common multi-gate types include double-gate FinFETs, tri-gate FinFETs, and gate-all-around (GAA) nanowire MOSFETs. Figure 4 shows two advanced multi-gate structures: i) GAA nanosheet FETs, which use stacked horizontal channels to improve electrostatic control, and ii) GAA nanowire FETs, which use a cylindrical gate to surround the channel for better control and scalability.

A major limitation of standard MOSFETs is that the subthreshold swing (SS) cannot go below 60 mV/decade [19]. To solve this issue, ferroelectric field-effect transistors (Fe-FETs) use the negative capacitance (NC) effect from a ferroelectric (FE) layer placed inside the gate oxide stack. This design helps Fe-FETs achieve an SS of less than 60 mV/decade, which improves efficiency and reduces power consumption [20]. Figure 5(a) shows a 3D schematic of an Fe-FinFET and Figure 5(b) shows a 2D cross-sectional view of the same device.

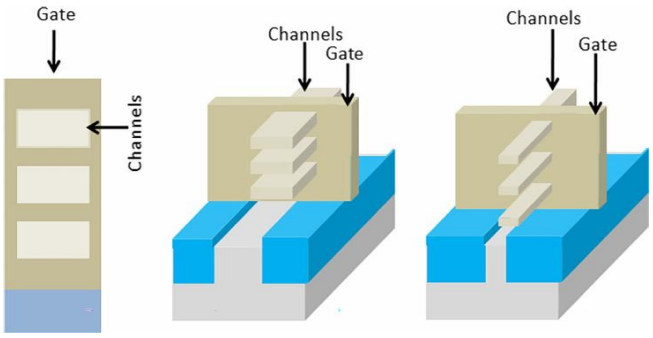

Figure 4. Device structures of advanced gate-all-around (GAA) technologies (a) Nanosheet FETs and (b) Nanowire FETs. Adapted from Reddy *et al.* [8]

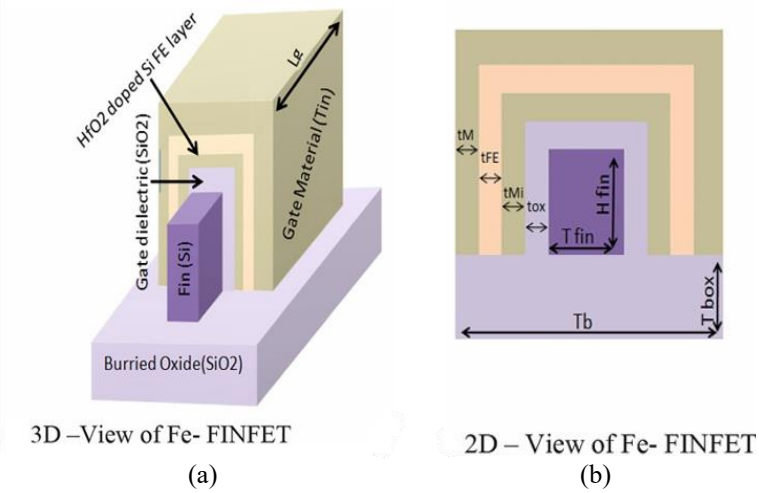

Figure 5. Illustration of Fe-FinFET structure (a) 3D schematic view and (b) 2D cross-sectional view. Adapted from Reddy *et al.* [8]

4. MATERIALS, DEPOSITION METHODS, AND FABRICATION OF FINFETS

4.1. Materials used in FinFET construction

For ease of fabrication and good electrical properties, Silicon is still the main construction material. Nevertheless, as devices scale down to a smaller level, silicon dioxide (SiO_2) faces problems like short-channel effects and high leakage current when used as a gate material. To solve this issue, hafnium oxide (HfO_2) are now used [21]. It permits for a wider gate insulator while keeping high capacitance. This reduces leakage and

improves gate control without further scaling [22]. For modern chips, it helps maintain better performance and lesser power use. Metal gates made of titanium nitride (TiN) provide a tunable work function, which helps ad-just the threshold voltage (Vt). The gate material's tunability supports low-power designs and improves overall efficiency [23]. The combination of metal gates and high-k dielectrics reduces gate leakage and improves scalability. Indium gallium arsenide (InGaAs) is also being explored as alternatives to silicon. InGaAs has higher electron mobility, which allows faster charge transport, higher speed, and lower power use [22]. Since silicon properties reaches its limits at nanoscale dimensions, InGaAs automatically becomes the better choice [5].

4.2. Thin-film deposition techniques for FinFETs

One of the widely used method to deposit thin films on multiplex three-dimensional surfaces is chemical vapor deposition (CVD). It produces uniform and conformal coatings that are important to yield fine fin geometry. Plasma-enhanced chemical vapor deposition, also known as PECVD, allows lower temperature film growth that helps create uniform dielectric layers while reducing thermal damage to the layout below [24]. Atomic layer deposition (ALD) gives atomic-level film thickness control. It is mainly used for high-k materials such as HfO_2. This precise control improves the quality of the gate dielectric,

reduces leakage, and enhances device performance. Figure 6 shows a model structure of a bulk FinFET [25] that helps explain source/drain (SD) doping. At present, the incidence angle of beam limits for doping top fin regions are not severe. However, taller fins designed to increase on-current may require smaller grazing angles of 10° or less. Shadowing from nearby resist masks can also reduce acceptable angles, making doping uniformity harder to maintain without the precision offered by ALD.

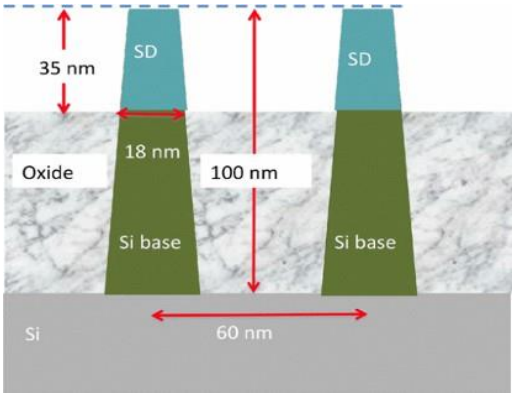

Figure 6. Schematic of a 22 nm bulk FinFET model with 60 nm fin pitch, 35 nm channel and source/drain height, and 100 nm deep etched fins. Adapted from Seidel *et al.* [25]

4.3. Fabrication process and characteristics of Bulk-Si FinFETs

Figure 7 shows the construction steps of Bulk-Si FinFETs that are oxide-isolated. The process starts with a Bulk-Si wafer designated p-type (100). N-well and P-well regions are doped at different densities to study the effects of body doping. Device isolation is then performed, followed by the deposition of a SiO_2/Si_3N_4/TEOS sandwich layer. This stack protects the fin during oxidation and etching. Trenches are created using anisotropic dry etching and electron-beam lithography. Si_3N_4 (Silicon Nitride) spacers protect the fin. Dry oxidation form the isolation oxide around the fin. Quasi-isotropic etching method is also used in this process. A thin gate oxide is then deposited, and a polysilicon gate is patterned using reactive ion etching (RIE). Electron-beam lithography plays a vital role in patterning. Two of the TEOS sidewall steps create the drain and source regions, followed by dopant activation using rapid thermal annealing (RTA). Nickel silicide reduces contact resistance. The thick sidewalls minimize parasitic capacitance. This process concludes with typical back-end fabrication steps [26].

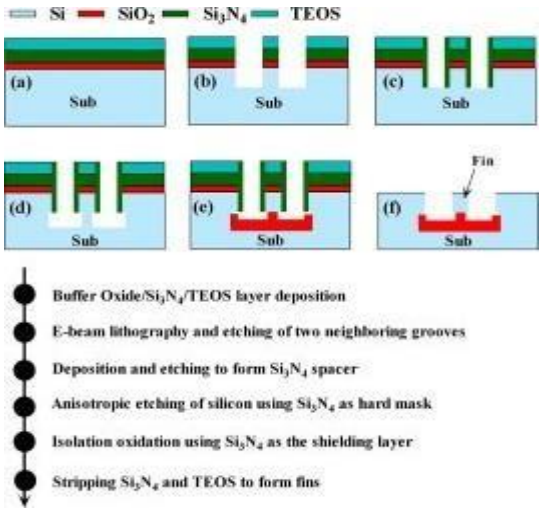

Figure 7. Illustration of the Bulk-Si FinFET fabrication process following a quasi-planar CMOS flow. Adapted from Zhou *et al.* [26]

4.4. Fabrication process and characteristics of SOI FinFETs

Silicon-on-insulator also known as SOI FinFET is shown in Figure 8(a). A tri-gate 3D structure uses three fins and a 08 nm long channel. The gate stack is composed of a high-k dielectric material along with SiO_2. Figure 8(b) displays the device's internal channel region, highlighting both the inverted channel and the silicon body [27]. Each SOI FinFET is built on a combined BOX and substrate layer about 30 nm thick. A SiO_2 layer of 1 nm depth coats three sides of every channel, forming the base oxide. Over this, a SiO_2 gate oxide of 0.5 nm thickness and a high-k dielectric layer of 0.5 nm depth are applied. Materials such as HfO_2, ZrO_2, Al_2O_3, and Si_3N_4 are used for this outer high-k layer, with dielectric constants of 28, 20, 9, and 7.8, respectively. Together, these layers form a stacked gate structure over the fin. Table 1 lists values for each material combination equivalent oxide thickness also known as EOT. The fin dimensions are designed for symmetry, with 08 nm source/drain lengths and 06 nm height and width, giving the device a square geometry. This aspect ratio helps maintain consistent electrical behavior and stable performance. Table 2 provides a complete summary of the device parameters and design specifications.

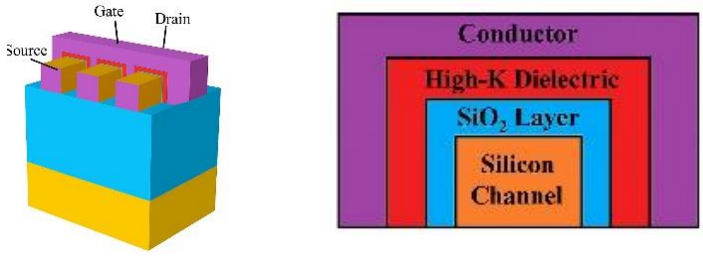

Figure 8. SOI FinFET structure (a) 3-Fin SOI FinFET featuring a SiO2/high-k gate stack, and (b) internal channel region cross-sectional view. Adapted from Nanda *et al.* [27]

Table 1. Gate-stack materials and their equivalent oxide thickness (EOT)

Gate-stack materials	Physical thickness	Dielectric constant of the high-k	EOT (nm)
SiO_2	1.0 nm	–	–
Si_3N_4 + SiO_2	(0.5+0.5) nm	7.8	0.75
Al_2O_3 + SiO_2	(0.5+0.5) nm	9	0.722
ZrO_2 + SiO_2	(0.5+0.5) nm	20	0.597
HfO_2 + SiO_2	(0.5+0.5) nm	28	0.569

Table 2. Device parameters for the SOI FinFET with 3-Fins and 08 nm length

Parameter	Description	Values
L_g, L_d, L_s	Gate, Drain & Source Length	8 nm
H_d, H_s	Drain and Source Height	6 nm
T_{Sub} + T_{Box}	p-Substrate + Buried oxide	(10 + 20) nm
N_D	Doping Concentration at Drain	1×10^{18} N type
N_S	Doping Concentration at Source	5×10^{18} N type
N_{ch}, N_{Sub}	Doping for channel and substrate	1×10^{15} P type
t_{ox}	Oxide thickness	EOT

5. OPERATIONAL BEHAVIOR AND PERFORMANCE METRICS OF FINFETS

FinFET operation depends on two main voltages. These are: the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}). The transistor source terminal is usually grounded in FETs. The gate voltage (V_{GS}) regulates the development of a conductive channel between source and drain along the fin-shaped semiconductor [7]. A positive V_{GS} pulls electrons in n-type transistors, creating a conductive path and turning the device "on." In a p-type FinFET, a negative V_{GS} attracts holes, which also turns the device "on." When no gate voltage is applied, the device stays "off" [9]. For a significant V_{GS} above threshold, the drain-source voltage (V_{DS}) drives charge carriers through the channel path, producing a drain current (I_D).

At low V_{DS}, the transistor works in the linear region. Here, V_{DS} and I_D are proportional. V_{GD} advances toward threshold voltage (V_{th}) with increasing V_{DS}, reaching pinch-off region. At higher V_{DS}, it reaches saturation, where I_D becomes nearly constant. FinFETs provide stronger electrostatic control through their multi-gate design, improving efficiency in sub-10 nm devices [28].

Figure 9 and Figure 10 illustrates I_D-V_{DS} correlation for bulk CMOS and finFETs. as V_{GS} increases from 0 V to 0.9 V. The FinFETs I_{ON} is higher than that of bulk CMOS due to the three-dimensional structure leading to better gate control. This design also increases output resistance, which means lesser modulation channel length and better overall efficiency. Recent studies show that FinFETs reduce channel length modulation by about 25% compared to planar transistors, improving linearity and stability in analog and RF applications [30]–[32]. The strong gate control of the tri-dimensional structure further limits channel length modulation, giving FinFETs better control and efficiency.

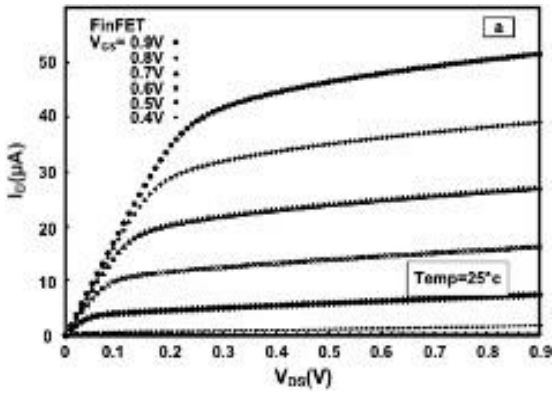

Figure 9. FinFET current-voltage (I-V) characteristics. Adapted from Farkhani *et al.* [29]

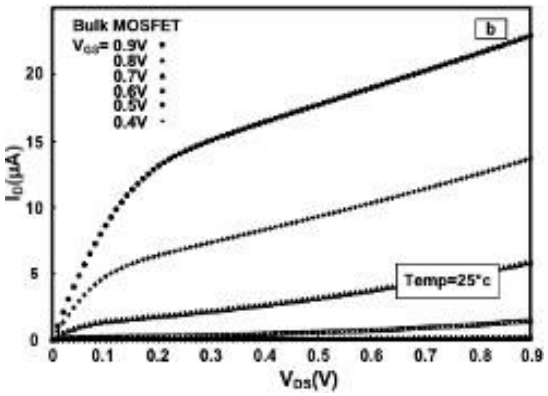

Figure 10. Bulk CMOS transistors current-voltage (I-V) characteristics. Adapted from Farkhani *et al.* [29]

(I_{ON} / I_{OFF}) is an important performance metric for FinFETs. When V_{GS} is high, the current flow I_{ON} indicates the device is fully turned on in conducting state. V_{GS} being almost zero, the current flow I_{OFF} is called leakage current depicting non-conducting state. FinFETs have a greater I_{ON} / I_{OFF} ratio comparing to the planar FETs, especially when the supply voltage is low. They keep I_{OFF} low while maintaining a high I_{ON}, making them suitable for low-power circuits. Studies comparing FinFET and planar CMOS devices confirm that FinFETs achieve much higher I_{ON} / I_{OFF} ratios below 0.7 V, showing their advantage in high-performance applications at low-voltages [6], [29], [33], [34].

Figure 11 shows that at lower supply voltages, FinFETs have a greater ratio of I_{ON} / I_{OFF} than bulk CMOS. At low voltages, I_{OFF} in both devices is similar, but I_{ON} is higher in FinFETs. At voltages above 0.72 V, the bulk CMOS transistor starts to exhibit a greater I_{ON} / I_{OFF} ratio. It occurs because the on current of the bulk CMOS transistor approaches FinFETs I_{ON} while keeping a lower I_{OFF}, making it slightly more efficient at higher voltages [29].

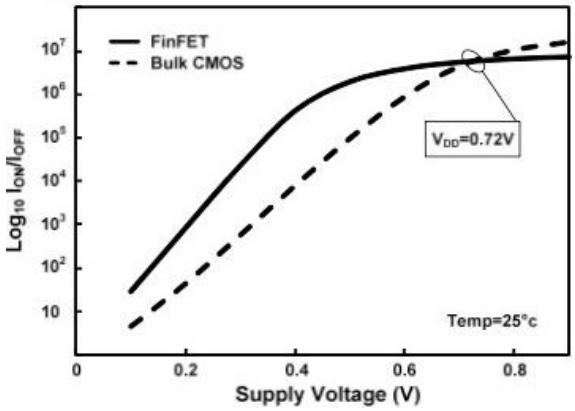

Figure 11. I_{ON} / I_{OFF} ratio with respect to supply voltage for bulk CMOS transistors and FinFETs. Adapted from Farkhani *et al.*[29]

Figure 12 shows how the drain current (I_D) changes with gate-source voltage (V_{GS}) for FinFETs and bulk CMOS transistors at V_{DS}: 0.1 V and 1.1 V. Drain-Induced Barrier Lowering also known as DIBL is one of the key differences seen in the figure. Bulk CMOS has a 124 mV/V DIBL, while FinFETs have a much lower value of around 58 mV/V. FinFETs also have a steeper subthreshold slope, which improve switching speed, reduce leakage current, and increase power efficiency. Simulation results confirm that FinFETs offer better reliability and stability in scaled technologies [35], [36]. Studies also report that FinFET circuits have lower leakage variability and more stable subthreshold slopes across temperatures from -40 °C to 125 °C, which is essential for reliable operation [37]–[39]. Figure 12 illustrates FinFETs having a lower V_{th} of 0.36 V, compared to 0.55 V in bulk CMOS.

Figure 12 illustrates subthreshold swing (SS) for FinFETs being about 21% smaller for bulk CMOS subthreshold swing at room temperature [29]. Figure 13 shows SS variation for temperature from -40 °C to 125 °C. A linear increase in SS in seen with increasing temperature for both devices. However, increase rate is greater for bulk CMOS. Recent studies show that FinFETs maintain stable switching performance, with only small SS changes (around 5%) even under extreme temperature conditions. This confirms their strong thermal stability and reliability for harsh environments [8], [40]–[42].

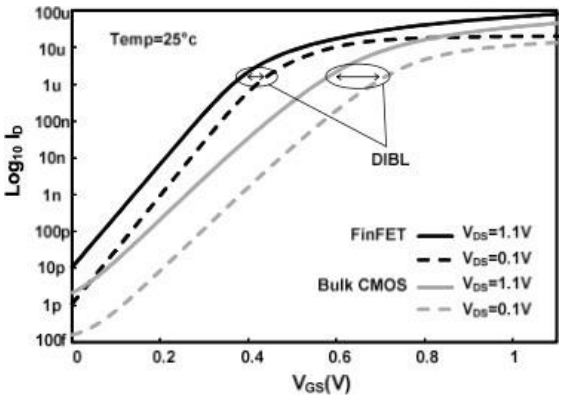

Figure 12. I_D–V_{GS} characteristics for FinFET and bulk CMOS devices measured at V_{DS} = 0.1 V and 1.1 V Adapted from Farkhani *et al.* [29]

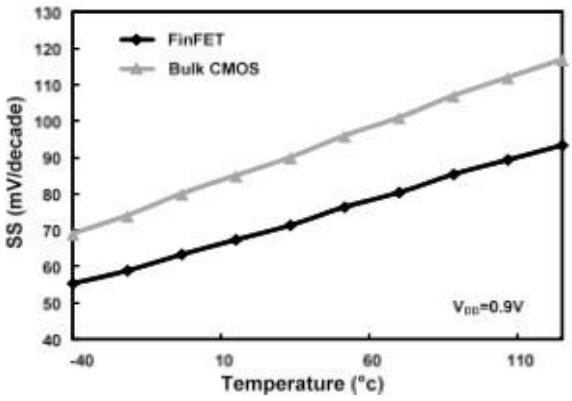

Figure 13. Temperature dependence of subthreshold swing in FinFET and bulk CMOS devices. Adapted from Farkhani *et al.* [29]

6. RESULTS AND DISCUSSION

The comprehensive review presented in this manuscript synthesizes pivotal advancements and performance benchmarks in FinFET technology, offering significant insights into device scalability, efficiency, and reliability compared to conventional planar MOSFET architectures. By evaluating the literature on structures, fabrication methods, materials, and device performance metrics, this study provides an integrated perspective essential for both academic researchers and semiconductor industry professionals. These conclusions are further supported by recent technology roadmaps, which highlight the transition from FinFET to gate-all-around (GAA) architectures at the 2-nm node, emphasizing electrostatics-driven scaling as the primary enabler of continued CMOS advancement [12], [43].

FinFETs demonstrate superior electrostatic control due to their tri-gate geometry, which effectively suppresses short-channel effects in aggressively scaled nodes. Studies on junction-less and gate-engineered FinFET variants confirm that fin geometry and spacer design are decisive levers for leakage suppression, as they improve drain-induced barrier lowering (DIBL) resilience and stabilize subthreshold behavior under scaling [44], [45]. Another critical advantage of FinFETs lies in their high on/off current ratio ($I_{ON}/I_{OF\ F}$), which supports both low-power logic and analog/RF circuits. Recent analyses of multifin configurations and careful gate work-function selection demonstrate that these strategies can boost current drive while maintaining off-state control and linearity, reinforcing the circuit-level applicability of FinFET devices [46], [47].

The suppression of short-channel effects also translates into reduced DIBL and steeper subthreshold swing (SS), thereby improving switching efficiency at low supply voltages. Modeling studies on temperature dependence clarify how SS trends evolve with scaling and operating conditions, while experimental III-V/III-N FinFET demonstrations report sub-60-65 mV/dec SS alongside stable threshold control, consistent with our comparative analysis [48], [49]. Sustaining FinFET performance further depends on process innovations, particularly in dielectric engineering. The use of atomic layer deposition (ALD) for high-K gate stacks has

proven essential for achieving tight equivalent oxide thickness control, improved interface quality, and enhanced threshold stability. Recent reports confirm that ALD-deposited HfO_2 films offer superior electrostatics and reproducibility, making this technique a cornerstone of future FinFET scaling [50], [51].

Thermal reliability also remains a decisive factor for device applicability. High-temperature studies on SiC-based CMOS FinFETs demonstrate stable thresholds and competitive SS up to 700 K, while new self-heating characterization work quantifies how layout and geometry, such as underlap, overlap, and fin thickness, directly influence reliability. These results highlight the importance of electro-thermal co-design strategies for robust FinFET integration [52]–[54]. In the context of emerging technology nodes, the insights synthesized here provide a foundation for the evolution from FinFETs to nanosheet-based GAA devices. Comparative benchmarking indicates stronger electrostatic integrity and reliability in nanosheets, while recent self-heating and quantum-transport studies reveal both the performance potential and thermal challenges associated with stacked GAA structures. These findings explain why FinFET design and fabrication guidelines remain highly relevant as the industry transitions toward GAAFET nodes [13], [55], [56].

This review consolidates how structural design, material selection, and fabrication strategies have shaped FinFET performance, while also outlining the boundaries that remain for continued scaling. Challenges such as variability from process imperfections, self-heating in densely integrated fins, and the integration of high-k dielectrics with emerging channel materials highlight the limits of current approaches. As the transition toward nanosheet and nanowire GAA architectures accelerates, the lessons drawn from FinFET design and reliability remain indispensable, serving not as an endpoint but as a framework for addressing the electrostatic, thermal, and quantum transport constraints that define future semiconductor technologies.

7. CONCLUSION

In conclusion, FinFETs represent a major improvement over traditional planar MOSFETs. Their three-dimensional design and strong electrostatic control help overcome scaling challenges. This study highlights FinFET structure, fabrication process, reduced short-channel effects, high I_{ON}/I_{OFF} ratios, and low-power operation. By analyzing design, materials, and performance metrics, the paper shows that FinFETs are well suited for modern high-performance circuits. As device scaling continues, FinFETs and new technologies like GAAFETs will play an important role in future semiconductor development.

AUTHOR CONTRIBUTIONS STATEMENT

Yead Rahman and Md Faiaz Al Islam was responsible for conceptualization, methodology, and investigation. Nafiya Islam, Sunzid Hassan, Sabbir Alom Shuvo, Iftesam Nabi, and Jarif Ul Alam contributed in draft preparation, reviews and editing,

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that there are no known financial or personal conflicts of interest that could have influenced the results or conclusions presented in this paper.

DATA AVAILABILITY

Data availability is not applicable to this article, as no new data were created or analyzed in this review study.

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