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Design and simulation of an electric vehicle charger with integrated interleaved boost converter and phase-shifted full-bridge converter using MATLAB/Simulink

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ABSTRACT

This paper presents the design and simulation of a high-efficiency electric vehicle (EV) charger that integrates a two-phase interleaved boost converter (IBC) with a phase-shifted full-bridge (PSFB) converter using MATLAB/Simulink. In contrast to existing studies that treat these converter stages independently, this work introduces a unified AC–DC–DC architecture that simultaneously minimizes input current ripple, improves DC-bus stability, and enables soft-switching operation for reduced switching losses. The values of the inductors and capacitors are derived analytically based on ripple constraints and switching frequency considerations, and example calculations are explicitly provided. Simulation results demonstrate that the proposed charger maintains a stable 600-V DC bus with less than 2% voltage ripple, delivers a controlled charging current of 100 A with 3 A ripple, and achieves an overall efficiency of 95%. These findings indicate that the integrated interleaved–PSFB topology provides superior conversion efficiency and power quality, making it a strong candidate for future EV fast-charging infrastructure.

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1. INTRODUCTION

The rapid growth of electric vehicle (EV) technology has become a major driving force in the global transition toward sustainable energy solutions [1], [2]. EVs offer a promising pathway to reduce carbon emissions and dependence on fossil fuels, positioning them as a critical component of climate change mitigation efforts [3], [4]. However, to support large-scale EV adoption, the development of efficient, reliable, and high-quality charging infrastructure is essential [5], [6]. Accordingly, the demand for advanced charging systems has intensified, accelerating the need for energy-efficient and robust EV chargers [7], [8].

The design of EV charging systems presents several technical challenges, including achieving high conversion efficiency, ensuring low harmonic distortion, and maintaining current quality to mitigate grid-side disturbances [9], [10]. Furthermore, these chargers must tolerate input voltage fluctuations, dynamic load conditions, and simultaneously comply with international safety and regulatory standards [11]–[13]. As the global population of EVs continues to rise, these challenges become increasingly critical, emphasizing the need for innovative and reliable charging technologies [14]–[16].

A commonly employed power conversion strategy includes a front-end boost converter followed by a secondary DC–DC conversion stage [17]–[19]. However, conventional single-phase boost converters suffer

from large current ripple and substantial stress on passive components, leading to higher thermal losses, reduced energy efficiency, and increased filtering requirements [20].

To address these limitations, interleaved boost converters (IBCs) have been proposed as an effective solution [21]–[23]. By distributing the input current across multiple switches operating out of phase, this topology effectively minimizes input current ripple. As a result, the reduced current ripple leads to lower voltage ripple across capacitors and mitigates dynamic voltage stress on passive components, such as inductors and capacitors [24]–[26]. This not only enhances overall efficiency but also improves the reliability and lifespan of the passive components used in EV charging systems. Meanwhile, phase-shifted full-bridge (PSFB) converters have demonstrated superior performance in high-efficiency DC-DC conversion, thanks to their ability to reduce switching losses and handle high-power applications [27]–[29]. The use of phase-shifted pulse width modulation (PWM) control enables precise voltage regulation, ensuring high output efficiency and low harmonic distortion, making it ideal for EV charging systems [30].

Although both topologies have been individually studied and optimized within the EV power electronics literature, existing works typically treat them as isolated subsystems rather than coordinated and integrated charging architecture. Moreover, many studies focus on theoretical analysis or hardware experimentation without presenting a unified framework of modeling, component selection, and integrated performance evaluation. This research addresses this gap by developing a complete AC–DC–DC charging architecture that combines IBC and PSFB converters within a unified simulation framework.

The key contributions of this paper are as follows: i) An integrated EV charger architecture combining IBC for DC bus regulation and PSFB for isolated DC-DC conversion; ii) Explicit analytical design of L and C values, including ripple-based selection and example calculations; iii) Simulation-based verification of performance, demonstrating stable 600 V DC-bus regulation, controlled 100 A charging current, <2% voltage ripple, and 95% overall efficiency; and iv) A validated modelling foundation for future hardware prototyping, forming a basis for laboratory implementation and control refinement.

By deploying the IBC on the front-end to minimize input ripple and utilizing the PSFB topology at the back-end to enable soft-switching and isolation, the proposed architecture enhances conversion efficiency, thermal performance, and power quality. The results presented in this work demonstrate the feasibility and performance benefits of the integrated topology, contributing valuable insight for future high-power EV fast-charging system designs.

2. THE PROPOSED OF ELECTRIC VEHICLE CHARGER SYSTEM

Figure 1 shows the block diagram of the proposed EV charger system. Figure 1 illustrates the overall design of the charger, which consists of an AC power source, a full-bridge rectifier, an IBC, a PSFB converter, an LC filter, and a charger controller circuit. The AC source provides the input AC voltage, which is first rectified by the full-bridge rectifier. The resulting DC voltage is then processed by the IBC, which steps up and regulates the voltage to produce a stable DC bus voltage. This DC bus voltage is subsequently fed into the PSFB converter, which ensures a well-regulated DC output suitable for charging the EV battery pack. An LC filter is connected at the output stage to reduce voltage and current ripple, thereby improving the charging quality delivered to the battery.

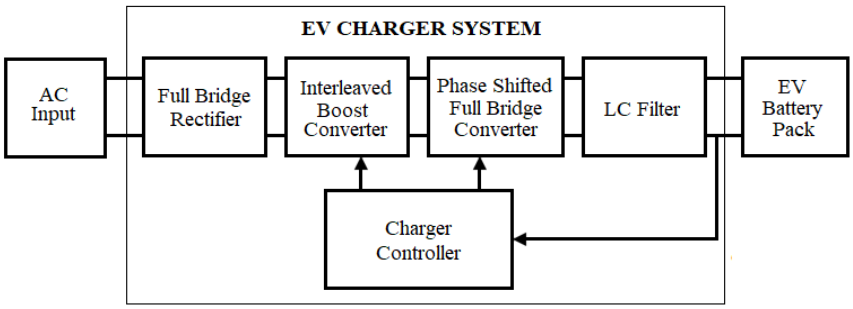

Figure 1. Block diagram of the proposed EV charger system

The charger controller circuit plays a crucial role in coordinating the operation of the proposed EV charger. At the front-end, the controller regulates the duty cycle of the IBC to maintain a stable DC bus voltage and to minimize input current ripple, thereby improving the power quality drawn from the grid.

At the DC-DC stage, the controller drives the PSFB converter using phase-shifted pulse-width modulation (PS-PWM). This technique allows precise regulation of the output voltage and current while enabling soft-switching operation, which significantly reduces switching losses and enhances system efficiency.

In addition to voltage and current regulation, the charger controller incorporates multiple protection features, such as over-voltage, over-current, and short-circuit protection, ensuring safe operation during the charging process. By dynamically adjusting switching parameters based on real-time feedback from both the DC bus and the battery pack, the controller guarantees efficient, stable, and reliable charging performance. This comprehensive control strategy ensures that the proposed EV charger system meets the requirements for high efficiency, reduced harmonic distortion, and compliance with safety standards in modern EV charging applications.

2.1. Interleaved boost converter

An interleaved boost converter (IBC) is a power electronics circuit designed to step up (boost) an input DC voltage to a higher DC voltage, while minimizing current ripple and enhancing overall system efficiency. The key principle behind this converter is the use of multiple boost converters operating in parallel, with a phase shift between them. This phase-shifting operation helps distribute the current load evenly, thereby reducing ripple current and minimizing stress on individual components.

Figure 2 illustrates a two-phase IBC circuit with a rectified AC input voltage. It consists of two boost converters operating in parallel, with a typical phase shift of 180 degrees between them. In this configuration, the two converters share the load, and their operation is arranged so that the current ripple from each inductor partially cancels each other out. As a result, the output voltage is smoother, and the input current ripple is reduced, leading to improved overall system efficiency and lower stress on individual components.

In a two-phase IBC, the input DC voltage is alternately applied to two inductors, each operating at different phases within the switching cycle. This phase-shifted operation helps balance the current load, decreases electromagnetic interference (EMI), and reduces the size and cost of passive components such as inductors and capacitors. Moreover, the two-phase design enables the converter to operate at higher switching frequencies without significantly increasing losses or the size of components. Figure 2 depicts the current flow, with the phase-1 current illustrated in red and the phase-2 current in blue.

The key advantages of IBCs include improved efficiency, reduced EMI, and enhanced thermal management. By distributing the current load across multiple inductors, the converter can operate at higher frequencies without causing significant increases in losses or component size. These characteristics make IBCs particularly suitable for high-power applications, such as EV chargers and renewable energy systems, where high efficiency and low ripple are essential for optimal performance.

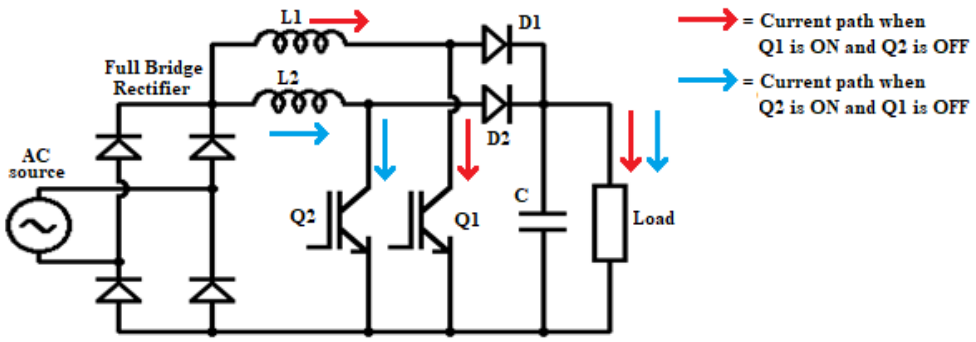

Figure 2. IBC circuit with rectified AC voltage input

2.2. Phase-shifted full-bridge converter

The phase-shifted full-bridge (PSFB) converter is a widely adopted topology for high-efficiency DC–DC conversion, especially in applications that demand high power output such as EV chargers, industrial power supplies, and renewable energy systems [31]. This converter employs four switching devices, typically metal-oxide-semiconductor field-effect transistors (MOSFETs) or insulated gate bipolar transistors (IGBTs), configured in a full bridge arrangement. The fundamental principle of operation lies in the control of the phase shift between the gating signals of the two bridge legs. By varying this phase shift, the converter regulates the power transfer while enabling soft switching, which significantly reduces switching losses and EMI, thereby improving overall efficiency, particularly at high switching frequencies [32].

In this topology, the primary side of the transformer is driven by the four power switches, while the secondary side employs rectification and filtering to deliver a stable DC output. The phase shift between the two switch pairs governs the applied voltage across the transformer, thereby determining the energy transfer and timing of the switching transitions. Under appropriate conditions, this control enables zero-voltage switching (ZVS), and in some cases, zero-current switching (ZCS), both of which reduce switching stress and enhance converter reliability [33].

A critical enabler of ZVS in the PSFB converter is the leakage inductance of the transformer and the parasitic capacitances of the switching devices. The leakage inductance stores energy during each switching cycle, which is then used to charge and discharge the parasitic output capacitances of the MOSFETs. This interaction ensures that the switch voltage falls to zero before the device is turned on, thereby achieving ZVS. Consequently, switching transitions occur with minimal overlap between voltage and current waveforms, drastically reducing switching losses. However, adequate leakage inductance is necessary to guarantee reliable ZVS over the entire load range, particularly under light-load conditions.

On the other hand, the parasitic capacitances of the switches, while typically considered a non-ideal effect, are deliberately exploited in the PSFB topology to facilitate ZVS. These capacitances provide the natural resonant elements that interact with the leakage inductance, forming a resonant transition that shapes the switch voltage waveform. The proper balance between leakage inductance and device capacitances is therefore crucial: insufficient inductance may prevent complete discharge of the parasitic capacitances, while excessive inductance can introduce unnecessary circulating currents and conduction losses. Overall, the PSFB converter achieves high efficiency by leveraging phase-shift modulation, leakage inductance, and parasitic capacitances to realize ZVS, making it one of the most reliable and efficient topologies for high-power DC–DC conversion.

Figure 3 shows the schematic of a PSFB converter. The phase-shift control allows the converter to adapt to varying load conditions, thereby maintaining high efficiency and ensuring a stable DC output. In the figure, the phase-1 current is denoted by the red trace, while the phase-2 current is denoted by the blue trace. This topology is renowned for its ability to deliver a regulated DC output with minimal harmonic distortion, making it a preferred choice for modern power conversion systems that prioritize both performance and reliability.

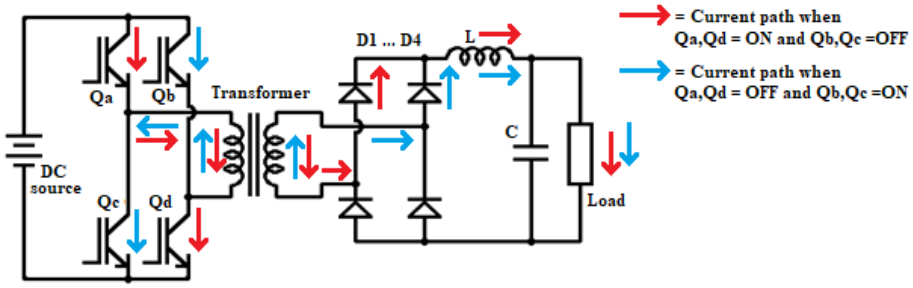

Figure 3. PSFB converter schematic diagram

2.3. Integrated IBC and PSFB converter

The integration of an IBC and a PSFB converter present a highly effective solution for EV charging systems, as it combines the advantages of both topologies to enhance overall performance and reliability. At the front-end stage, the IBC is employed to step up the input voltage while simultaneously reducing current ripple. By interleaving the operation of multiple boost phases with a 180° (or phase-shifted) switching scheme, the input current ripple is significantly minimized. Theoretically, for an N-phase interleaved converter, the input current ripple can be expressed as:

$$\Delta I_{in} = \frac{V_{in} \cdot (1-D)}{N \cdot fs \cdot L} \quad (1)$$

where V_{in} is the input voltage, D is the duty cycle, L is the inductance per phase, fs is the switching frequency, and N is the number of phases. From this relationship, it is evident that increasing the number of interleaved phases reduces ripple and improves efficiency. This also leads to lower conduction and switching losses in each semiconductor device, improved thermal distribution, and the ability to operate at higher power densities, which are essential for high-power EV charging applications.

The output of the interleaved boost stage feeds into a regulated DC bus, ensuring stable voltage with minimal ripple. This stable DC bus is a critical requirement, as it directly influences the performance of the subsequent isolated conversion stage. The PSFB converter is then utilized as the isolated DC-DC stage. The PSFB topology operates based on phase-shift modulation, where the leading and lagging legs of the full bridge are controlled with a variable phase shift to regulate power transfer. One of its theoretical advantages is the achievement of ZVS for the primary switches, which reduces switching losses and enhances efficiency at high frequencies. The soft-switching condition is made possible due to the energy stored in the leakage inductance of the transformer and the parasitic capacitance of the MOSFETs, which assist in the resonant transition of the switching devices.

The fundamental output voltage of the PSFB converter can be expressed as (2):

$$V_{out} = \frac{n \cdot D_{ph}}{2} \cdot V_{dc} \quad (2)$$

where n is the transformer turns ratio, D_{ph} is the phase shift ratio (0–1), and V_{dc} is the input DC bus voltage supplied by the interleaved boost stage. This equation shows that the PSFB provides a wide output voltage regulation capability while maintaining soft-switching conditions over a broad load range.

By integrating these two converters, the system benefits from the low input ripple and high efficiency of the interleaved boost stage and the high-frequency isolation, galvanic safety, and soft-switching performance of the PSFB stage. This synergy makes the combined topology an ideal candidate for next-generation high-power EV charging systems, where efficiency, power density, and reliability are of paramount importance. Figure 4 illustrates the integration of the IBC and PSFB converter for the EV charging system.

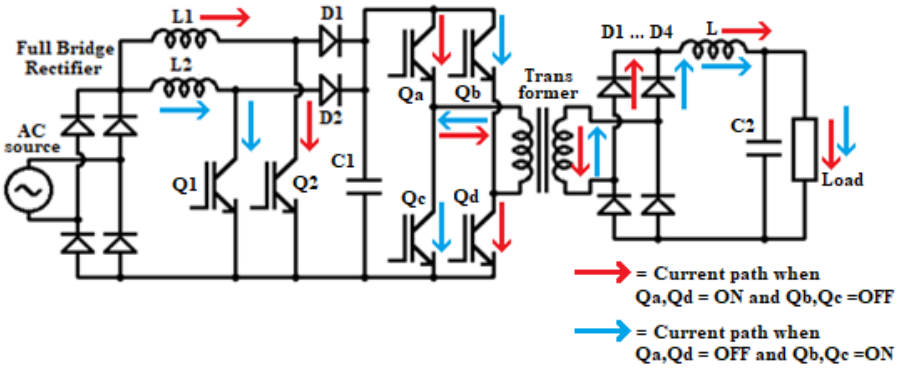

Figure 4. Integrated IBC and PSFB converter schematic diagram

3. METHOD

3.1. Design of IBC model

The IBC consists of two boost converter stages connected in parallel, where each stage is composed of an inductor, a power switch, a diode, and an output capacitor. The two converter stages operate with a 180° phase shift, allowing the input current to be evenly distributed between both phases. This interleaving operation reduces the current stress on individual components, suppresses both input and output current ripples, enhances electromagnetic compatibility (EMC), and improves the overall efficiency of the system.

The input voltage (V_{in}) is applied equally to both phases, while the regulated DC output voltage (V_{out}) is the combined contribution of the parallel stages. The voltage gain of the two-phase IBC is expressed as (3):

$$V_{out} = \frac{V_{in}}{1-D} \quad (3)$$

where D is the duty cycle. With $V_{in} = 311$ and $V_{out} = 600$ V, the theoretical duty ratio is $D = 0.48$.

a. Inductor value selection

The inductor current ripple per phase is given by (4):

$$\Delta I_L = \frac{V_{in} \cdot (D)}{f s \cdot L} \quad (4)$$

By setting a maximum allowable ripple current 10% of the average inductor current, the required inductance can be calculated.

$$V_{in} = 220 \times 1.414 \approx 311\ V$$
$$D = 0.33$$
$$f_s = 20\ kHz$$
$$\textit{Target ripple}: \Delta I_L = 0.1 \times 100\ A = 10\ A$$
$$\textit{Substituting}: L = \frac{311 \times 0.33}{10 \times 20000} = 0.74\ mH \quad (5)$$

To ensure lower ripple and thermal margin, a practical value of 1 mH was selected, providing ripple reduction below the theoretical threshold and enhancing current stability. The interleaving technique significantly reduces the net ripple current at both the input and output. This effect occurs because the ripple components generated by the two phases are of opposite polarity and time-shifted, leading to partial cancellation. As a result, the load receives cleaner power, the input source experiences lower stress, and the converter achieves higher reliability and efficiency.

b. Output capacitor selection

To design the output capacitor, a ripple-based sizing method is applied. The capacitor value is selected to limit DC bus voltage ripple to <2%. The required output capacitance C_{out} is expressed as:

$$\Delta V_{out} = \frac{I_{out} \cdot D}{f_s \cdot C_{out}} \quad (6)$$

where ΔV_{out} is the permissible output ripple, I_{out} is the load current, D is the duty cycle, f_s is the switching frequency, and C_{out} is the required output capacitance.

For a nominal output voltage of 600 V, the allowable ripple is set to 2% (ΔV_{out} = 12 V), With I_{out} = 100 A, D = 0.33, and fs = 20 kHz, the capacitance is calculated as:

$$C_{out} = \frac{I_{out} \cdot D}{f_s \cdot \Delta V_{out}} = \frac{100 \cdot 0.33}{20000 \cdot 12} \approx 137\ \mu F \quad (7)$$

To ensure reliability against equivalent series resistance (ESR) effects and dynamic load variation, a 470 µF capacitor bank was implemented through parallel capacitors to increase ripple-current handling capability.

3.2. Design of PSFB converter model

The PSFB converter is designed to achieve efficient DC–DC power conversion with reduced switching losses and enhanced output voltage regulation. This converter topology employs a full bridge configuration consisting of four power switches arranged in two complementary pairs, a high-frequency transformer, rectifier diodes, and an output filter.

The converter operates under phase-shift modulation, where the relative timing of the switching signals applied to the bridge legs is controlled. This technique enables zero-voltage switching (ZVS) during commutation intervals, significantly lowering switching losses and improving efficiency, particularly under high-power operating conditions.

On the primary side, the DC input voltage V_{in} is applied to the transformer windings through the full bridge network. Energy is transferred across the high-frequency transformer and rectified on the secondary side, followed by filtering to produce a regulated DC output voltage ΔV_{out}.The voltage gain of the PSFB converter is determined by the transformer turns ratio (n) and the effective duty cycle (D) of the phase-shift control, and can be expressed as:

$$V_{out} = n \cdot V_{in} \cdot D \quad (8)$$

where n =Ns/Np, with Ns and Np being the number of secondary and primary turns of the transformer, respectively. In this study, a turns ratio of as 3:1 ($N_p : N_s = 3 : 1$), is selected to step down a 600 V DC bus voltage on the primary side to approximately 200 V on the secondary side. This selection is suitable for EV battery charging applications while maintaining high efficiency in the PSFB operation.

The ZVS mechanism is achieved by utilizing the energy stored in the transformer leakage inductance and the parasitic capacitances of the power switches. This eliminates the overlap between voltage and current during switching transitions, thereby reducing power dissipation. Furthermore, phase-shift modulation provides precise control over energy transfer, ensuring stable output voltage regulation under variable input and load conditions.

On the secondary side, the output filter, typically comprising an inductor and a capacitor, smooths the rectified voltage to minimize ripple and improve power quality. The output voltage (ΔV_{out}) is defined as (9):

$$\Delta V_{out} = \frac{I_{out} \cdot D}{fs \cdot C} \tag{9}$$

where I_{out} is the load current, fs is the switching frequency, and C is the output capacitance.

In the design, the output voltage ripple is limited to less than 3% of the nominal 200 V output (ΔV_{out} = 6 V), With I_{out} = 100 A, D = 0.33, and fs = 20 kHz, and assuming continuous conduction, the required capacitance is calculated as (10):

$$C_{out} = \frac{I_{out} \cdot D}{f_s \cdot \Delta V_{out}} = \frac{100 \cdot 0.33}{20000 \cdot 6} \approx 275\ \mu F \tag{10}$$

To account for component tolerances, transient load variations, and capacitor ESR, a practical capacitance value of 470 µF is selected. This value aligns with common EV charger designs reported in literature, ensuring reduced voltage ripple and enhanced output stability under varying load conditions.

4. RESULTS AND DISCUSSION

The proposed EV charger system was simulated using MATLAB/Simulink to evaluate its performance under various operating conditions. The simulation model, shown in Figure 5, accurately represents the power stage configuration and control strategy of the integrated IBC–PSFB charger. The system parameters and component ratings are listed in Table 1, while the DC bus and PSFB control parameters are detailed in Tables 2 and 3.

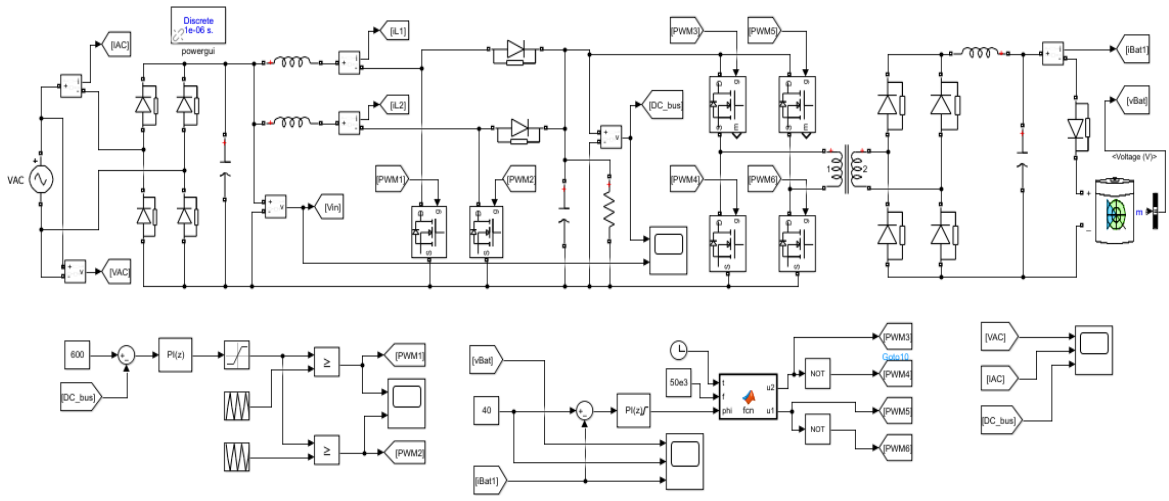

Figure 5. Simulink model of the EV charger system

Table 1. EV charger circuit parameters

Parameter	Symbol	Value
AC input voltage	V_{AC}	220 V
AC input frequency	f	50 Hz
Rectifier capacitor	C	470 µF
Interleaved inductor	L	1 mH
Interleaved capacitor	C	470 µF
Phase-shifted inductor	L	1 mH
Phase-shifted capacitor	C	470 µF
Switching frequency	f_{sw}	20 kHz
Battery (Lithium - Ion)	–	48 V, 50 Ah
Initial state-of-charge	SOC	20%

Table 2. DC BUS controller parameters

Parameter	Symbol	Value
Proportional gain	Kp	5
Integral gain	Ki	0.1

Table 3. PSFB controller parameters

Parameter	Symbol	Value
Proportional gain	Kp	200
Integral gain	Ki	100

4.1. Parameter selection justification

The simulation parameters in Tables 1 to 3 were derived from theoretical calculations and validated against practical design considerations. The rectifier capacitor of 470 µF was selected to limit post-rectification ripple, and the IBC inductor of 1 mH was chosen to maintain current ripple at approximately 10% of the 100 A average phase current. The IBC output capacitor of 470 µF ensures DC bus ripple below 2%, while the PSFB-side output capacitor maintains stable battery-side voltage with acceptable ripple. A 20 kHz switching frequency represents a design compromise between component sizing and switching loss. The 48 V, 100 Ah battery model reflects typical medium-power EV storage characteristics.

4.2. System-level waveform analysis

The AC input voltage, AC input current and DC bus voltage waveforms are shown in Figure 6. The 220 V AC supply is rectified and boosted to a stable DC bus voltage of 600 V, demonstrating stable regulation aligned with the reference setting. The DC bus ripple was measured at <2%, confirming the effectiveness of the IBC ripple cancellation and capacitor sizing approach.

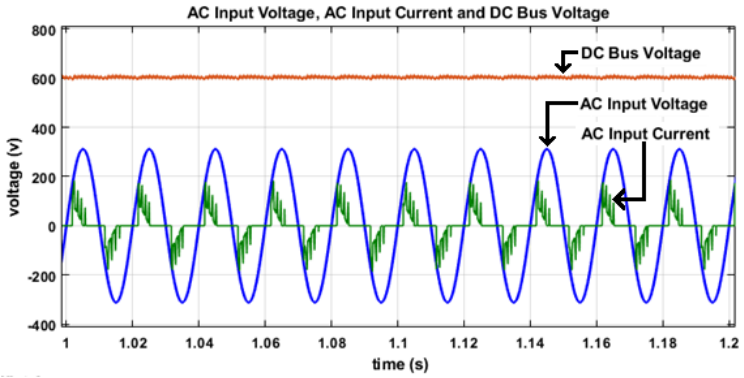

Figure 6. AC input voltage, AC input current and DC bus voltage

4.3. Charging current regulation

The PSFB converter is supplied by the regulated DC bus and delivers the charging current to the battery through a unidirectional rectifier. As shown in Figure 7, the charging current remains tightly regulated at 100 A, validating the controller's ability to track current reference with minimal overshoot and fast transient settling. The current ripple was approximately 3 A peak-to-peak, remaining within the expected performance range for the selected inductance and switching frequency.

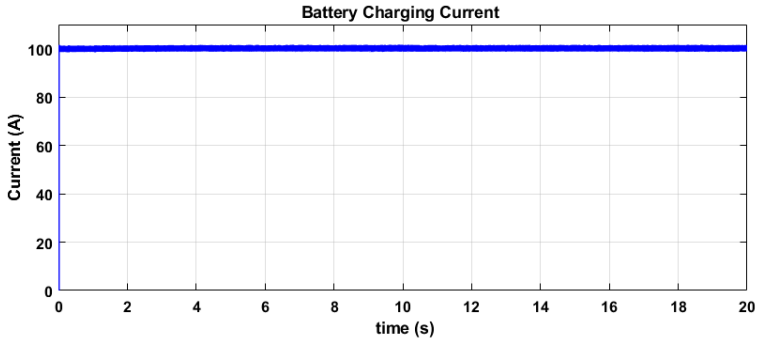

Figure 7. The battery charging current

4.4. Battery charging behavior

The battery voltage progression is illustrated in Figure 8, where the battery voltage increases from 47.5 V to approximately 52 V during the charging period. This smooth voltage rise indicates controlled power transfer without oscillations or overshoot, ensuring safe and healthy battery charging behavior.

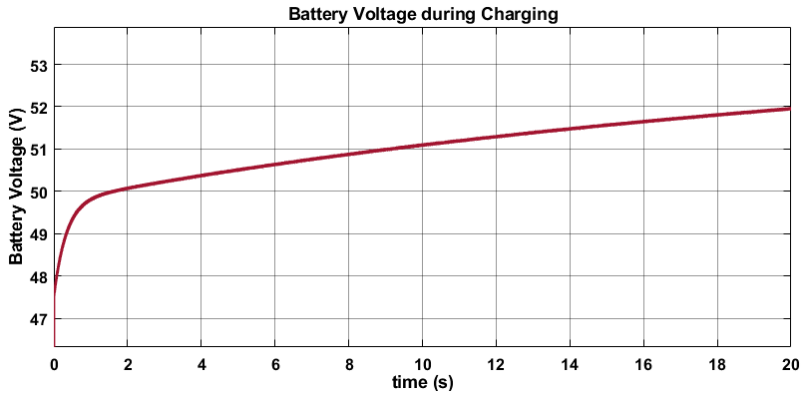

Figure 8. The battery voltage during charging

4.5. Performance summary

The overall performance of the proposed charger demonstrates stable and reliable operation under the simulated test conditions. The DC bus voltage was consistently regulated at 600 V, with a voltage ripple maintained below 2%, indicating effective suppression of bus fluctuations.

The battery charging current remained stable at 100 A, with a measured ripple of approximately 3 A, which aligns with the expected behavior based on the selected filter design and switching frequency. In addition, the battery voltage increased smoothly from 47.5 to 52 V during the charging interval, indicating controlled energy transfer and safe charging dynamics.

The system efficiency was calculated using

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{11}$$

with $P_{out} = 52 \times 100 = 5200$ W and $P_{in} = 5475$ W, the resulting efficiency is

$$\eta = \frac{5200}{5475} \times 100\% = 94.97\% \tag{12}$$

An overall efficiency of approximately 95% demonstrates strong performance and confirms the effectiveness of the integrated IBC–PSFB conversion architecture in delivering efficient and stable battery charging.

5. CONCLUSION

This paper presented the design and simulation of an EV charger system integrating an IBC and a PSFB converter within a unified control framework. The simulation results demonstrated successful DC bus regulation at 600 V, stable charging current of 100 A, battery voltage increase from 47.5 to 52 V, and an overall system efficiency of approximately 95%. With DC bus ripple maintained below 2% and controlled current ripple of 3 A, the proposed architecture effectively reduces switching stress, improves conversion efficiency, and ensures reliable charging behavior. These findings validate the suitability of the IBC–PSFB approach for practical EV charging applications and provide a strong foundation for future work involving hardware prototyping, closed-loop control refinement, and real-world performance validation.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
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Alfin Fitrohul Huda			✓		✓		✓	✓						
Luthfiyyatun Mardiyah			✓		✓		✓	✓	✓	✓	✓		✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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