International Journal of Electrical and Computer Engineering (IJECE)
Vol. 15, No. 6, December 2025, pp. 5223~5233
ISSN: 2088-8708, DOI: 10.11591/ijece.v15i6.pp5223-5233

Optimization of a level shifter integrated with a gate driver using TSMC 130 nm CMOS technology

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Article Info

Article history:

Received Feb 14, 2025
Revised Jul 26, 2025
Accepted Sep 16, 2025

Keywords:

Gate drivers
Integrated circuits
Level shifter
Li-ion battery chargers
Propagation delay
TSMC 130 nm

ABSTRACT

Modern electronic systems increasingly operate across multiple voltage domains, necessitating robust and efficient level shifter (LS) circuits to ensure reliable inter-domain communication. In low-power digital applications, minimizing propagation delay and transition time is critical for achieving high-speed and energy-efficient operation. This work presents a high-performance level shifter optimized for integration within Li-ion battery charger systems. The proposed design achieves a substantial reduction in propagation delays from 0.15 to 0.09062 ns while preserving signal integrity. When integrated with a gate driver, the overall structure exhibits a propagation delay of 0.20468 ns and a transition time of 0.014 ns, marking a significant improvement from the previous 0.036 ns. Furthermore, the proposed circuit occupies only 0.00039 mm² of silicon area, representing a 92% reduction compared to prior implementations (0.05 mm²). The complete design was implemented using Taiwan semiconductor manufacturing company (TSMC) 130 nm complementary metal–oxide–semiconductor (CMOS) technology, with both schematic simulation and layout carried out in the Cadence Virtuoso design environment. These results underscore the potential of the proposed solution for compact and high-efficiency system-on-chip (SoC) battery management applications.

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1. INTRODUCTION

Lithium-ion (Li-ion) batteries have emerged as the leading energy storage technology, replacing nickel-cadmium (NiCd) and nickel-metal hydride (NiMH) batteries due to their superior energy density, longer cycle life, and minimal maintenance requirements [1], [2]. The power nearly all modern portable electronic devices, from smartphones to electric vehicles, while offering critical advantages such as high operational efficiency without memory effect, fast charging capabilities, and integrated safety features including protection against overvoltage, overcurrent, and thermal extremes [3]. Furthermore, their lower environmental toxicity compared to previous chemistries contributes to their widespread adoption [4]. To support these performance requirements, Li-ion battery chargers integrate several functional blocks, including level shifters (L-S), gate drivers (G-D), low dropout regulator (LDO), bootstrap circuit, power metal–oxide–semiconductor (MOS), direct current control (DCC), direct voltage control (DVC), and current sensing circuit (CSC), as illustrated in Figure 1. Among these components, the level shifter–gate driver pair plays a pivotal role in ensuring signal integrity across voltage domains while maintaining low latency and minimal power consumption. This work focuses on optimizing that pair to enhance the overall efficiency of the charger architecture.

Level shifter (LS) circuits play a critical role in system-on-chip (SoC) designs, facilitating the interaction between distinct voltage domains and ensuring that signals from the low voltage domain (V_{DDL}) can be correctly understood in the higher voltage domain (V_{DDH}) and vice versa. The conventional level shifter (CLS) shown in Figure 2, using 10 transistors and deals with complementary input signals V_{IN} and V_{INB} from the low voltage domain, and an output signal V_Z from the high voltage domain.

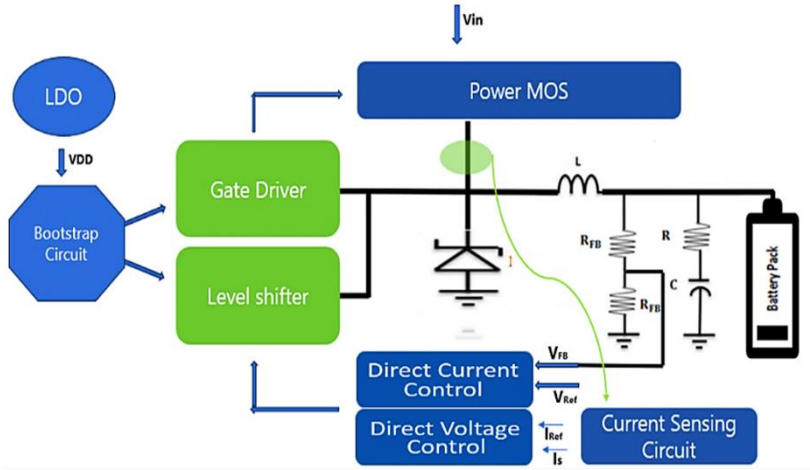

Figure 1. Structure of the lithium-ion battery charger chip

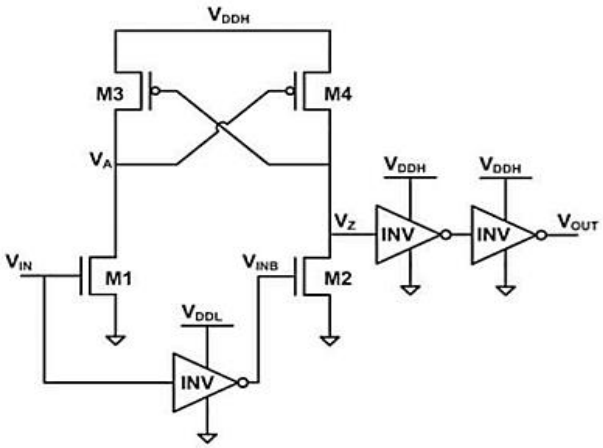

Figure 2. Conventional cross-coupled half latch

When the input voltage V_{IN} is equal to V_{DDL}, the transistor M1 pulls down the V_A node, causing the V_Z to be charged to V_{DDH} by M4. At that point, the transistor M2 persists off because its gate-source voltage (VGS) is V_{INB} which is 0 V in this case. However, there is a notable conflict between the pull-up and pull-down networks. When V_{INB} goes high (reaches V_{DDL}), M2 attempts to pull down the V_Z node, even though it is simultaneously being charged by transistor M4.

This situation creates contention between these opposing actions. Consequently, this leads to elevated dynamic power consumption and extended delays. It is evident that this limitation underscores the impracticality of the conventional LS architecture. Numerous studies have been documented aiming to address the constraints of CLS. For example, Zhai *et al.* [5] used A cascade of four stages of CLS to transform a 200 mV signal into a 1.2 V signal. Nevertheless, implementing such a solution necessitates the use of voltage regulators, which in turn adds extra complexity in terms of both space and power consumption. The design outlined in [6] utilized only two CLS stages, linking the first one to a higher voltage via a diode connected NMOS transistor, this approach eliminates the necessity for intermediate supply voltages.

This design does not attain high-speed performance. As a result, there is an urgent requirement for a dependable, speedy, and energy-efficient circuit design to ensure the robustness of low-power designs. Design presented in [7], weakened and mitigated the pull-up network by controlling its currents through the utilization of a current mirror, this approach accomplishes an extensive operational range but comes at the cost of significant quiescent current dissipation. As we are aware the quiescent current is a vital parameter in electronic circuits, especially in battery-powered devices or low-power applications, where minimizing power consumption during standby or idle modes is essential for extending battery life or reducing overall power usage, therefore design presented in [8] managed to avoid this significant static current by implementing a level shifter based on the Wilson current mirror.

This design boosts energy efficiency by ceasing the flow of current as soon as the desired output level is attained. Nevertheless, the mechanism involving negative feedback introduces a delay in charging the output node, consequently impacting operational speed and dynamic power dissipation. Additionally, for a high V_{IN} level, the output node of the current mirror is left floating, leading to a notable adverse effect on the output buffer. Some modified designs based on the Wilson current mirror have been suggested as well, but these changes only offer slight improvements in terms of delay and power consumption [9], [10].

In this paper, we implement a highly efficient voltage level shifter using Wilson current mirror with Gate Driver that is intended to be used in the battery charger chip. that can notably reduce time delay, total area and we conducted a comparison between our advanced LS with other studies [11]–[16], that delve into the application of level shifters across various domains, each characterized by varying propagation delays that ultimately influence the speed. In this work, we present an optimized LS-GD implementation in TSMC 130 nm CMOS that simultaneously improves three key metrics: i) propagation delay (reduced by 40%), ii) transition time (61% faster), and iii) layout area (92% smaller), with extremely short and negligible differences between the rise transition time and fall transition time which give us a very stable circuit. In this paper, a pre-driver stage is employed to minimize signal propagation delay by carefully selecting both the number of inverter stages and the optimal transistor sizing ratios at each stage.

The remainder of this article is organized as follows: section 2 briefly introduces the battery charger's key functional blocks. Section 3 presents the comprehensive theoretical basis and design details of the proposed level shifter-gate driver (LS-GD) circuit. Section 4 discusses simulation results and comparisons with prior work. Finally, section 5 concludes the study.

2. BATTERY CHARGER ARCHITECTURE OVERVIEW

Lithium-ion battery charger architecture comprises multiple functional blocks organized into four critical subsystems, as illustrated in Figure 1. include power management, control, sensing, and signal interfacing circuits. This modular design ensures three key operational requirements: safe charging conditions, high power conversion efficiency, and optimal performance across all charging phases. Each subsystem addresses a core functional requirement:

a. Power management:
   – LDO regulator [17]: provides stable low-voltage supply for control circuits with minimal dropout.
   – Bootstrap circuit [18], [19]: generates gate-drive voltages above the main supply rai l.
b. Control:
   – Direct current control (DCC) [20]: maintains constant-current charging during initial phases.
   – Direct voltage control (DVC) [21]: regulates voltage during final charging stages.
c. Sensing:
   – Current sensing circuit (CSC) [22]: accurately monitors charging current for system feedback.
d. Signal interfacing:
   – Level shifter (LS) [11]–[16], [23]–[26]: translates signals between different voltage domains.
   – Gate driver (GD) [27]: drives power switches with sufficient current for fast transitions.
   – Power MOSFETs [28]: efficiently handle high-current switching.

While all subsystems are essential for charger operation, this work specifically targets the co-design of the level shifter–gate driver (LS-GD) pair due to its critical influence on system performance. The LS-GD interface governs timing precision through propagation delay, power efficiency via switching losses, and integration density through layout area constraints. Power management, control, and sensing subsystems employ conventional designs. They are presented here to provide architectural context. Section 3 details the proposed level shifter design, while Section 4 presents the LS-GD co-optimization methodology with an emphasis on optimizing speed, area, and energy performance.

3. PROPOSED DESIGN

This section details the design methodology of the proposed level shifter, including its functional architecture, timing analysis, and transistor sizing strategy to achieve high-speed and energy-efficient operation.

3.1. Circuit architecture

This paper presents a high-speed, energy-efficient level shifter architecture developed for robust voltage domain interfacing. As illustrated in Figure 3, the proposed design is composed of three main functional blocks: a pre-driver stage, an anti-cross conduction logic circuit, and a push-pull output stage. The pre-driver consists of two inverter gates that sharpen transitions and provide proper signal conditioning from the low-voltage logic domain (1.8 V). The anti-cross conduction circuit, based on an AND gate and controlled transistors, ensures that the two output transistors are never ON simultaneously, thereby avoiding shoot-through currents. A small capacitor C1 is connected to the logic gate to assist in the timing and stabilization of the anti-cross conduction behavior. The output stage is formed by transistors M2 (PMOS) and M5 (NMOS), which operate in a complementary push-pull configuration to drive the output node (OUT_VCC) with a full swing at high voltage (5 V).

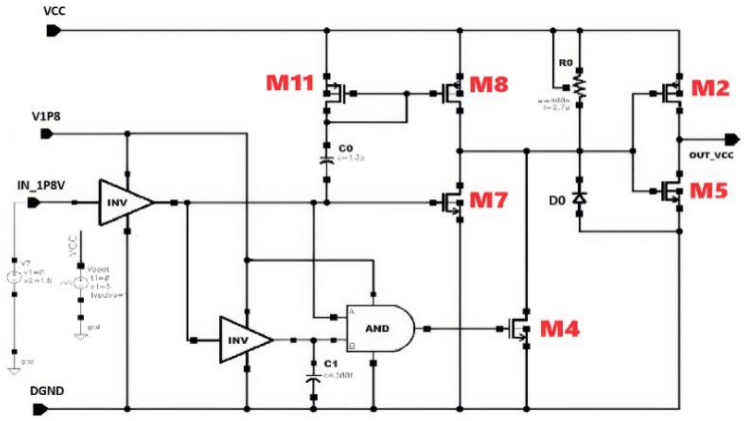

Figure 3. The circuit diagram of developed level-shifter under cadence tool version

More specifically, the level shifting function is achieved through four key transistors M4, M7, M8, and M11 along with a resistor R0 and capacitor C0. M4 and M7 are NMOS devices that contribute to pulling down the intermediate nodes, while M8 and M11 are PMOS devices responsible for pulling them up. During a high-to-low input transition, the signal is coupled through C0 to discharge the Vg11 node, which activates M8 and causes R0 to pull the Vg5 node up. Conversely, during a low-to-high transition, M7 turns ON and pulls the Vg5 node down, turning M8 OFF. A diode D0 is connected between Vg5 and DGND to provide simple protection against excessive negative gate-to-source voltage on M5 during switching, particularly when DGND rises faster than Vg5.

The circuit operates under dual supply voltages: V1P8 (1.8 V) for the logic level and VCC (5 V) for the output stage. The transistors M2 and M5 must be designed as high-voltage devices capable of withstanding 5 V without performance degradation. If low-voltage transistors are used instead, M7 must be upscaled significantly (*e.g.*, ×20) to ensure reliable switching, which increases chip area and adversely affects delay and power performance. Having described the functional structure and sizing strategy of the proposed level shifter, the next step is to examine its dynamic behavior. We focus on analyzing the propagation delay, which is a critical performance metric in voltage-level translation circuits.

3.2. Propagation delay analysis

Propagation delay represents the time required for a signal to travel from the input of the circuit to the output node. In the context of level shifters and gate drivers, minimizing this delay is essential to ensure rapid and reliable switching, especially when driving large gate capacitances in power transistors.

The propagation delay T_P is influenced by several factors:

- The total load capacitance seen by the switching node
- The drive current of the transistors

- The overdrive voltage ($V_{gs} - V_{th}$)
- The technology parameters ($\mu_{n,} C_{ox}$)

The relationship between these factors can be expressed as (1):

$$T_P = \frac{C_{total}}{I} \quad (1)$$

where C_{total} includes the gate capacitance of the driven transistors (M2 and M5), interconnect parasitic, and intrinsic capacitances in the level shifter path. The current I, for a transistor operating in saturation, is given by (2):

$$I = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2 \quad (2)$$

where:

- μ_n is the mobility of the charge carriers
- C_{ox} is the oxide capacitance per unit area
- W and L are the width and length of the transistor
- V_{gs} is the gate-source voltage
- Vth is the threshold voltage

Substituting (2) into (1) leads to:

$$T_P = \frac{C_{total}}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - Vth)^2} \quad (3)$$

This highlights that propagation delay decreases with larger transistor widths (W) and stronger gate overdrive ($V_{gs} - Vth$), both of which are part of transistor sizing. On the other hand, the delay increases with longer channel lengths (L) and higher capacitive loads. These dependencies must be carefully balanced during design to optimize performance.

3.3. Transistor sizing and optimization

Transistor sizing is one of the most critical aspects in designing high-speed, low-power level shifters. The dimensions of the transistors directly impact the charging and discharging paths of intermediate nodes, thereby influencing the overall speed, power consumption, and reliability of the circuit. Table 1 summarizes the transistor dimensions selected for the optimized level shifter.

Table 1. Transistors sizes for the optimized level shifter

Transistors names	Length	Width
PMOS (M11, M8)	130 n	2 u
PMOS HV M2	500 n	1.9 u
NMOS (M4, M7)	130 n	2 u
NMOS HV M5	740 n	600 n

The level shifter transistors M4, M7, M8, and M11 are sized with minimum channel lengths (130 nm) and moderate widths (2 µm) to ensure low delay and balanced current drive. The high-voltage transistors M2 and M5 are specially sized to handle 5 V operation: M2 uses a longer channel for reliability, while M5 is heavily upscaled to drive large capacitive loads without timing degradation.

It should be noted that aggressively minimizing transistor widths can reduce area but may introduce layout constraints. For example, excessively narrow transistors may result in single-contact source/drain regions, which are generally avoided due to higher parasitic resistance and lower reliability. Thus, transistor dimensions must be chosen carefully to balance delay, area, and manufacturability.

4. SIMULATION RESULTS AND DISCUSSION

Following the careful sizing and optimization of transistors described in section 3, this section presents the simulation results, implementation insights, and performance comparison of the proposed level shifter and integrated gate driver. All simulations were conducted using the Cadence Virtuoso tool and TSMC 130 nm CMOS technology.

4.1. Transient analysis of the proposed level shifter

Figure 4 presents the transient simulation demonstrates a successful logic level shifting from 1.8 to 5 V. The measured propagation delays are: i) tp1=0.08897 ns (low-to-high transition) and ii) tp2=0.09062 ns (high-to-low transition). These nearly identical values confirm that the circuit exhibits symmetrical switching behavior and stable performance.

Having validated the timing performance of the level shifter through transient simulation, the next step involves the design of an efficient gate driver. This component is critical for delivering the necessary current to switch power MOSFETs rapidly and reliably, thus playing a vital role in overall system efficiency and speed.

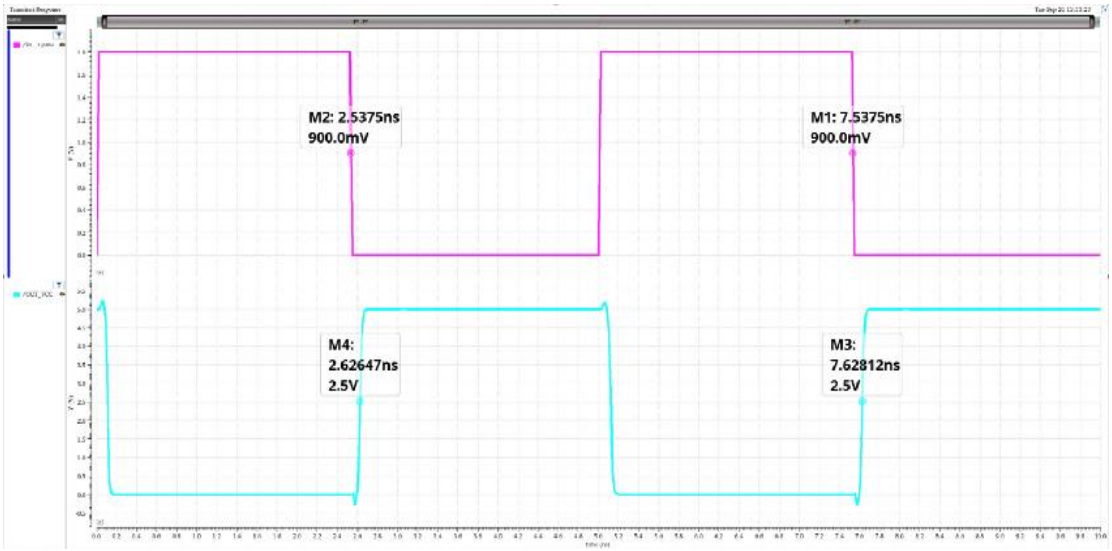

Figure 4. Transient analysis result of the proposed level-shifter

4.2. Gate driver design

The gate driver plays a pivotal role in controlling the switching behavior of the power MOSFET. Its primary function is to quickly charge and discharge the gate capacitance of the power transistor, ensuring fast switching and minimizing power losses. The proposed gate driver, shown in Figure 5, is designed to efficiently deliver high-speed operation. The design consists of 18 transistors (9 PMOS and 9 NMOS), with the NMOS M167 transistor having a wider channel to handle larger currents during the discharge phase.

Table 2 provides the transistor dimensions selected for the gate driver design. These sizes were chosen to provide strong drive strength, balanced switching characteristics, and to minimize gate delay while ensuring the layout remains compact.

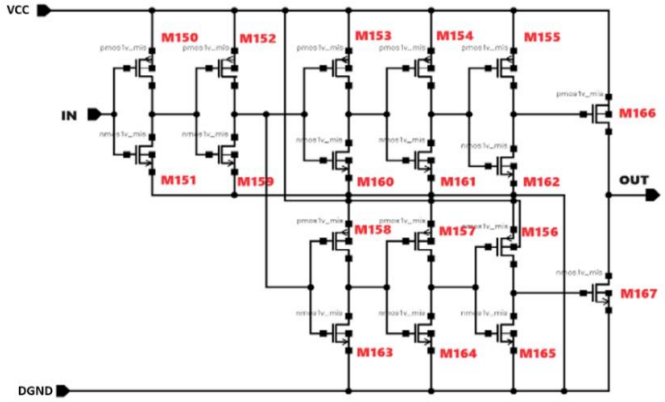

Figure 5. The circuit diagram of developed gate driver under cadence tool version

Table 2. Transistors sizes of proposed gate driver

Transistors names	Length	Width
PMOS (M150, M152, M153, M154, M155, M156, M157, M158, M166)	130 n	740 n
NMOS (M151, M159, M160, M161, M162, M163, M164, M165)	130 n	740 n
NMOS M167	130 n	1.7 u

Once the gate driver was designed and optimized for high-speed operation, it was integrated with the level shifter to form a complete voltage interface. This combined architecture enables both accurate logic level translation and strong gate-driving capability, which are essential for controlling power switches in Li-ion battery charging circuits.

4.3. Level shifter with gate driver

To validate the functionality of the complete interface, the level shifter was integrated with the previously developed gate driver. The combined architecture ensures both voltage level translation and strong current delivery for efficient gate control of the power MOSFET. Figure 6 presents the full schematic of the integrated level shifter and gate driver. In this design, the level shifter converts a 1.8 V control signal into a 5 V output, which is then amplified by the gate driver to deliver sufficient current to the gate of the power transistor.

The effectiveness of this design is confirmed through transient simulation results, presented in Figure 7. The circuit successfully shifts the 1.8 V logic signal to a stable 5 V output. The measured propagation delay is 0.20468 ns, indicating high-speed operation suitable for modern power management systems. To further evaluate switching performance, Figure 8 illustrates the rise and fall times observed at the output node. The rise time is approximately 0.0145 ns, while the fall time is around 0.0139 ns, confirming that the circuit operates with excellent timing characteristics and fast transitions.

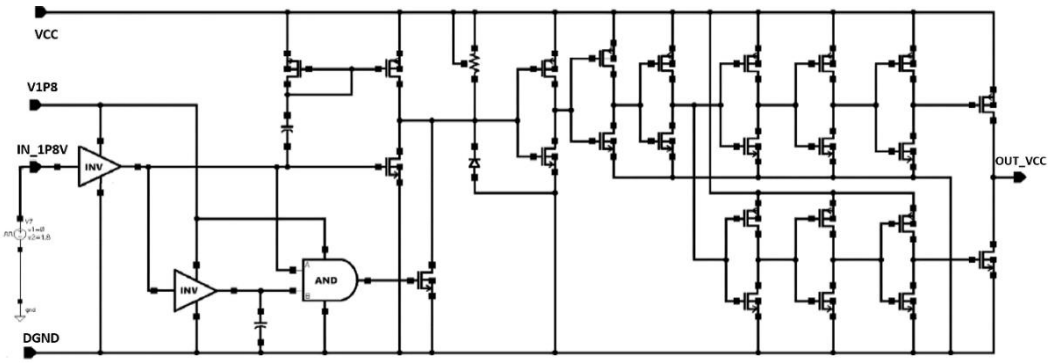

Figure 6. The circuit diagram of the developed level-shifter with date driver

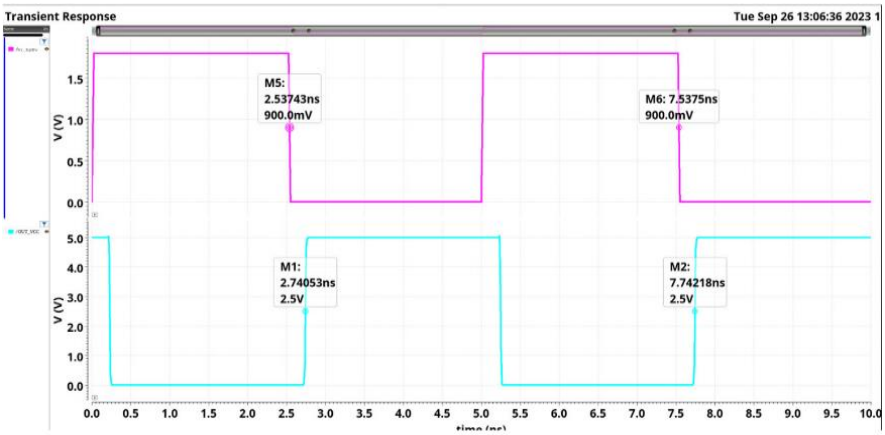

Figure 7. The transient analysis result of the developed level-shifter with date driver

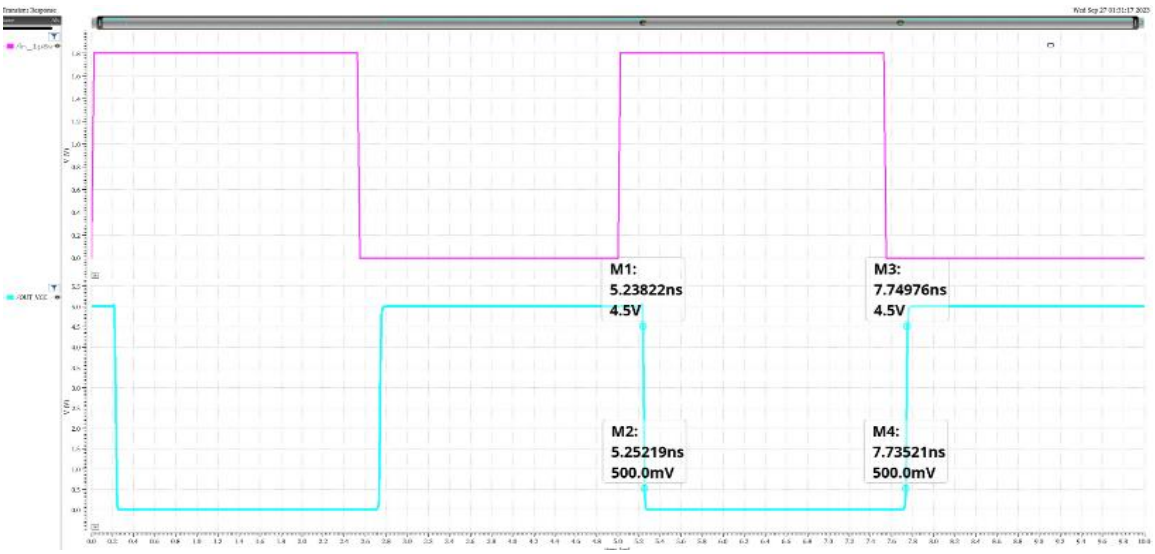

Figure 8. The simulation results of rise and full time

These results validate the effectiveness of the proposed design in performing low-to-high voltage translation with excellent high-speed characteristics. Overall, the architecture provides: i) the accurate level shifting from 1.8 to 5 V, ii) sub-nanosecond propagation delay, and iii) balanced rise and fall times, minimizing signal distortion.

Such performance is particularly valuable in battery charger systems where speed, efficiency, and reliability are essential. Moreover, the successful integration of the gate driver demonstrates the scalability of the design for full SoC integration. Following the successful simulation of the integrated level shifter and gate driver, the circuit was translated into a physical layout. This step ensures manufacturability and enables further evaluation of area usage and parasitic effects.

4.4. Layout

The layout of the proposed level shifter with integrated gate driver was implemented in Cadence Virtuoso. The design includes floorplaning, device placement, and metal routing, while ensuring compliance with design rules and foundry constraints to ensure functionality and manufacturability.

Figure 9 presents the final layout of the proposed level shifter integrated with the gate driver. The design prioritizes compact area, signal integrity, and minimal parasitic effects. The layout underwent a complete verification flow, including design rule check (DRC), layout versus schematic (LVS), antenna rule checks, metal density, manufacturing rule check (MRC), and design for manufacturability (DFM). All checks passed successfully, confirming the correctness and reliability of the layout. The total silicon area occupied is 15.13×25.83 µm, which demonstrates an efficient use of space and makes the design well suited for integration into larger system.

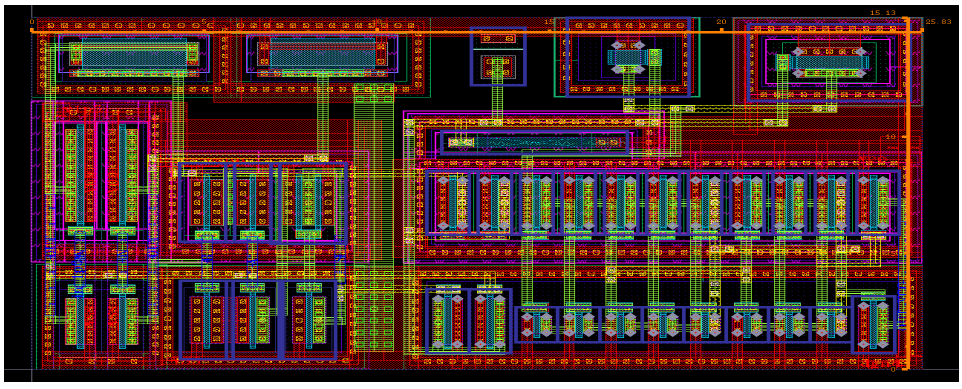

Figure 9. The layout of the proposed level-shifter with gate-driver

4.5. Comparison with literature

Following the physical layout and validation of the integrated level shifter and gate driver, a comparative analysis was conducted to evaluate the performance of the proposed design against recent works. Table 3 summarizes the technology nodes, voltage ranges, and delay times. Our design, implemented in 130 nm CMOS, achieved a propagation delay of 0.09 ns, establishing a new performance benchmark and significantly outperforming several reported designs across various technology nodes. For example, Alaoui *et al.* [11] (180 nm) reported a delay of 0.15 ns, while Zhao *et al.* [12], using the same 130 nm process, achieved 1.51 ns. Designs based on more advanced technologies, such as Shukla *et al.* [13] (65 nm) and Saurab and Chavan [15] (7 nm), reported delays of 0.63 and 1.88 ns, respectively. The slowest performance was observed in Gosatwar and Ghodeswar [14] (90 nm) with 10.99 ns, whereas Chatterjee and Ruckert [16] (28 nm) reported a delay of 3.11 ns. These results demonstrate that performance is not solely determined by technology scaling. Optimizing transistor sizing and design methodology is key to achieving superior performance.

Table 3. Comparative analysis of the proposed level shifter versus existing designs

Design	Technology	Low voltage	High voltage	Delay time [ns]
This proposed design	130 nm	1.8 V	5 V	0.09
Alaoui *et al.* [11]	180 nm	1.8 V	5 V	0.15
Zhao *et al.* [12]	130 nm	1.8 V	5 V	1.51
Shukla *et al.* [13]	65 nm	1.2 V	6 V	0.63
Gosatwar and Ghodeswar [14]	90 nm	0.2 V	1 V	10.99
Saurab and Chavan [15]	7 nm	0.19 V	1.5 V	1.88
Chatterjee and Ruckert [16]	28 nm	0.25 V	1 V	3.11

5. CONCLUSION

This paper presented an optimized voltage level shifter tailored for Li-ion battery charging applications. The design focused on three key performance metrics: propagation delay, rise/fall transition time, and circuit area, all of which contribute to improving overall system efficiency and reducing cost. The proposed architecture achieves a significant reduction in propagation delay, from 0.15 to 0.09062 ns, and delivers nearly symmetrical rise and fall times of 0.014 ns, compared to 0.036 ns in conventional designs. The entire circuit was implemented using TSMC 130 nm CMOS technology, and all simulations and layout work were performed using the Cadence Virtuoso design environment. These results confirm the suitability of the design for integration into modern, high-efficiency battery charger systems and underscore its potential for full SoC integration. The design achieved improvements of 40% in delay, 61% in transition time, and a 92% reduction in layout area, highlighting the effectiveness of the proposed optimization strategy.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Hicham Guissi	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
Khadija Slaoui		✓				✓	✓	✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Derived data supporting the findings of this study are available from the corresponding author, HG, on request.

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