International Journal of Electrical and Computer Engineering (IJECE)
Vol. 15, No. 5, October 2025, pp. 4993~5002
ISSN: 2088-8708, DOI: 10.11591/ijece.v15i5.pp4993-5002

Field-programmable gate array-based voltage-feedback-driven battery charging with DC-DC buck converter

Afarulrazi Abu Bakar[1], Suhaimi Saiman[1], Tharnisha Sithananthan[1], Muhammad Nafis Ismail[1], Saidina Hamzah Che Harun[2]
[1]Department of Electrical Engineering, Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Johor, Malaysia
[2]Magnitude Power Sdn Bhd., Selangor, Malaysia

Article Info

Article history:

Received Sep 8, 2024
Revised May 28, 2025
Accepted Jun 30, 2025

Keywords:

Buck converter
DC charger
Field-programmable gate array
Pulse-width modulation
Voltage feedback

ABSTRACT

This paper presents the design and development of a reference-driven field-programmable gate array (FPGA)-based controllable battery charging system featuring a buck converter. The controller tracks and adjusts the system's duty cycle based on output voltage feedback. The primary goal was to introduce a digital pulse-width modulation generator program using a hardware description language within a feedback loop. To enhance the buck converter's accuracy, the system's switching frequency was set to 20 kHz with an 8-bit counter, achieving a resolution of 0.390625% per clock cycle. An 8-bit parallel analog-to-digital converter provided feedback by measuring the output voltage and comparing it with the reference setpoint. The simulation model was developed using MATLAB/Simulink, while the Quartus II software was employed for controller programming. The resultant data was meticulously analyzed to assess the circuit's performance across various voltage and control parameters. To validate the proposed controller's effectiveness, a 400 W system prototype comprising a step-down transformer, rectifier, and buck converter was constructed and tested for voltage ranging from 24 to 72 V. Through FPGA-based digital control, this system demonstrated a voltage regulation accuracy of ±0.39 per clock cycle and the capability to continuously track and regulate the duty cycle with each clock trigger, ensuring precise control over the charging process.

Corresponding Author:

Suhaimi Saiman
Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia
Johor, Malaysia
Email: suhaimis@uthm.edu.my

1. INTRODUCTION

The diverse topologies of DC-DC converters have been intensively studied and widely used in several applications, such as battery chargers [1], renewable energy [2], electric vehicles [3], portable devices [4], and lighting systems [5]. It is also driven by the development of renewable energy and government initiatives that raise awareness about maintaining environmental sustainability [6]. The fascinating demand for higher direct current (DC) power has introduced new power electronic devices, such as gallium nitride (GaN), which are capable of providing more advantages over silicon-based devices [7], [8]. The fundamental goal of DC-DC converters is to provide an adequate amount of voltage to a load within the specified operational range [9], [10]. Trends, standards, and compliance are shaping the future of power electronics converters, driving innovations that result in lower cost, higher efficiency, higher power density, more compact size, and more versatile power conversion solutions for various industries and applications [11].

The development of controllers is indeed aligned with advancements in new power electronics switching devices, ensuring that the full potential of the technologies is realized in practical applications. Pulse-width modulation (PWM) switching is one of the important control techniques for controlling PWM converters to increase efficiency [12]. PWM switching is commonly implemented using microcontrollers [13], digital signal processors (DSPs) [13], field-programmable gate arrays (FPGAs) [14], application-specific integrated circuits [15], and analog controllers. Controller selection varies based on complexity, required precision, and application. DSPs are commonly used for systems that require solving complex mathematical operations and high-speed numerical processing [16]. On the other hand, FPGAs are commonly used for operations with high switching frequency and have the ability to handle multiple operations simultaneously. Therefore, the switching controller should be correctly chosen to match the power electronic devices used in order to achieve the desired response.

Nowadays, most controllers are implemented based on a DSP and an FPGA to leverage both technologies' strengths. FPGAs have been proven to provide a high-speed control system and flexibility in custom applications, which can be easily reconfigured [17]. Recent efforts in FPGA-based converters have shown promising advancements in battery management for electric mobility and solar energy [18], [19]. Studies, such as study [20] emphasized adaptive digital PWM strategies, highlighting the increasing relevance of real-time configurability in low-voltage, high-efficiency systems. FPGAs have also been widely used for switching in various kinds of converters, such as rectifiers (AC-DC) [21], DC choppers (DC-DC) [22], [23], cyclo-converters (AC-AC) [24], and inverters (DC-AC) [14], [25]. Battery charging systems using DC-DC converters are used to regulate the output voltage and control the charging current [26]. To increase effectiveness, it must be intelligent, sensitive to the battery's health, and satisfy a variety of demands, especially when it comes to current ripples in the battery mode of float charging, for efficient charging and power distribution [27]. Engineers are researching new methods and techniques to boost charging rates without harming the condition of batteries [28].

This research proposes a digital PWM based on voltage feedback, which is implemented in a DC-DC buck converter fed from a rectifier circuit. The proposed digital PWM technique can be applied in other PWM DC-DC converters by adapting the specifications of the input, output, frequency, accuracy, and response time. The key contributions of this research include the implementation of a reference-driven PWM controller using an 8-bit ADC for real-time feedback, integration of a digital control loop into an FPGA platform for fine voltage adjustment, and comprehensive validation through analysis of both simulation and experimental findings to emphasize the controller's suitability for precision battery charging systems. The DC output voltage can be adjusted based on the given reference or set point, and automatically match the programmed PWM, which is facilitated by the voltage and current feedback assigned. The controller's control algorithm is programmed using a hardware description language, which can ultimately allow for the implementation of hardware designs at various levels of abstraction.

The rest of the manuscript is organized as follows: section 2 consists of the research methodology of the proposed system. In section 3, the results and detailed analysis of the experimental assessments of the research are documented. In section 4, the overall manuscript is concluded.

2. RESEARCH METHOD

The parameters of the critical components required for this proposed system were calculated in order to ensure proper functionality and the desired performance. The MATLAB/Simulink software was used for circuit modelling and verification. The charging performance was verified, potential errors were identified, and necessary adjustments were made to achieve the desired output. In addition, hardware implementation was carried out based on the specified parameters. The values of the critical components in the buck converter were chosen to be much greater than the calculated values to ensure the converter operated in a continuous conduction mode, even though the duty cycle changed. Based on the hardware implementation, testing was conducted to ensure the circuit met the requirements and performed effectively.

2.1. Proposed circuit block diagram

In the proposed setup, the AC power source was first connected to a 3 kVA step-down transformer, which reduced the voltage before it was fed into the bridge rectifier circuit, as illustrated in Figure 1. The rectifier consisted of four diodes arranged in a bridge configuration, enabling the conversion of alternating current (AC) to pulsed direct current (DC). These diodes ensured that current flowed in only one direction, resulting in a consistent positive voltage output. The diode also played a key role in maintaining the flow of current through the inductor and preventing potential damage caused by reverse current.

A buck converter was integrated into the system to further control the voltage and reduce it to the appropriate level required for battery charging. This converter played a key role in ensuring that the power supplied to the battery was efficient and within safe operating limits. An FPGA was used as the control unit, precisely adjusting the duty cycle of the buck converter to maintain optimal charging conditions. To monitor the system performance, an 8-bit parallel analog-to-digital converter (ADC) and a current sensor were used to track the voltage and current in real-time. This coordinated approach aimed to improve power conversion efficiency, support longer battery life, and improve overall system reliability.

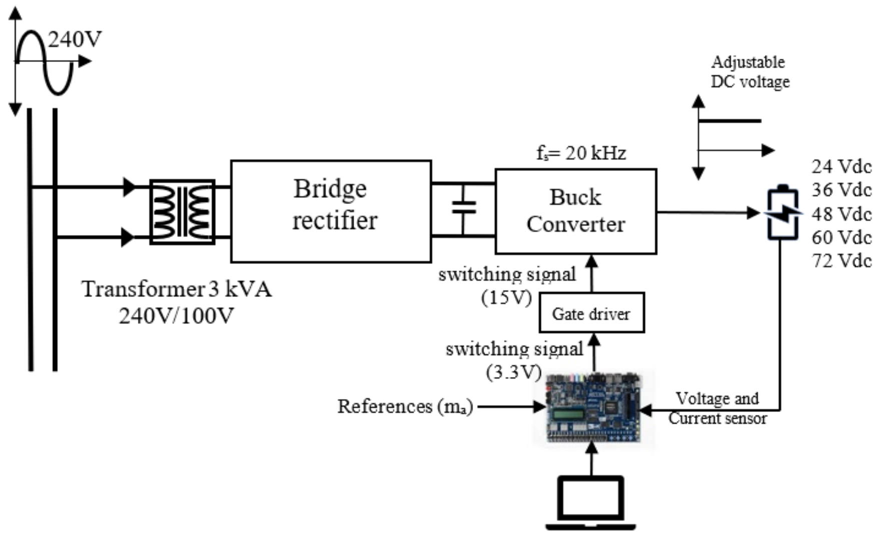

Figure 1. Proposed system’s block diagram

2.2. Circuit simulation using MATLAB/Simulink software

The charging circuit shown in Figure 2 initiates with a supply voltage of 240 V_{AC} at a frequency of 50 Hz. The supplied voltage was then reduced to 100 V_{AC} through the aid of a step-down transformer. The voltage of 100 V_{AC} was then passed through a bridge rectifier to convert the AC voltage into a pulsating DC voltage. A capacitor was then connected to filter out AC ripples and obtain an unregulated filtered DC signal. The buck converter was connected after the rectifier to produce an output voltage lower than the input voltage by controlling the switching of its components.

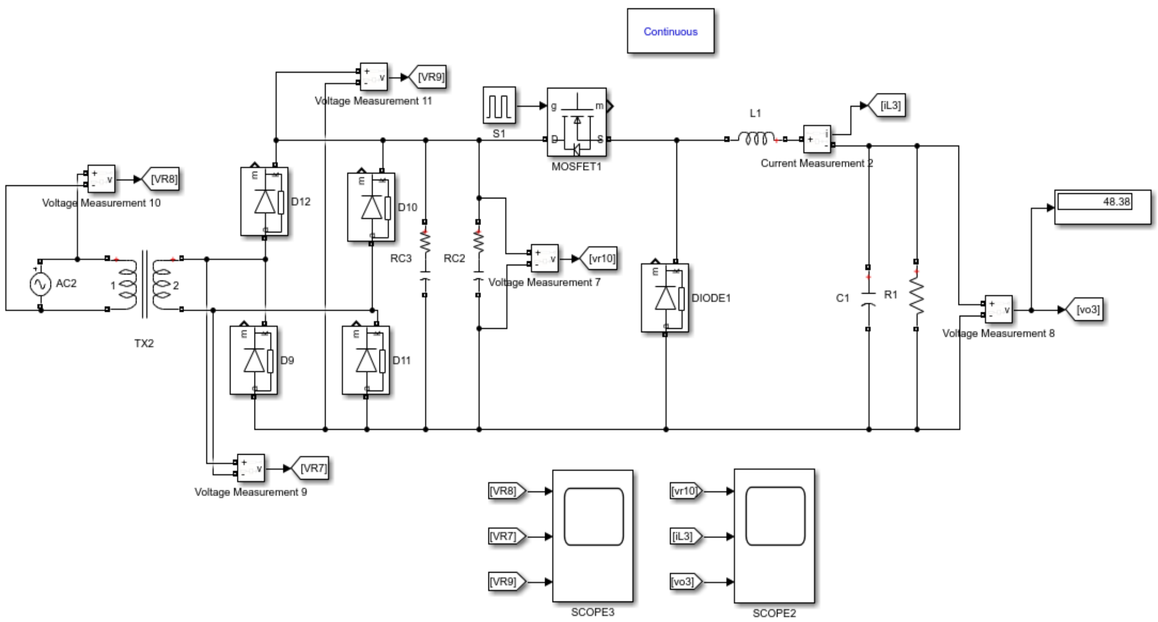

Figure 2. Diagram of circuit simulated using MATLAB/Simulink software

2.3. Control algorithms

The flowchart presented in Figure 3 illustrates the process of a PWM generator that operates based on reference-driven feedback. During the initialization stage, the comparator reads the setpoint value "A". It generates an initial PWM signal "X" using a control algorithm. The feedback from the ADC labelled "B" is continuously updated with each clock trigger. The comparator compares the feedback signal to the setpoint value "A". If the feedback signal is greater than the setpoint value, the PWM signal is adjusted by -1, and if the feedback signal is less than the setpoint value, the PWM signal is adjusted by +1. A new PWM signal, "X", is generated after the adjustment. This iterative process ensures that the PWM signal is continuously adjusted to match the desired setpoint value by comparing the feedback signal and making the necessary corrections. Figure 4 shows the digital representation of the PWM signal generator based on the flowchart.

Figure 5 illustrates the block diagram file (*.bdf) for reference-driven PWM control signal generation. The input clock, sourced from the FPGA board's 50 MHz internal clock, was divided into 25 MHz and 5.12 MHz frequencies using a phase-locked loop. The 25 MHz output was connected to the *clk_div* function, providing multiple clocks for ADC and triggering circuits, while the 5.12 MHz output was connected to the *lpm_counter* function to generate a 20 kHz frequency for the PWM signal. The *lpm_counter* would count up to 256, with each clock cycle representing a 0.390625% duty cycle. The comparator compared the reference signal with the ADC input to produce the signals. A parallel flash 8-bit ADC (ADC0804LCN) was used to read the current output voltage and convert it into a digital signal, with each bit corresponding to 0.01953125 V (5/256). The input references and ADC values were decoded to their actual values, ensuring that there was no offset.

The comparator's output was compared with the digital sawtooth signal from the *lpm_counter* to generate the PWM signal. This signal continuously was adjusted based on the reference and output voltage (ADC) during each clock cycle assigned to the comparator. The response time of the ADC (write) and comparator can be adjusted within the clock assigned.

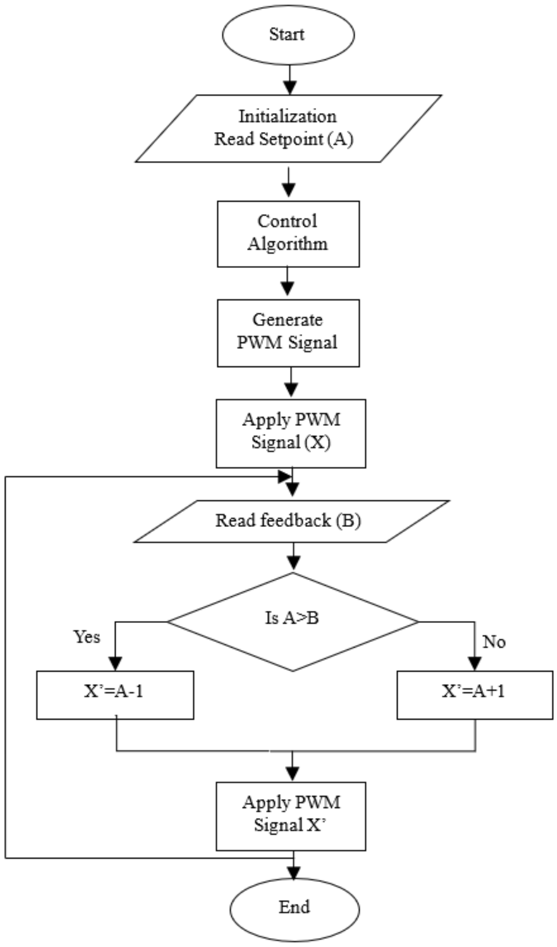

Figure 3. Flowchart of control algorithm

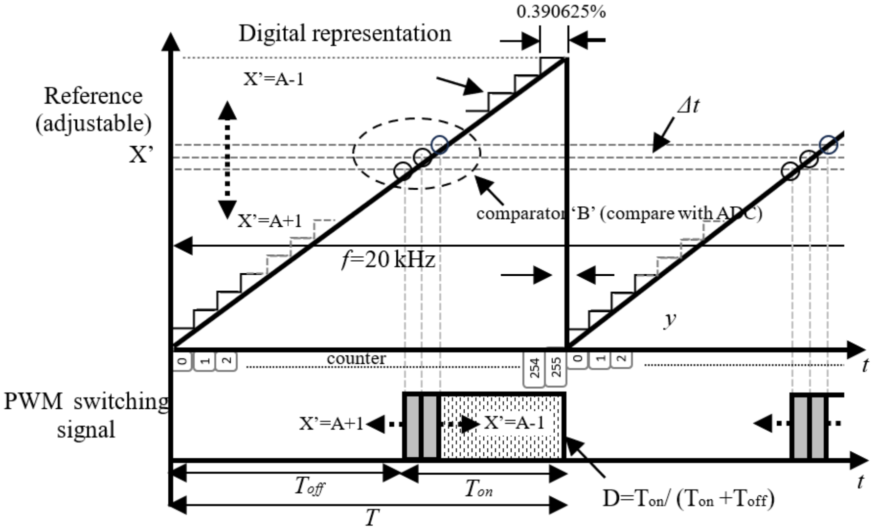

Figure 4. Digital representation of digital-PWM-based reference-driven system

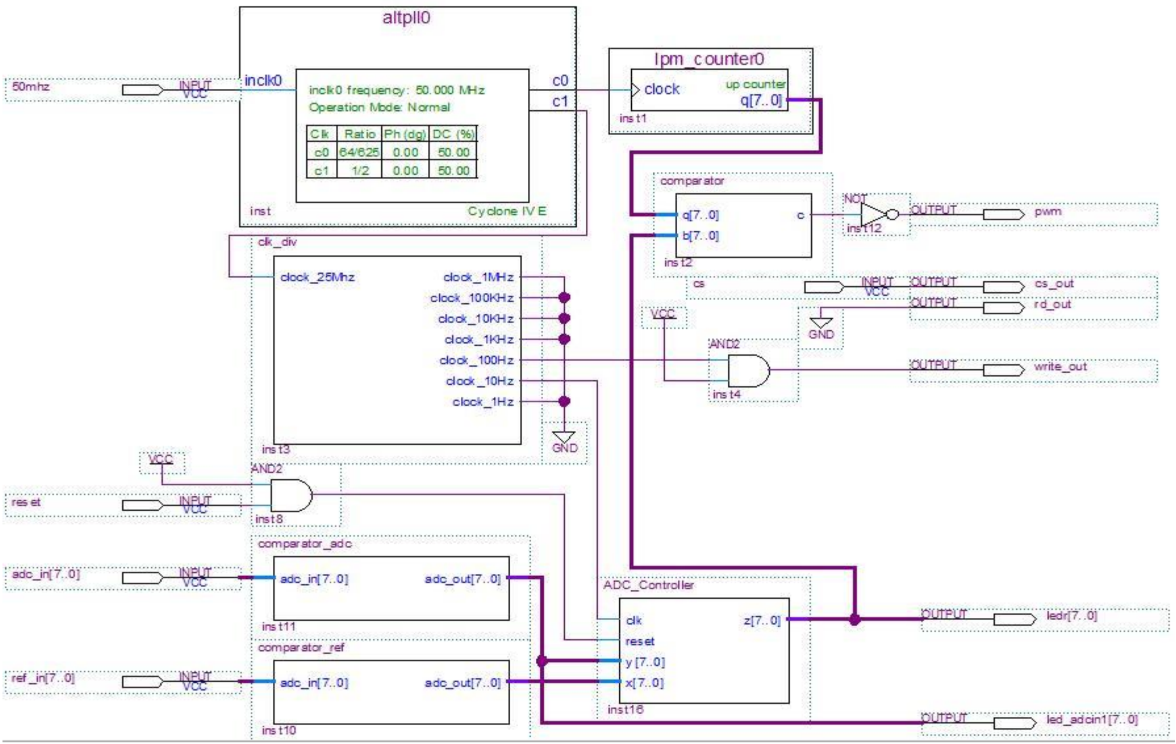

Figure 5. Block diagram file (*.bdf) for PWM generator

2.4. Experimental setup

Figure 6 depicts the complete connection of components in the proposed charging system. The FPGA enabled precise modulation of the buck converter's output voltage. A 3 kVA 230/110 V aluminum-winding dry-type step-down transformer complete with an IP21 enclosure, was used to step down the input voltage. Smoothing capacitors were used to filter DC voltage, hence removing ripples and providing a more consistent power supply. Inductors were used to control current fluctuations and optimize the charging process. The MOSFETs acted as high-speed switches in the buck converter, efficiently converting voltage and regulating output. Gate drivers controlled the MOSFETs' switching behavior, allowing for precise control of the on and off states. These components and their functions aimed to contribute to an efficient and reliable battery charging system. The circuit was tested to verify if the expected results were achieved.

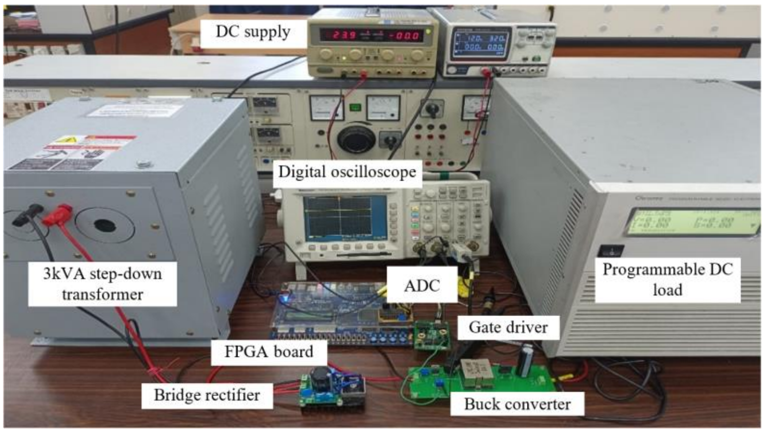

Figure 6. Experimental prototype

3. RESULTS AND DISCUSSION

A comparison and analysis of the simulation and experimental findings were conducted to validate the outcome of the proposed system.

3.1. Software simulation

The circuit's waveforms and characteristics were analyzed under various conditions through software simulation using the MATLAB/Simulink software. The simulation results, depicted in Figure 7 and Figure 8 show the waveform variations. Figure 7(a) illustrates the sinusoidal waveform of the input voltage, peaking at 340 $V_{pk\text{-}pk}$, which subsequently underwent a step-down transformation to 100 V via the transformer, as shown in Figure 7(b). The filtered output waveform, displayed in Figure 7(c), exhibits minor ripples attributed to residual AC components post-rectification. This simulation output vividly illustrates the conversion of AC voltage to pulsating DC voltage through the step-down and rectification processes.

On the other hand, Figure 8 presents waveforms measured during the buck converter's operation. A capacitor was employed to mitigate voltage pulsations and smooth the output. Figure 8(a) depicts the duty cycle waveform, controlled by PWM to achieve the desired output voltage level. Figure 8(b) illustrates the measured inductor current charging and discharging, which indicates a continuous conduction mode of operation. Figures 8(c) and 8(d) showcase the DC output (charging voltage) and input (from the rectifier), respectively. These findings validate the efficient performance of the buck converter in filtering the DC voltage, controlling the duty cycle, maintaining a continuous inductor current, and regulating the output voltage.

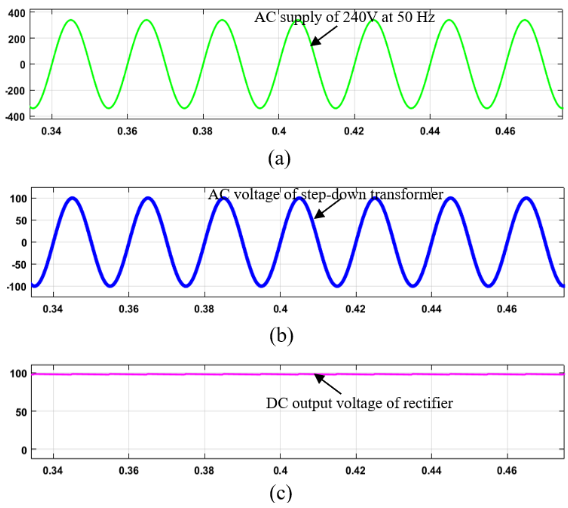

Figure 7. Simulation results measured from rectifier side: (a) AC supply, (b) AC secondary transformer voltage, and (c) output voltage from rectifier

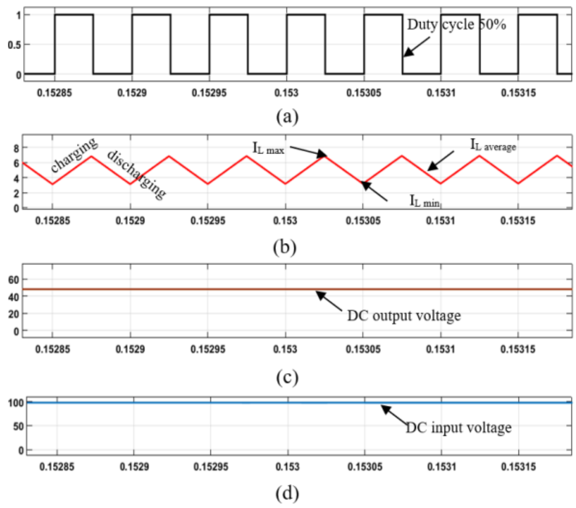

Figure 8. Simulation results measured from DC-DC side: (a) duty cycle, (b) inductor current, (c) DC output voltage, and (d) DC input voltage from rectifier

3.2. Experimental analysis

The experimental analysis of the buck converter demonstrated that, by adjusting the duty cycle of the PWM signal, the output voltage can be effectively regulated. Increasing the duty cycle raised the output voltage; while decreasing it lowered the voltage. Simulation results indicated that higher duty cycles enhanced efficiency and improved power delivery to the load. Figures 9 and 10 present the measured outputs of the proposed system using a TDS 3024B oscilloscope.

Figure 9 shows the waveform of the supplied voltage, which was 240 V_{AC} at a frequency of 50 Hz, along with the stepped-down and smoothed DC voltage measured at the rectifier's output. Figure 10 shows the measured voltage and current waveforms at the buck converter with a 40% duty cycle. The inductor current exhibited a typical sawtooth pattern corresponding to the PWM switching duty cycle, which was critical in transferring and regulating energy from the input to the output. The resulting output voltage was a regulated DC voltage suitable for battery charging.

The PWM switching technique was employed to adjust the average value of the digital signal by modulating it based on the reference input. A comparative analysis of simulation and experimental results reveals a minor discrepancy in measurement values. This discrepancy can be attributed to losses in hardware implementation, particularly conduction and switching losses associated with the switching devices, as well as the core materials of the inductor, which are termed core losses/iron losses. Despite these differences, the output voltage values remained relatively consistent across various duty cycles. The selected parameters proved to be appropriate for the circuit's intended purpose, as evidenced by the simulation results.

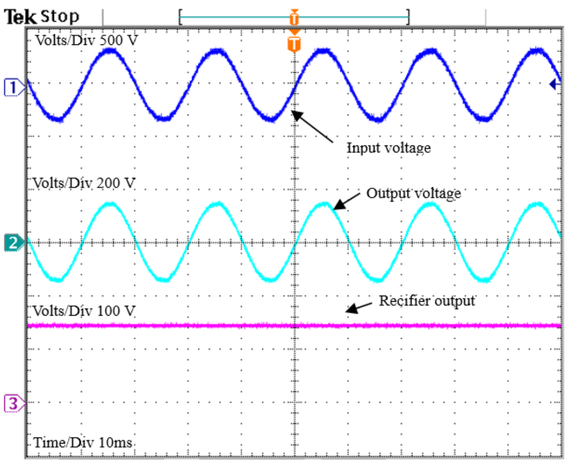

Figure 9. Input voltage, output voltage, and rectifier output

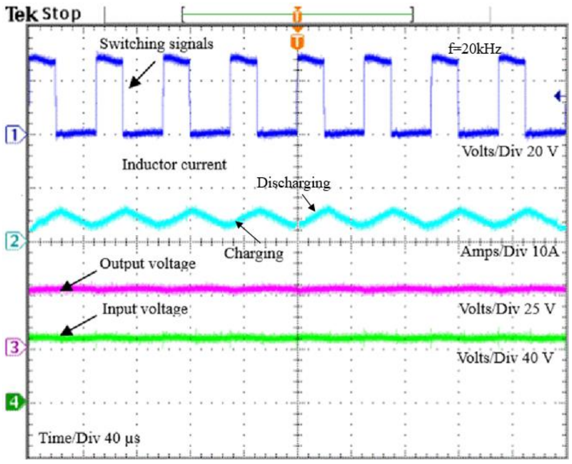

Figure 10. Switching signal, inductor current, output voltage, and input voltage

4. CONCLUSION

In conclusion, this research successfully demonstrated a voltage-driven buck converter through a digital PWM generator on an FPGA. The strength of the control algorithm lies in its ability to regulate the output voltage to within a ±0.39% error margin, and the control algorithm proved its capability through a consistent performance in both simulation and real hardware tests. The error margin can be further reduced by increasing the number of counters in line with the size of the ADC and closely related to the clock generator assigned by maintaining the same proposed digital techniques. The achievements suggest strong potential for deployment in applications that require fast, accurate, low-ripple, and reconfigurable voltage control, especially in battery management systems and renewable energy converters.

FUNDING INFORMATION

This research was supported by Universiti Tun Hussein Onn Malaysia (UTHM) through TIER 1 (Vot Q544) and GPPS (Vot Q325).

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Afarulrazi Abu Bakar	✓	✓	✓	✓	✓			✓	✓		✓		✓	
Suhaimi Saiman	✓	✓	✓	✓	✓			✓	✓		✓	✓	✓	✓
Tharnisha Sithananthan	✓				✓	✓			✓	✓				
Muhammad Nafis Ismail					✓		✓							✓
Saidina Hamzah Che Harun					✓		✓							✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article and its figures. Additional details can be obtained from the corresponding author upon request.

REFERENCES

[1] M. Deepak, G. Janaki, and C. Bharatiraja, "Single phase shift dual active bridge high frequency DC-DC converter for electric vehicle battery charger 6.6 kW," in *2023 5th International Conference on Electrical, Computer and Communication Technologies, ICECCT 2023*, 2023, pp. 1–6, doi: 10.1109/ICECCT56650.2023.10179621.

[2] N. Rahman, U. Aiman, M. S. Alam, M. R. Khalid, A. Sarwar, and M. S. J. Asghar, "A non-isolated DC-DC boost converter with high gain ability for renewable energy sources applications," in *2020 International Conference on Decision Aid Sciences and Application, DASA 2020*, 2020, pp. 137–141, doi: 10.1109/DASA51403.2020.9317225.

[3] S. Yahyazadeh, M. Khaleghi, S. Farzamkia, and A. Khoshkbar-Sadigh, "A new structure of bidirectional DC-DC converter for electric vehicle applications," in *2020 11th Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2020*, 2020, pp. 1–6, doi: 10.1109/PEDSTC49159.2020.9088414.

[4] K. Zhang, "A compact digital-controlled soft-start circuit of DC-DC switching converter for portable devices," in *2022 IEEE 4th International Conference on Circuits and Systems, ICCS 2022*, 2022, pp. 86–90, doi: 10.1109/ICCS56666.2022.9936264.

[5] G. J. Chen and W. H. Chung, "Evaluation of charging methods for lithium-ion batteries," *Electronics (Switzerland)*, vol. 12, no. 19, 2023, doi: 10.3390/electronics12194095.

[6] K. K. Jaiswal *et al.*, "Renewable and sustainable clean energy development and impact on social, economic, and environmental health," *Energy Nexus*, vol. 7, Sep. 2022, doi: 10.1016/j.nexus.2022.100118.

[7] S. Musumeci and V. Barba, "Gallium nitride power devices in power electronics applications: state of art and perspectives," *Energies*, vol. 16, no. 9, 2023, doi: 10.3390/en16093894.

[8] A. Letellier, M. R. Dubois, J. P. Trovao, and H. Maher, "Gallium nitride semiconductors in power electronics for electric vehicles: advantages and challenges," in *2015 IEEE Vehicle Power and Propulsion Conference, VPPC 2015 - Proceedings*, 2015, pp. 1–6, doi: 10.1109/VPPC.2015.7352955.

[9] L. Ashok Kumar, S. Albert Alexander, and M. Rajendran, *Emerging DC-DC converter topologies*. 2020.

[10] A. A. Bakar, T. Sithananthan, S. Saiman, and A. F. H. A. Gani, "Power losses analysis of multiphase interleaved DC-DC boost converter using OrCAD PSpice software," in *2024 IEEE 4th International Conference in Power Engineering Applications: Powering the Future: Innovations for Sustainable Development, ICPEA 2024*, 2024, no. March, pp. 112–116, doi: 10.1109/ICPEA60617.2024.10499116.

[11] S. M. S. H. Rafin, R. Ahmed, M. A. Haque, M. K. Hossain, M. A. Haque, and O. A. Mohammed, "Power electronics revolutionized: a comprehensive analysis of emerging wide and ultrawide bandgap devices," *Micromachines*, vol. 14, no. 11, 2023, doi: 10.3390/mi14112045.

[12] A. Al-Safi, A. Al-Khayyat, A. M. Manati, and L. Alhafadhi, "Advances in FPGA based PWM generation for power electronics applications: literature review," in *11th Annual IEEE Information Technology, Electronics and Mobile Communication Conference, IEMCON 2020*, 2020, pp. 252–259, doi: 10.1109/IEMCON51383.2020.9284821.

[13] K. Manaswi, N. Jose, S. Bhaktha, B. Venkatesaperumal, and K. V. Gangadharan, "Implementation of PWM speed control for SRM drive using TMS320F28069 microcontroller," in *Proceedings of the 2023 1st International Conference on Cyber Physical Systems, Power Electronics and Electric Vehicles, ICPEEV 2023*, 2023, pp. 1–6, doi: 10.1109/ICPEEV58650.2023.10391895.

[14] T. Sithananthan, A. A. Bakar, B. Sannasy, W. M. Utomo, and Taufik, "Fast synchronization with enhanced switching control for grid-tied single-phase square wave inverter using FPGA," *International Journal of Power Electronics and Drive Systems*, vol. 15, no. 2, pp. 1105–1116, 2024, doi: 10.11591/ijpeds.v15.i2.pp1105-1116.

[15] P. Mishra, A. Banerjee, M. Ghosh, S. Gogoi, and P. K. Meher, "Implementation and validation of quadral-duty digital PWM to develop a cost-optimized ASIC for BLDC motor drive," *Control Engineering Practice*, vol. 109, no. September 2020, p. 104752, 2021, doi: 10.1016/j.conengprac.2021.104752.

[16] A. A. Bakar, W. M. Utomo, T. Taufik, and A. Ponniran, "Modeling of FPGA- and DSP-based pulse width modulation for multi-input interleaved DC/DC converter," *International Review of Electrical Engineering (I.R.E.E.)*, vol. 14, pp. 79–85, 2019.

[17] M. Lakka, E. Koutroulis, and A. Dollas, "Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 356–365, 2014, doi: 10.1109/TPEL.2013.2253216.
[18] R. Ramya, T. Pasupathi, and T. Shanthi, "Design and implementation of FPGA based real time multiple high frequency charger for electric vehicle charging system," *International Journal of Engineering Research & Technology (IJERT)*, vol. 12, no. 02, 2024.
[19] V. Sawant and P. Zambare, "DC fast charging stations for electric vehicles: a review," *Energy Conversion and Economics*, vol. 5, no. 1, pp. 54–71, 2024, doi: 10.1049/enc2.12111.
[20] A. Saday, İ. A. Ozkan, and I. Saritas, "FPGA-based battery management system for real-time monitoring and instantaneous SOC prediction," *International Journal of Applied Mathematics Electronics and Computers*, vol. 11, no. 1, pp. 55–61, 2023, doi: 10.18100/ijamec.1233451.
[21] G. Liu, L. Pan, and Q. Sun, "Design on one-cycle control VIENNA rectifier based on FPGA," in *IEEE 6th Information Technology and Mechatronics Engineering Conference,* 2022, vol. 6, pp. 1972–1975, doi: 10.1109/ITOEC53115.2022.9734333.
[22] A. A. Bakar, W. M. Utomo, S. A. Zulkifli, E. Sulaiman, M. Z. Ahmad, and M. Jenal, "DC-DC interleaved boost converter using FPGA," *CEAT 2013 - 2013 IEEE Conference on Clean Energy and Technology*, no. November, pp. 98–101, 2013, doi: 10.1109/CEAT.2013.6775607.
[23] Z. Dong and W. Li, "FPGA-based modular DC chopper model for real-time simulation & HIL tests," in *2023 IEEE 24th Workshop on Control and Modeling for Power Electronics, COMPEL 2023*, 2023, pp. 1–7, doi: 10.1109/COMPEL52896.2023.10221159.
[24] Z. Idris, M. K. Hamzah, A. Saparon, N.R.Hamzah, and N. Y. Dahlan, "FPGA design of single-phase matrix converter operating as cycloconverter," in *PEDS 2007*, 2007, pp. 301–307.
[25] A. A. Bakar, B. Sannasy, H. M. Poad, T. Sithananthan, W. M. Utomo, and N. F. D. Rosli, "Digitally fast synchronization of single-phase grid-tied inverter using FPGA," *International Journal of Power Electronics and Drive Systems*, vol. 15, no. 4, pp. 2452–2461, 2024, doi: 10.11591/ijpeds.v15.i4.pp2452-2461.
[26] L. Komsiyska *et al.*, "Critical review of intelligent battery systems: challenges, implementation, and potential for electric vehicles," *Energies*, vol. 14, no. 18, pp. 1–82, 2021, doi: 10.3390/en14185989.
[27] T. Pangaribowo, W. M. Utomo, A. A. Bakar, and D. S. Khaerudini, "Battery charging and discharging control of a hybrid energy system using microcontroller," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 17, no. 2, pp. 575–582, 2019, doi: 10.11591/ijeecs.v17.i2.pp575-582.
[28] N. Ghaeminezhad and M. Monfared, "Charging control strategies for lithium-ion battery packs: Review and recent developments," *IET Power Electronics*, vol. 15, no. 5, pp. 349–367, 2022, doi: 10.1049/pel2.12219.

BIOGRAPHIES OF AUTHORS

Afarulrazi Abu Bakar was born in Johor, Malaysia, in May 1980. He received his B.Eng. degree in electrical engineering from Universiti Teknologi Mara (UiTM), Malaysia, in 2004 and M.Eng. and Ph.D. degrees from Universiti Tun Hussein Onn Malaysia (UTHM) in 2019 and 2007, respectively. He has been working as a senior lecturer at the Department of Electrical Engineering, Faculty of Electrical and Electronic Engineering, UTHM, since 2007. His research interests include renewable energy, grid-connected systems, DC-DC converters, multiple-input converters, multiphase, resonant converters, and advanced controller design. He can be contacted at email: afarul@uthm.edu.my.

Suhaimi Saiman is a member of the IEEE. He received his B.Eng. degree in electrical and electronics engineering from University Leeds Metropolitan in 1997 and M.Eng. degree from Universiti Malaya (UTHM) in 2007, respectively. He has worked as a senior lecturer at the Department of Electrical Engineering, Faculty of Electrical and Electronic Engineering, UTHM, since 2008. His current research interests include battery charging, DC-DC converters, and inverters. He can be contacted at email: suhaimis@uthm.edu.my.

Tharnisha Sithananthan was born in Perak, Malaysia, in May 1997. She received her B.Eng. degree in electrical engineering from Universiti Tun Hussein Onn Malaysia (UTHM), Malaysia, in 2023. She has been pursuing an M.Eng. at UTHM since 2023. Her current research interests include power electronics and renewable energy. She can be contacted at email: tharnisha97@gmail.com.

Muhammad Nafis Ismail was born in Johor, Malaysia, in 1982. He received his B.Eng. Degree in electrical engineering from Universiti Teknologi Malaysia (UTM) in 2005. He worked as an Electrical Testing and Commissioning Engineer from 2005 to 2007. He has been appointed Vocational Training Officer at the Department of Electrical Engineering, Faculty of Electrical and Electronic Engineering, UTHM, since 2007. His areas of interest include renewable energy, electrical switchgear, and electrical power generation. He can be contacted at email: nafis@uthm.edu.my.

Saidina Hamzah Che Harun was born in Kuala Pilah, Negeri Sembilan, Malaysia, in September 1982. He received a degree in electrical engineering (power and high voltage) in 2005 from Universiti Teknologi Malaysia, Johor, Malaysia. Currently, he is the Managing Director of Magnitude Power Sdn Bhd. The company that conducts M&E business and HT Transformer service (up to 500 kV) is based in Kajang, Selangor. He also represents the Local Technical Advisor (TA) for transformer manufacturers such as Astor Transformer, Turkey, and Fortune Electric Transformer, Taiwan. He can be contacted at email: magnitudepower@gmail.com.