Design and experimental validation of a single phase grid tied inverter for residential low power applications

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Article Info	ABSTRACT
	This paper presents the design and control of a single phase grid tied inverter intended for low power applications in residential sector as part of smart grid environments or solar photovoltaic source integration. The total cost of the converters used in such applications involving low power rates, generally lower than 1 kW, cannot afford expensive components or complex techniques, so, the optimization of the power circuits as well as the simplification of the control algorithms are necessary to meet the specifications. In this purpose, this work presents the design steps of a single phase grid tied inverter including the structure choice, a synchronization algorithm based on the grid voltage zero crossing method, and the algorithm to control the injected power. Different experimental tests have been carried out and show the good performance of the converter which meets the requirements in terms of total harmonic distortion and efficiency. *This is an open access article under the [CC BY-SA](#) license.*

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1. INTRODUCTION

The growth of smart-grids and renewable energy sources where optimal electrical energy management strategies is a main objective, increase the demand on low power new generation converters and transform them to an indispensable devices as well as the appliances in households [1]. For example, solar photovoltaic sources have quickly found an important place in residential areas which allows households to produce a part or all of their consumption, and probably transforming them into suppliers of electrical energy. Injecting the surplus production into the electrical grid can only be done with grid tied inverters.

In order to make this new grid connected generation systems cost effective, regarding their low power range, the optimization of the power circuits as well as the simplification of the control algorithms are required. Moreover, the connectivity of such devices has no longer been only an option, but a main feature, so, the computational resource needs increase and therefore impose using more advanced control card or more than one. In this regard, whether in the context of smart grids [2]–[6] or the integration of photovoltaic energy [7]–[10], any connection to the grid with the aim of injecting electrical power into it, requires the use of a voltage or current grid tied inverter whose control should allow to control the active and reactive power flows and guarantee the injection of an energy with a good quality that complies with the standards in force, particularly, in terms of total harmonic distortion and electromagnetic compatibility [11]–[15], which relies on the design and the control quality of the inverter. Various control methods have been proposed to control the injected power of a grid tied inverter [16], [17], the specificity of controlling a grid tied inverter is that it requires a grid synchronization phase, in other words, the information about the frequency and the phase of the grid voltage are necessary to control the power flow, so, a so-called phase locked loop (PLL) is usually

used and allows to generate the good current references the inverters should impose [18], [19]. The PLL unit requires some mathematical transformations that can be heavy and significantly increases the computational resources needs. Moreover, the PLL algorithm is based on the grid voltage information, which imposes in addition the use of an extra fast response time voltage sensor, which considerably increases the converter cost because of the high price of such sensors. It should be noted that the voltage sensor price is not too significant compared to the total cost of high power rang devices, but in low power applications, according to commercial prices, the price of one voltage sensor with fast response time can be higher than the total price of all the switches the power circuit consists of, especially, when simple silicon-based transistors are used. Hence, the synchronization procedure will play an important role in reducing the overall price of the inverter if one can do without the voltage sensor and being back to the traditional method of voltage zero crossing using simply a low power transformer [20]. Today, this method can perform pretty well thanks to the good sampling time calculation provided by the recent microcontrollers, like the one used in this paper helping to reduce the needed computational resources and the overall cost of the device.

The work in [2] presents a very concrete application in the context of smart-grids, it presents a bidirectional DC/AC converter which makes it possible to recharge a battery outside peak hours and reuse this electricity within peak hours, the operation mode and the power amount are supposed to be imposed by the electricity supplier. In [21], the paper proposes a PLL-less vector control method for a single phase grid connected, however, it requires the use of a voltage sensor, the real-time tests were applied on a 220 V network for a power of 150 W. In fact, the required mathematical transformations are improved compared to methods with PLL but still remains significant.

This paper presents the structure and the control of a cost-effective grid tied inverter in order to control the power injected into the grid from a direct voltage source which is usually the output of a DC/DC converter in such applications Figure 1. The primary source can be a battery or any other renewable energy source. The reader will find in this paper the theoretical details of the control principle of a single phase grid tied voltage inverter allowing the control of the injected current, the good practices according to the experiments results, as well as the different steps of the real time implementation of the synchronization algorithm and the power control using a simple hysteresis closed loop current control. The assembly was tested with a 110 V/50 Hz electrical network and the experiment results clearly show the effectiveness of the control strategy that allows to inject a current with a good quality that meets properly the standards requirements.

The first section presents the implemented control principle and discusses the choice of the power structure. The second section presents the grid synchronization algorithm and discusses its advantages. The third section presents the current closed loop control making it possible to control the power flow as well as the comparison of several configurations to be able to select the best one. The last part, presents the power and control circuits in accordance with the theoretical study, then, in order to demonstrate the validity and the effectiveness of the adopted configuration, experimental results are presented and demonstrate a total harmonic distortion (THD) of 1.6% and an efficiency of 97%. At the end, the reader will find a conclusion focusing on the strong points and the points to improve.
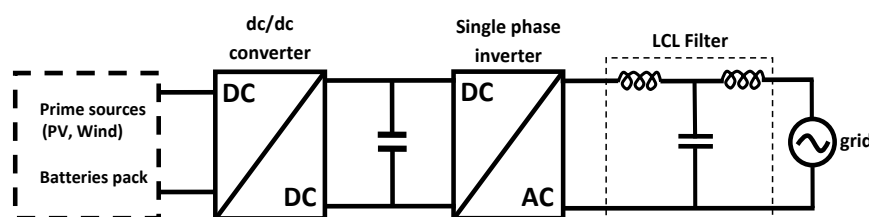

Figure 1. Grid connected converter

2. METHOD
2.1. Single phase inverter

The classic single phase inverter consists of two arms with tow reversible current switches each. There are other more sophisticated circuits referred as multilevel inverters [22], where each arm consists of more than two switches and provides more output voltage levels which improves the waveform of the output current knowing that it should generally be as close as possible to a sinusoidal waveform. In this paper, we are interested in the classic single phase inverter, where the output voltage can only be bipolar or unipolar according to the command type. Each switch is made up of one transistor and one anti-parallel diode. Figure 2 presents the circuit of such converter. Only a coil is used as a filter to simplify the operation reasoning.
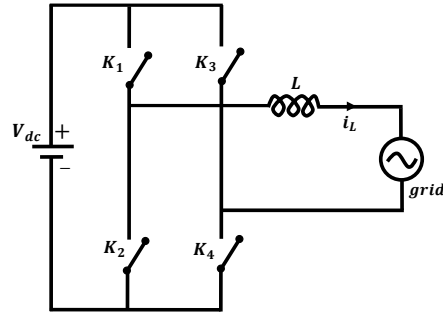
Figure 2. Power circuit of a grid tied inverter

2.1.1. Control principle

In bipolar control, at any moment two transistors or two diodes conduct. During the positive alternation T1 and T4 (respectively T2 and T3 during the negative alternating) are turned ON to force the current to increase, D2 and D3 (respectively D2 and D3 during the negative alternating) ensure the freewheeling and cause the current to decrease. So, we can control the current and force it to follow the desired reference, which is generally, a sinusoidal current with the same frequency and phase as the grid voltage.

In high switching frequencies and low power applications, the switching losses are predominant, so, the efficiency of such devices depends mainly on them. Let's assume F to be the average of the switching frequency in steady state operation, (1) gives the switching losses.

$$P_{com} = 2.P_{sw\_T} + 2.P_{rr\_D} = 2.W_{com}.F + 2.V\,Q_{rr}.F \tag{1}$$

Where P_{sw_T}: transistor switching power losses; P_{rr_D}: power losses due to the diodes reverse recovery current; W_{com}: switching energy loss of a transistor, equal to: $0.5.V_{DS}.I_D.(t_{ON} + t_{OFF} + t_{rr})$; and Q_{rr}: the diode reverse recovery charge.

Using metal-oxide-semiconductor field-effect transistor (MOSFET) as switches, which are the most used recently in low and medium power ranges, especially, with the growth of wide bandgap MOSFETs [23], we can get rid of the anti-parallel diodes and make do with the MOSFET's body diodes. Given that these ones are slow diodes, we can adopt a complimentary command of each arm transistors. The complimentary command makes it possible to simplify the driver's circuits by using bootstraps to drive the high side transistors, however, it requires the use of a dead time to avoid short-circuiting the input voltage source, which is difficult to implement when digital outputs are used instead of pulse width modulation (PWM) blocs as in our case.

In this paper, the unipolar command is adopted thanks to its superiority over the bipolar one in terms of power losses and ripple amplitude. It should be noted that the reasoning here is done in an algebraic sense and we recall that the goal is to force the current to follow a sinusoidal reference provided by the synchronization algorithm presented. The transistors switching's depend on the current half wave.

In the first half-wave ($V_G > 0$): T4 remains ON, and the switching of T1 is used to control the current, so we have two cases:
a. T1 is ON: T1 and T4 conduct, the equivalent circuit is given by Figure 3 and this configuration is used to increase the current when $i_L < i_{ref}$, (2).

$$L.\frac{di_L}{dt} = V_L = V_{dc} - V_G > 0 \tag{2}$$

b. If i_L exceeds i_{ref}, T1 is turned OFF to decrease the current according to (3), so, the current continuity is ensured by T4 turned ON throughout the first half-wave and the anti-parallel diode of K2. The equivalent circuit is given by Figure 4.

$$L.\frac{di_L}{dt} = V_L = -V_G < 0 \tag{3}$$

In the second half-wave ($V_G < 0$): T3 remains ON and T2 is switched to control the current, so, we end up with two cases:
a. T2 is ON: T2 and T3 conduct, the equivalent circuit is given by Figure 5 and allows to increase the current according to (4) when $|i_L| < |i_{ref}|$.

$$L.\frac{di_L}{dt} = V_L = -V_{dc} - V_G < 0 \tag{4}$$

b. If $|i_L|$ gets over $|i_{ref}|$, T2 is turned OFF to decrease it, and the current continuity is provided by T3 all time ON during the second half-wave and the anti-parallel diode D1, as shown in Figure 6 and (5).
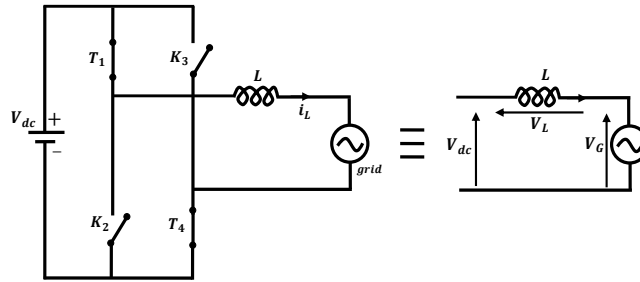
$$L.\frac{di_L}{dt} = V_L = -V_G > 0 \tag{5}$$

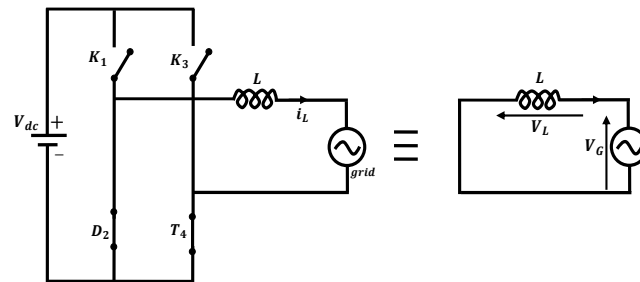Figure 3. Equivalent circuit to increase the current in the positive alternation

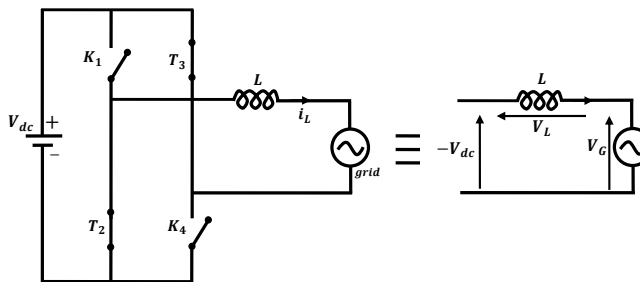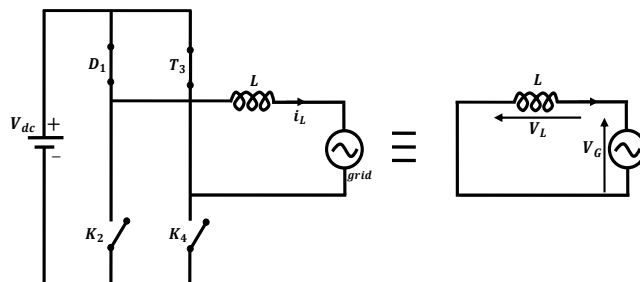Figure 4. Equivalent circuit to decrease the current in the positive alternation

Figure 5. Equivalent circuit to increase the current in the negative alternation

Figure 6. Equivalent circuit to decrease the current in the negative alternation

This control method reduces significantly the switching losses since only one transistor switches at a time (T1 during the first half-wave and T2 during the second one). Generally, the losses are half those of the bipolar control. If no Schottky diodes are used, a complimentary command of each arm should be used to avoid the problems related to the slow body diodes. Besides, it should be noted that the two transistors used each alternation can change role, so, different combinations will be tested to determine the best configuration.

Figure 7 presents one of the configurations of the carried out power circuits. It consists of four silicon based MOSFETs and two Schottky diodes added in anti-parallel to T1 and T2. As explained above, the current is regulated by T1 in the first half-wave (T2 in the second half-wave) knowing that T4 remains ON during this half-wave (T3 during the second half-wave) and the freewheeling is provided by T4 and D2 (T3 and D4 in the second half-wave). The main benefit of this configuration is to prevent the body diodes from conducting, and consequently, to minimize the diodes reverse recovery current that degrades the efficiency and accentuates the electromagnetic interference (EMI) issues. Figure 8 shows the driver circuit carried out to drive each of the four MOSFETs, it consists of a commercial transistor gate driver and a galvanic isolated DC/DC converter to supply properly the gate driver.
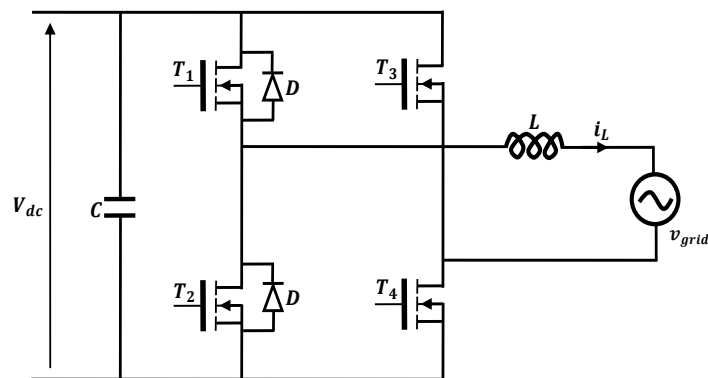

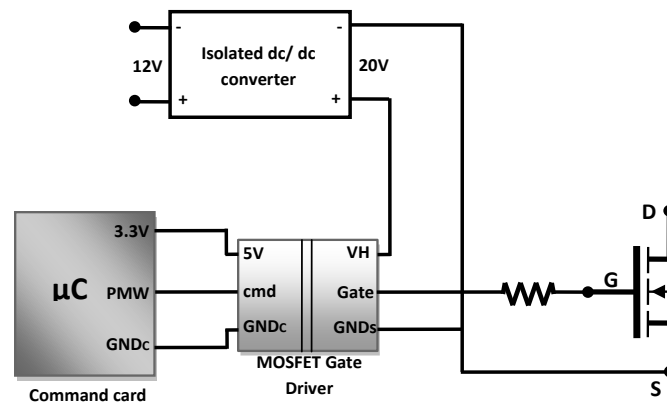Figure 7. Adopted configuration for the power circuit

Figure 8. MOSFET's driver circuit

2.1.2. Closed loop control

Figure 9 presents the control diagram practically used in this work to implement the control strategy detailed. In fact, as two transistors switch at high frequency and the others at 50 Hz, there are three ways to implement our approach; actually, as high frequency transistors, (T1 and T2) or (T1 and T3) or (T2 and T4) can be used. In simulation, the three configurations give the same performance, but practically, the first one shown in Figure 7 provides more performance over the two others that are less efficient because of the high current ripple in one of the two alternations. As will be shown in section 3, the current ripple is higher during the second half-wave in the second configuration and during the first half-wave in the third configuration.

The injected power is assumed to be purely active in this work and is referred as P_{ref}, so, the reference current amplitude is calculated using (6).

$$I_{ref} = \frac{P_{ref}}{\sqrt{2}.V_{grid}} \tag{6}$$

Once the synchronization is achieved, the control algorithm should force the current toward the grid to follow as close as possible the current reference. In this regard, a simple hysteresis controller is used to control the high frequency switching transistors as shown in Figure 9, which results in the MOSFETs switching given in Figure 10. It should be noted that a dead time is added at the zero-crossing moment to move on from one half wave to the other smoothly. In fact, around the point zero of the grid voltage all the transistors are turned off. Several dead time values are tested in section 3.
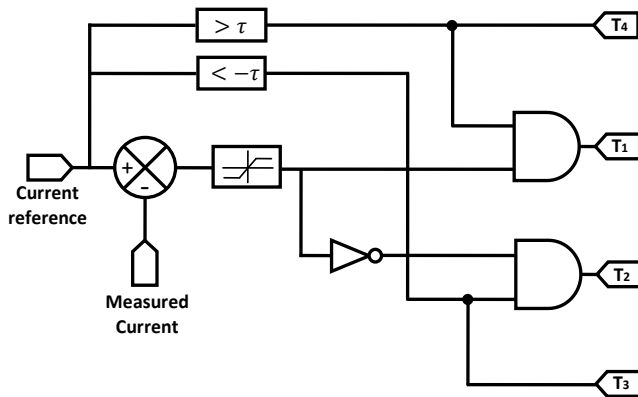
Figure 9. Control bloc diagram of the single phase grid tied inverter
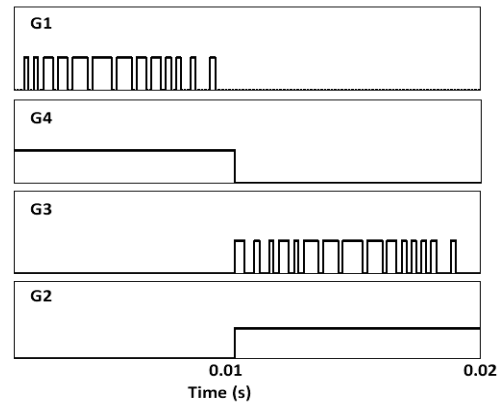
Figure 10. MOSFET's gates signals

2.1.3. Synchronization procedure and current reference calculation

PLL is a fundamental component of grid tied inverters, it plays a significant role in controlling the grid current and should be as much as possible accurate in phase detection, so that, the inverter can inject the right amount of power into the grid regardless the grid voltage changes in terms of frequency, phase or amplitude. Some methods are designed without modifying the control structure, they are easy to implement but they are limited by the stability concerns [24]. Others involve modifying the control structure and even require the prior knowledge of the grid impedance [25]. It should be noted that most inverter controllers are grid-following and designed basing on the fact that the system voltage and frequency are regulated by other inertial sources. Recently, with the growth of non-traditional sources such as renewable energy sources and energy storage devices used in particular in weak grid or low inertia power systems, a new generation known as grid forming controllers has been developed. To synchronize these latter, a modified droop-control of the active power error is used instead of the PLL [26], [27].

In this work, a grid following method to synchronize the inverter is used. The method is carried out taking into consideration the simplicity and the total cost in order to match the requirements in the case of low power inverters, used in particular in smart grid environment and solar tied converters. The algorithm uses a low power printed circuit board (PCB) transformer instead of a voltage sensor, which allows considerable savings in terms of cost. Figure 11 shows the electrical circuit practically implemented for the synchronization and Figure 12 illustrates the corresponding signals, knowing that the comparator is a built-in component of the microcontroller.
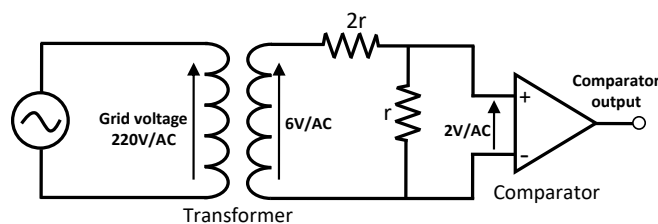

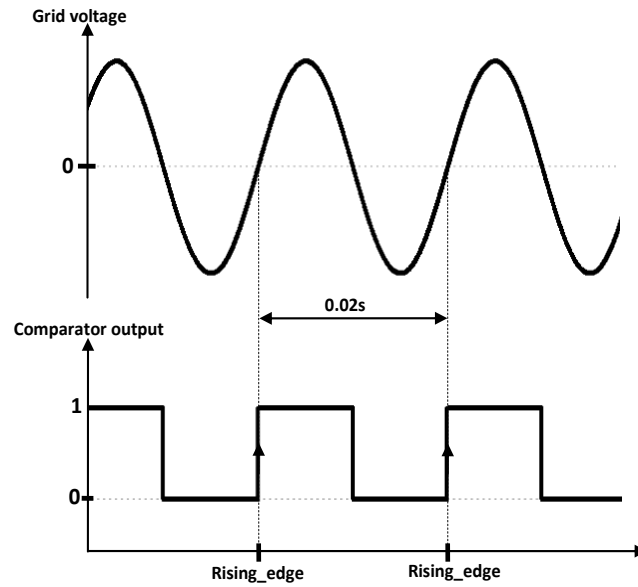Figure 11. Voltage zero crossing circuit

Figure 12. Signals of the zero-crossing circuit

The grid synchronization algorithm is only based on the grid voltage zero crossing times to calculate the frequency and the phase of the grid voltage. All is expressed as a function of the microcontroller sampling time. Hence, each rising edge of the comparator bloc output means the beginning of the first half-wave of the grid voltage. It should be noted that this allows the frequency to be tuned every period and adjusts with the frequency variation of the grid, moreover, it is not sensitive to the grid type (50 or 60 Hz). Figure 13 shows the implemented algorithm diagram.
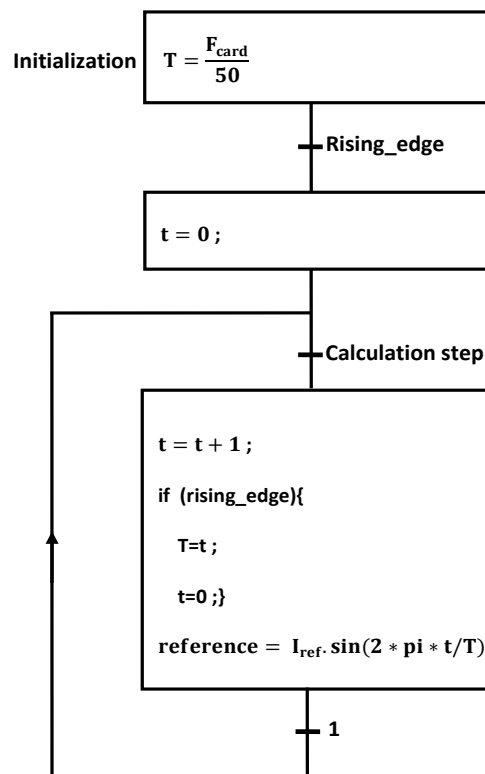
Figure 13. Diagram of the proposed synchronization algorithm

3.   EXPERIMENT RESULTS

Figure 14 shows the experimental test bench, which consists of a single phase inverter based on silicon discrete transistors locally carried out, and a microcontroller TMSF28335 DSP that hosts the control and synchronization algorithms implemented using code composer studio (CCS) software. Parameters of the components forming the control and power circuits are listed in Table 1. The inverter input is powered by a DC power source with a voltage fixed at 180 V, the inverter output is connected to the grid through a transformer. An LC filter is used to connect to the grid.
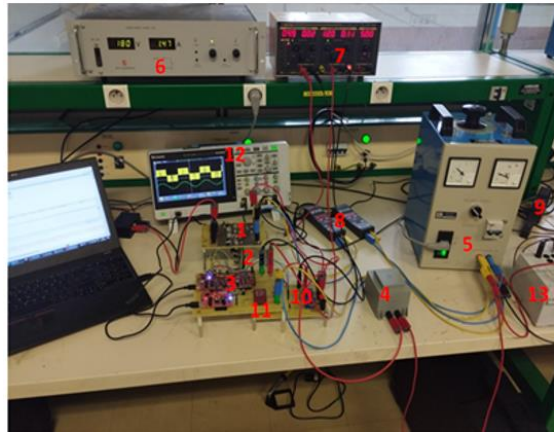
1 Inverter
2 Driver card
3 Command card
4 Coil
5 Capacitor
6 DC source
7 Drivers
8 Voltage probes
9 Current probe
10 Current sensor
11 Oscilloscope
12 Grid
13 Drivers power supply

Figure 14. Experimental setup

Table 1. Hardware parameters

MOSFET	Diode	Microcontroller	Gate driver	V_{dc}, V_{grid}	LC filter
Silicon	Schottky	EzDSP F28379D	STgap SCMTR	180 V, 110 V/50 Hz	5 mH, 5 mF

3.1. Test 1: selection of the best configuration

Figures 15 to 17 give the currents injected into the grid according to the transistors used as high frequency switching transistors. Figure 15 corresponds to the first configuration where T1 and T3 are used, Figure 16 corresponds to the second configuration using T2 and T4, and Figure 17 corresponds to the third one in which T1 and T2 are used. The experiment results show clearly the superiority of the third configuration that allows injecting a current with a THD around 1.6% instead of 5.5% given by the other two structures.
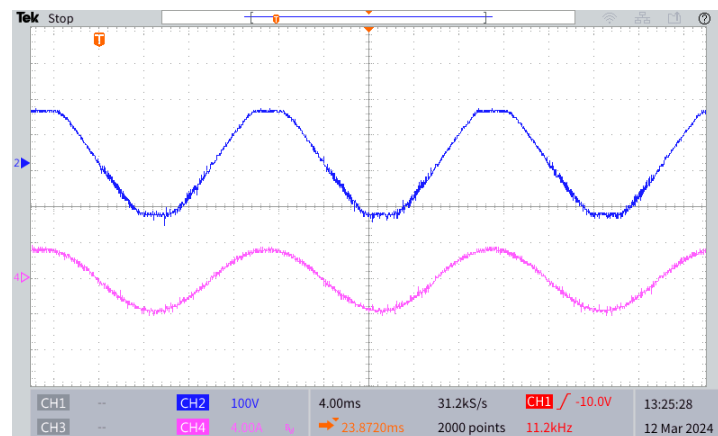

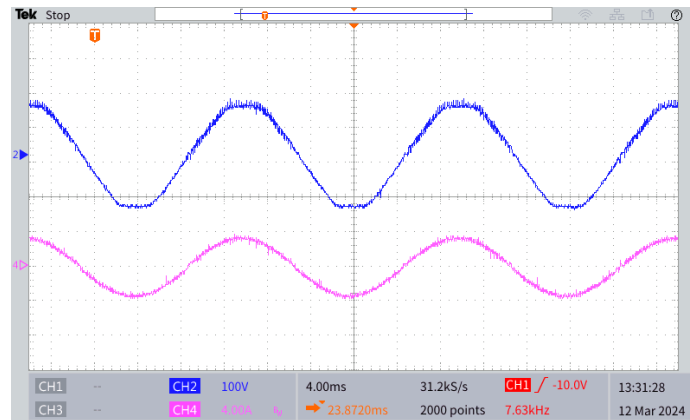Figure 15. Configuration 1 (blue: grid voltage, pink: grid current)

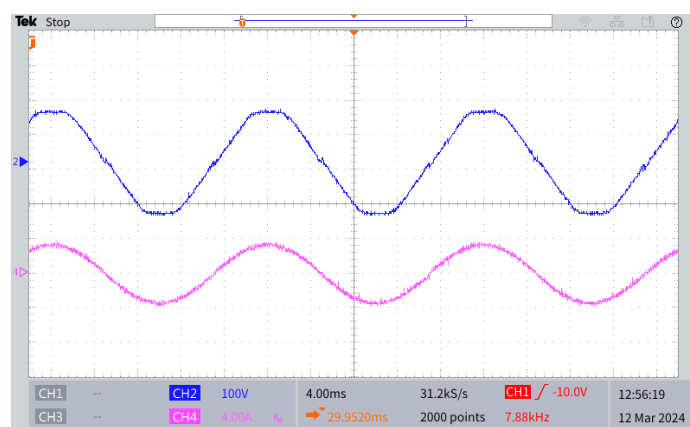Figure 16. Configuration 2 (blue: grid voltage, pink: grid current)

Figure 17. Configuration 3 (blue: grid voltage, pink: grid current)

3.2. Test 2: highlight of different quantities of the best configuration

Figure 18 shows the gate voltage of T1 (yellow) and T4 (red), Figure 19 shows the drain-source voltages of T1 (yellow) and T4 (red), obviously there is no risk of overvoltage. Figure 20 shows the grid side quantities, namely, the grid current (pink), the grid voltage (blue) and the inverter output voltage (red). Figure 21 shows a zoom of Figure 20 in order to highlight the grid current and the inverter voltage output behaviors in a switching period. The figures make sure that the expected operation according to the theoretical reasoning is achieved.
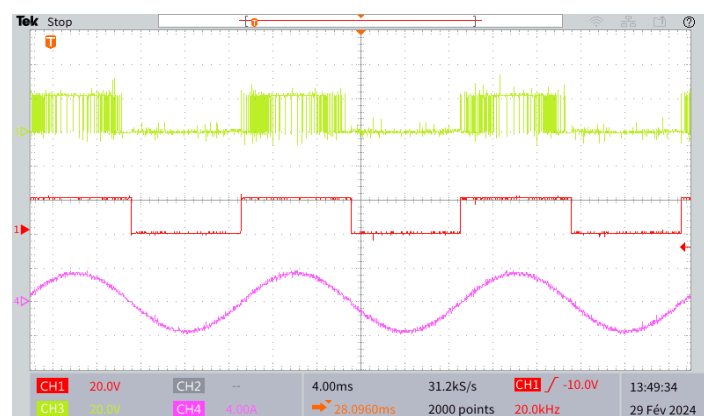

Figure 18. MOSFETS's gates voltages (T1 yellow) (T4 red), and grid current (pink)
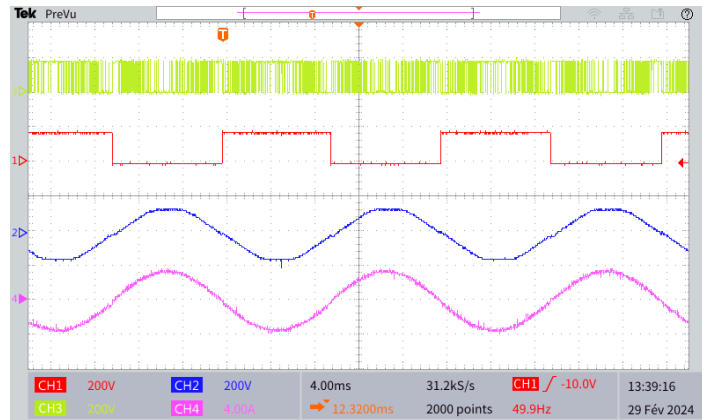
Figure 19. MOSFETS's drain-source voltages (T1 yellow) (T4 red), grid voltage (blue), and grid current (pink)
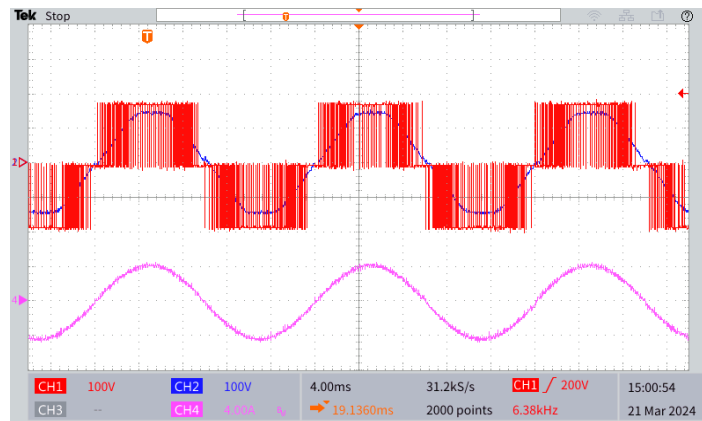

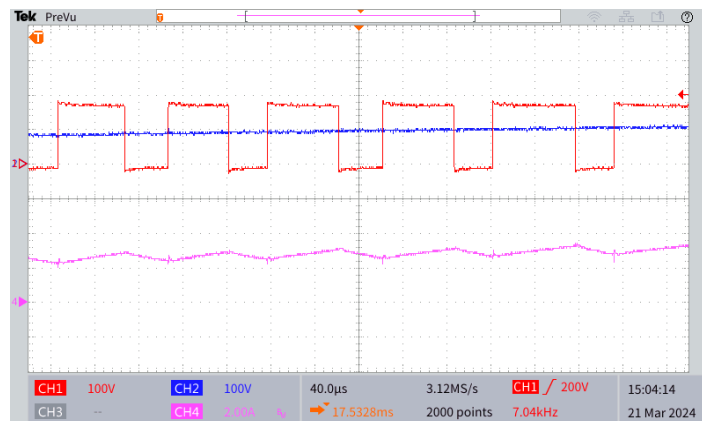Figure 20. Inverter output voltage (red), grid voltage (blue), and grid current (pink)

Figure 21. Inverter output voltage (red), grid voltage (blue), and grid current (pink)

3.3. Test 3: zero crossing moment

The adopted control approach needs to add a dead time at the zero-crossing moment to prevent T1 and T2 to conduct together and causes the DC-bus to be short-circuited. Knowing that only digital outputs of the card are used, which means that the orders are updated together only after a sampling time (equal to 10 µs in our case), there is no possibility to add a dead time to avoid short-circuiting the DC-bus at zero crossing. To address this issue, we have chosen to disconnect the input around the zero crossing moments and let the

current drops to zero in freewheeling way knowing that the grid voltage is around zero this time. The response time of the transistors is around 100 ns, so one sampling time is enough to address this problem, however, several intervals has been tested as shown in Figures 22 and 23. As a result, one sampling time gives the best performance.
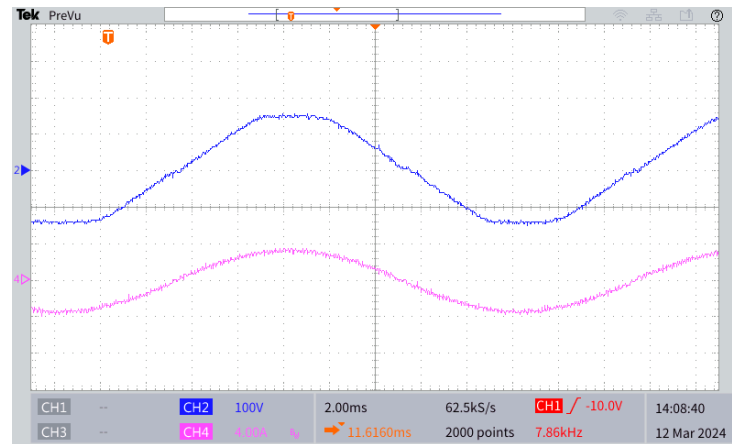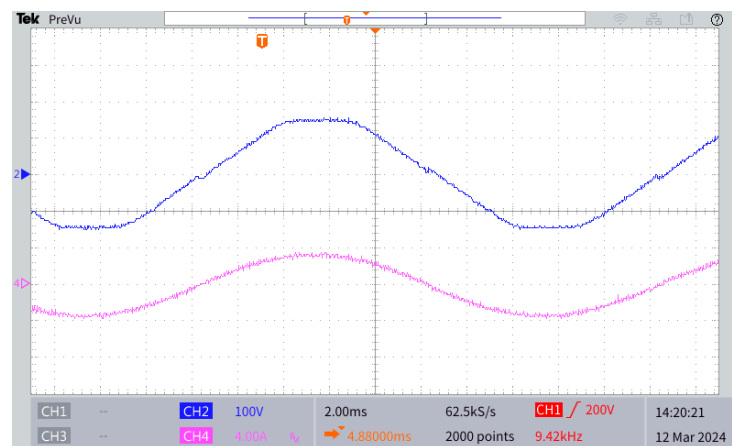

Figure 22. Dead time equal to one sampling time (10 μs)

Figure 23. no dead time

4. CONCLUSION

In this paper the design and the control algorithms of a grid tied inverter intended for low power applications have been presented. The cost is the main criterion taken into account in the design given that the new electrical distribution systems, especially in residential sectors, involve using such low power converters that were long time limited to industrial areas. However, the converter should meet the requirements imposed by the standards in terms of the total harmonic distortion and electromagnetic interferences. The experiment results show a very good performances in terms of THD which is kept around 1.6% and an efficiency of 97%. The presented experiment results were taken injecting a power amount of around 400 W into the grid. In fact, tests have been extended to a power level up to around 800 W, yet, there is no need for heat sinks. In terms of EMI standards, even if they have not been presented, the results show that there is a need to use an EMI filter to make the converter meet the standards for frequencies between 150 KHz and 5 MHz. Generally, the converter is part of an overall system that includes basically at least a DC/DC stage and a power factor correction (PFC) in addition to the inverter in bidirectional applications, so designing the EMI filter should be carried out for the complete system.

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