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Design of low power complementary metal-oxide semiconductor static random-access memory cell for embedded memories at three different technology nodes

Seerapu Venkatesh[1,2], Krishna Veni Sahukara[2]
[1]Andhra University Trans-Disciplinary Research HUB, Department of Electronics and Communication Engineering, Andhra University College of Engineering, Visakhapatnam, India
[2]Department of Electronics and Communication Engineering, Gayatri Vidya Parishad College for Degree and PG Courses (A), Visakhapatnam, India

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ABSTRACT

In this work, the complementary metal-oxide semiconductor (CMOS) static random-access memory (SRAM) cell is proposed using a hybrid model. It is designed by combining two different methods and simulated at different technologies which are 180, 90, and 45 nm. The proposed hybrid model SRAM cell has less power consumption. The power consumption results of the hybrid model SRAM cell are contrasted with the 6T CMOS SRAM, Stacked SRAM cell, and 8T SRAM cell at 180, 90, and 45 nm. Tanner tool was used for designing and simulating these different SRAM cell topologies at 180, 90, and 45 nm technology nodes. S-edit is used for designing circuit diagrams, T-edit is used for simulating spice net lists and W-edit is used for observing waveforms in Tanner tool. The hybrid SRAM cell at 45 nm got better power consumption results than other SRAM cell topologies at different technology nodes.

Corresponding Author:

Seerapu Venkatesh
Andhra University Trans-Disciplinary Research HUB, Department of Electronics and Communication Engineering, Andhra University College of Engineering
Visakhapatnam, Andhra Pradesh, India
Email: venkateshseerapu2019@gmail.com

1. INTRODUCTION

Volatile and non-volatile memories are the two types of electronic memories. Volatile memory is random access memory (RAM) and non-volatile memory is read only memory (ROM). RAM is a main memory. The instructions from secondary memory are transferred to central processing unit (CPU) through main memory so the speed of the main memory should be high to work faster. The main memory RAM can be static structure or dynamic structure. Static memories have feedback to hold their state where as dynamic memories use capacitor to hold the state. The problem with the dynamic memory is that the capacitor may leak the charge so here there is a need of refresh operation. So, it is considered as dynamic because it dynamically refreshes all the time. In static memory, the cell does not required refreshment so it is faster than the dynamic memory cell. In cache memories where the high speed is required static RAM cells are used. Static random-access memory (SRAM), or static random-access memory, is now a requirement for every system-on-a-chip (SoC) design. SRAM is frequently used in modern high-performance systems due to its exceptional flexibility with logical circuit designs [1], [2] because battery-powered devices have limited energy, there has been a great deal of attention paid to the study of low-power memory circuits in the modern era [1]. Numerous advantages of devices, including enhanced performance, lower power consumption, and

smaller device dimensions, are made possible via technology scaling. Nevertheless, circuits grow increasingly prone to noise and inconsistency as technology nodes drop [3], [4]. The factors of static, dynamic, average, and peak power all contribute to the explanation of the SRAM cell's overall power dissipation. Static power has received the most attention thus far [5]. The power dissipation in the bit and data lines of SRAM increases in tandem with its bit width. Power dissipation is therefore a crucial factor to consider in designs. High-performance and low-power design has received a lot of demand with the addition of faster models and an increase in battery-operated devices [6]. Furthermore, it is critical to differentiate between the different power consumption components and decrease some without raising others [7]. For many years, the dynamic power, which accounts for between 70 and 90 percent of the overall circuit consumption in digital complementary metal-oxide semiconductor (CMOS) circuits till 100 nm, dominated the power dissipation equation in these circuits when compared to other factors. V_{DD} reduction is a useful technique to lower both the dynamic and total power dissipation because, the $P_{Dynamic}$ is proportional to the square of the supply voltage [8], [9]. Traditional SRAM cell design is challenged by aggressive size reductions brought forth by technology scaling, which affect cell stability and memory leakage [10], [11]. Only super computers had access to this processing power before, but in inexpensive cell phones now we can have that feature [12]. The low power implementation of SRAM, one of the fundamental memory components in computer processors and controllers, as well as mobile apps, presents a challenge for longer battery life [13]. V_{DD} scaling has newly stretched to subthreshold circuit actions to extremely decrease the total power consumption [14], [15]. As an effect, a heavy amount of power consumption has been saved which may affect speed performance. Low power SRAM cell is crucial part of modern electronic gadgets because of increased life of the battery, leads lower dissipation of heat which can reduce the cost and size of the cooling system, and boost the performance by reducing the power related problems like timing variations and noise.

6T CMOS SRAM cell is the standard CMOS SRAM cell. In the 8T CMOS SRAM cell the transistor T7 gate terminal is connected to the node Q and the transistor T8 gate terminal is connected to the node Q_B due these connections the logic will be pulled either high or low strongly in the memory. The discharge rate at the nodes Q and Q_B decreases which saves the power consumption.

Shorter interconnects between layers or components are made possible with the stacking technique. In stacked integrated circuits (ICs) due to with shorter interconnects and optimized design circuits can operate at lower voltages. Dynamic power consumption is proportional to the square of the supply voltage. So, stacked designs also decreases power consumption due to less supply voltage requirements. Proposed hybrid model SRAM cell is obtained by combining both 8T CMOS SRAM cell and stacked CMOS SRAM cell. So, in this we got advantages of both 8T CMOS SRAM cell and stacked CMOS SRAM cell without compromising in performance.

2. CMOS 6T SRAM CELL

In the below circuit T1 and T3 forms one inverter and T2 and T4 forms another inverter output of T1T3 inverter is connected as input for inverter T2T4 and output of T2T4 inverter connected as input for the T1T3 inverter as shown in Figure 1. T1 and T2 are called as driver transistors, T3 and T4 are termed as load transistors and T5 and T6 are the access transistors. Through T5 and T6 can access data from the SRAM cell so those are called access transistors. This SRAM circuit is designed with two P-Channel MOS (PMOS) and four N-Channel MOS (NMOS) so this is called as 6T SRAM cell. The operation of 6T SRAM cell is explained in three different modes those are Hold mode, Read mode, and Write mode [10]. For maintaining more stable operation current flowing through T3 and T4 greater than the current flowing through T5 and T6 [16]. The 6T SRAM cell is high sensitivity to power, voltage and temperature fluctuations as an effect of the exponential relationship between drain current and V_{GS} in added to V_t in subthreshold situations [17], [18].

In Hold mode the SRAM cell holds the previous data, further in this mode Read and Write operations cannot be performed. In Hold mode the word line (WL) should be low. In Read operation word line should be equal to logic-1 so the transistors T5 and T6 transistors are in ON condition BL and BL_B are connected to SRAM cell and read the data from SRAM [19]. In Read-0 operation transistor T2 is in ON condition and T4 is in OFF condition so the output of the inverter T2T4 is connected to the V_{DD} which is appeared at output line BL_B so the output at BL_B is equal to logic-1 output of the inverter T2T4 connected as input for the inverter T1T3 so the transistor T3 is in ON condition and T1 is in OFF condition so the output of the inverter T1T3 is connected to the ground which is appeared at output line BL so the output at BL is equal to logic-0 [3], [20] as shown in Figure 2.

In Read-1 operation transistor T2 is in OFF condition and T4 is in ON condition. The output of the inverter T2T4 is connected to the ground which is appeared at output line BL_B so the output at BL_B is equal to logic-0. Output of the inverter T2T4 connected as input for the inverter T1T3 so the transistor T3 is in OFF condition and T1 is in ON condition. The output of the T1T3 inverter is connected to the V_{DD} which is appeared at output line BL so the output at BL is equal to logic-1 as shown in Figure 3.

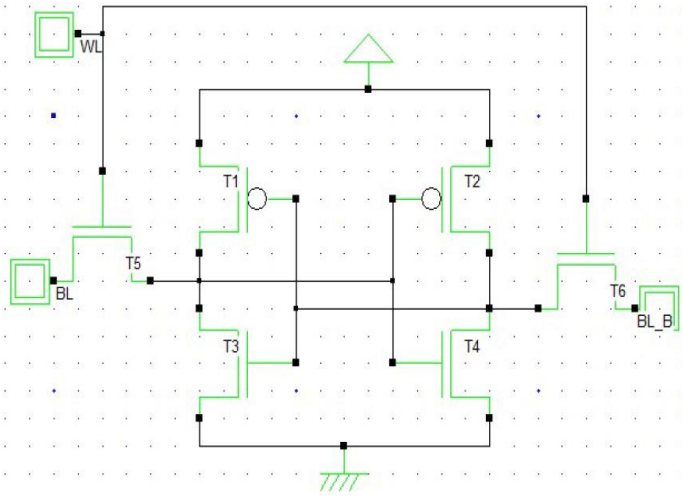

Figure 1. Schematic diagram of 6T SRAM cell

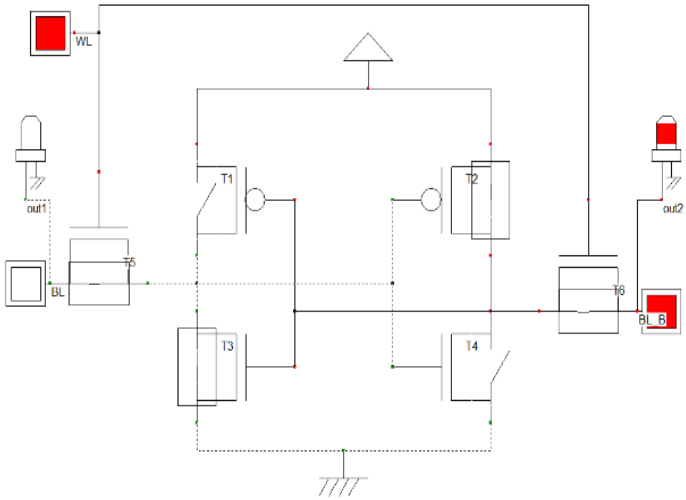

Figure 2. Read-0 operation of 6T SRAM cell

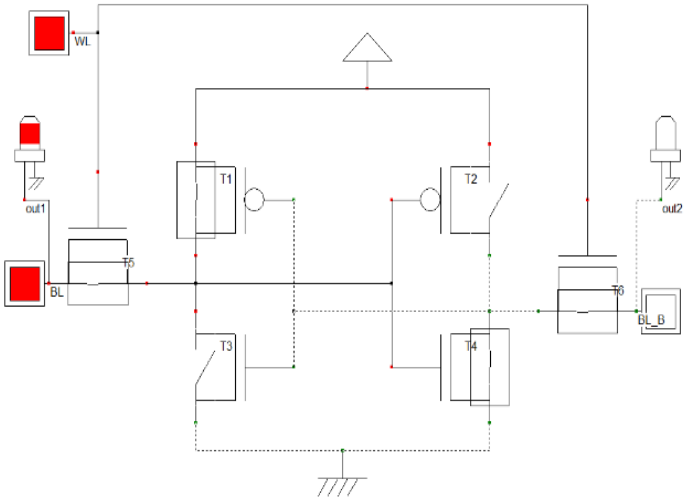

Figure 3. Read-1 operation of 6T SRAM cell

In Write operation word line should be equal to logic-1 so the transistors T5 and T6 transistors are in ON condition BL and BL_B are connected to SRAM cell and write data into the SRAM. In Write-1 operation, let us consider output of the T1T3 inverter is logic-0 and output of the T2T4 inverter is logic-1. Now consider writing data logic-1 into BL and logic-0 into BL_B. WL is logic-1 so the transistors T5 and T6 are in ON condition. Since BL is equal to logic-1 transistor T5 want to make output of T1T3 inverter to logic-1 but T3 want to keep output of the inverter T1T3 to logic-0 so to win T5 over T3 the width of the transistor T3 should be greater than the T5 [21], [22], [23]. Similarly, BL_B is equal to logic-0 transistor T6 want to make output of T2T4 inverter to logic-0 but T2 want to keep output of the inverter T2T4 to logic-1 so to win T6 over T2 the width of the transistor T2 should be greater than the T6 [12].

In Write-0 operation, let us consider output of the T1T3 inverter is logic-1 and output of the T2T4 inverter is logic-0. Now consider writing data logic-0 into BL and logic-1 into BL_B. WL is logic-1 so the transistors T5 and T6 are in ON condition. Since BL is equal to logic-0 transistor T5 want to make output of T1T3 inverter to logic-0 but T1 want to keep output of the inverter T1T3 to logic-1 so in order to win T5 over T1 the width of the transistor T1 should be greater than the T5. Similarly, BL_B is equal to logic-1 transistor T6 want to make output of T2T4 inverter to logic-1 but T4 want to keep output of the inverter T2T4 to logic-0 so in order to win T6 over T4 the width of the transistor T4 should be greater than the T6. The SRAM pull-up ratio (PR) is the ratio of the width of the driver transistor (T1 or T3) to the access transistor (T5 or T6) [24]. The SRAM cell ratio (CR) is the ratio of the width of the load transistor (T2 or T4) to the access transistor (T5 or T6).

3. 8T CMOS SRAM CELL

Figure 4 shows the schematic diagram of 8T CMOS SRAM cell in which two extra transistors T7 and T8 are added to 6T CMOS SRAM cell. Transistor T7 is added in series with the transistors T1 and T3 and its gate terminal is connected to BL. Transistor T8 is added in series with the transistors T2 and T4 and its gate terminal is connected to BL_B. Due to these added transistors the logic either low or high pulled strongly at the output of SRAM cell enlightening the cells capacity to Write mode operation [1]. These transistors also reduce rate of discharge ON the output in the Write mode sensitively opposing dynamic power. Short circuit power consumption occurs when input signal transition occurs from logic-0 to logic-1 and logic-1 to logic-0 [25], since in that condition only both PMOS and NMOS transistor are in ON condition which causes direct path from supply voltage to ground [8]. In this 8T SRAM cell topology short circuit power consumption also decreased since extra transistor is added which cause increases resistance between supply and ground, so the short circuit current will decrease and short circuit power consumption also decreases [13].

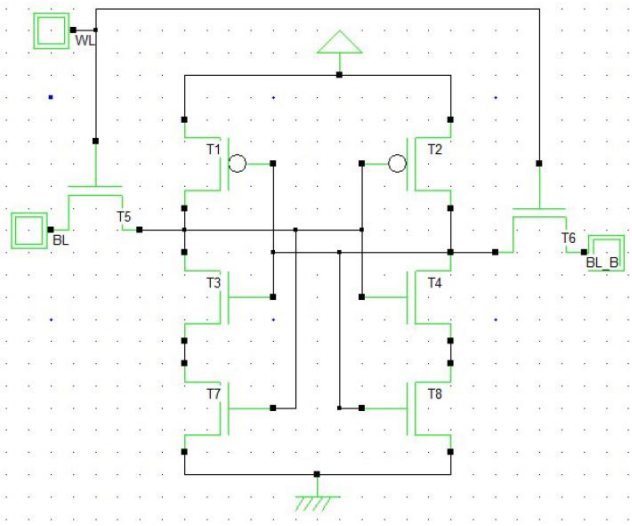

Figure 4. Schematic diagram of 8T CMOS SRAM cell

4. STACKED CMOS SRAM CELL

Stacking means connecting two are more transistors in series. The leakage power present in two series transistors is less compared to single transistor since two are OFF at the same time [26]. Figure 5 represents the schematic diagram of Stacked CMOS SRAM cell in which each transistor in both the inverters

are replaced with two transistors with half of the width. The sleep transistors T1 and T3 which are connected to supply voltage are called as header switches. The header switches turn OFF the supply voltage and keeps the ground [6]. The sleep transistors T6 and T8 which are connected to supply voltage are called as footer switches. The footer switches control the ground. Current flowing through the single NMOS transistor as depicted in Figure 6.

$$I = I_0 \frac{W}{L} e^{(-\frac{V_t}{\emptyset_t})}$$

Current flowing through the two NMOS stacked transistors as depicted in Figure 7.

$$I_2 = I_0 \frac{W}{L} e^{(-\frac{V_t}{\emptyset_t})}(1\text{-}e^{(-\frac{V_x}{\emptyset_t})})$$

$$I_1 = I_0 \frac{W}{L} e^{(\frac{-V_x - V_t}{\emptyset_t})}(1\text{-}e^{(-\frac{V_{DD}}{\emptyset_t})})$$

$$V_{DD} >> \varnothing_t$$

$$I_1 = I_0 \frac{W}{L} e^{(\frac{-V_x - V_t}{\emptyset_t})}$$

$$I_1 = I_2$$

$$I_0 \frac{W}{L} e^{(\frac{-Vx - Vt}{\emptyset t})} = I_0 \frac{W}{L} e^{(-\frac{V_t}{\emptyset_t})}(1\text{-}e^{(-\frac{V_x}{\emptyset_t})})$$

$$V_x = \varnothing_t \ln 2$$

$$I_1 = I_2 = I_{stacked} = \frac{1}{2} I_0 \frac{W}{L} e^{(-\frac{V_t}{\emptyset_t})}$$

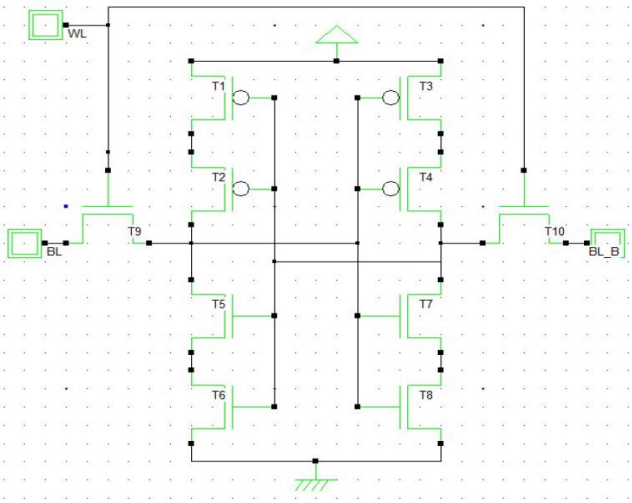

Figure 5. Schematic diagram of stacked CMOS SRAM cell

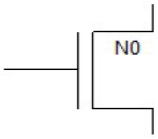

Figure 6. Single NMOS transistor

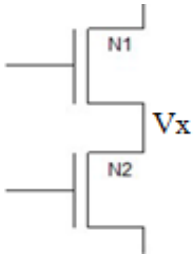

Figure 7. NMOS transistors connected in stacking

5. HYBRID MODEL SRAM CELL

Figure 8 shows schematic diagram of hybrid model SRAM cell which is a combination of both 8T CMOS SRAM cell and stacked CMOS SRAM cell. This SRAM topology has advantages of both 8T CMOS SRAM cell and stacked CMOS SRAM cell. Like 8T CMOS SRAM cell it gives strong logic signals at the output so in Write mode operation it increases the cell capacity and reduces the short circuit power consumption since the resistance between supply and ground increases. The hybrid model SRAM cell also uses stacking of transistors, so due to stacking effect leakage current is reduced which decreases the leakage power consumption.

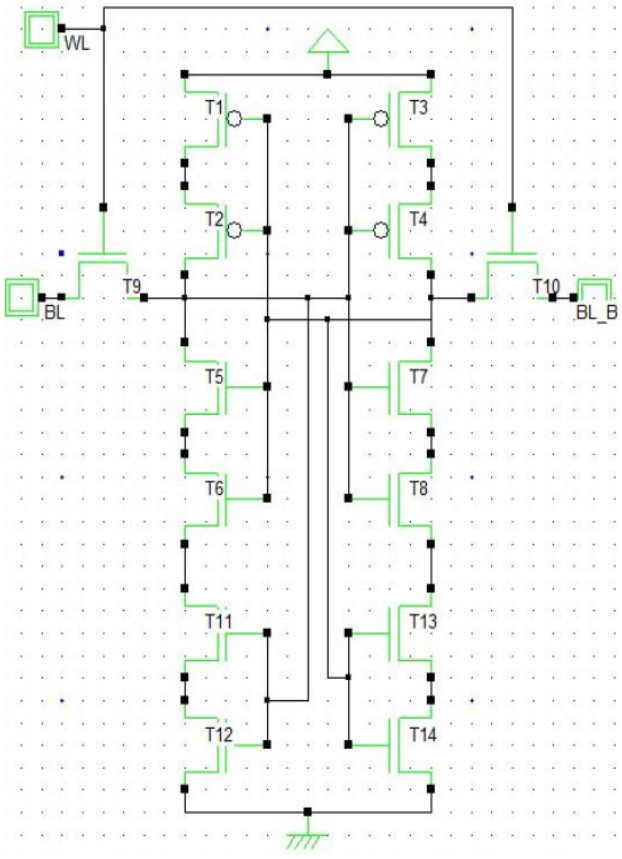

Figure 8. Schematic diagram of hybrid model SRAM cell

6. RESULTS

In this paper CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell designed using tanner tool and power consumption results are generated using t-spice at 180, 90, and 45 nm technology nodes. Table 1 represents the comparison table for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 180 nm technology. Figure 9 represents the

bar chart representation for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 180 nm technology. Different modes of operations of SRAM cell are taken on X-axis and power consumption in micro watts taken on Y-axis.

At 180 nm technology the hybrid model SRAM cell the Hold mode power consumption is 74.03% less than CMOS 6T SRAM cell, 39.97% less than the 8T CMOS SRAM cell and 37.14% less than the stacked CMOS SRAM cell, in Read mode power consumption is 79.4% less than CMOS 6T SRAM cell, 56.82% less than the 8T CMOS SRAM cell and 39.67% less than the stacked CMOS SRAM cell and in Write mode power consumption is 73.74% less than CMOS 6T SRAM cell, 51.17% less than the 8T CMOS SRAM cell and 20.21% less than the stacked CMOS SRAM cell.

Table 1. Power consumption results of different SRAM topologies at 180 nm technology

	Hold	Read 0	Read 1	Write 0	Write 1
6T SRAM cell	14.4	12.8	9.76	8.72	8.72
8T SRAM cell	6.23	6.46	3.58	4.69	4.69
Stacked SRAM cell	5.95	5.84	1.4	2.87	2.87
Hybrid SRAM cell	3.74	4.46	0.62	2.29	2.29

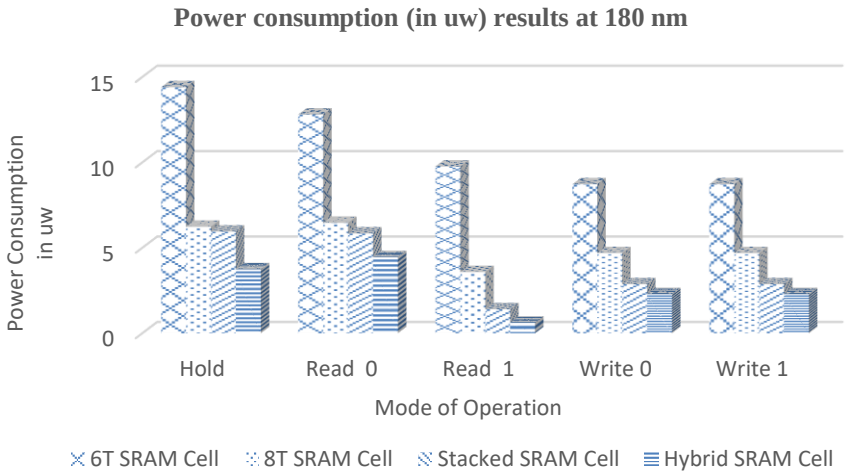

Figure 9. Power consumption results of different SRAM topologies at 180 nm technology

Table 2 represents the comparison table for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 90 nm technology. Figure 10 represents the bar chart representation for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 90 nm technology. Different modes of operations of SRAM cell are taken on X-axis and power consumption in micro watts taken on Y-axis.

At 90 nm technology the hybrid model SRAM cell the Hold mode power consumption is 77.57% less than CMOS 6T SRAM cell, 46.63% less than the 8T CMOS SRAM cell and 24.33% less than the stacked CMOS SRAM cell, in Read mode power consumption is 85.10% less than CMOS 6T SRAM cell, 53.33% less than the 8T CMOS SRAM cell and 48.17% less than the stacked CMOS SRAM cell and in Write mode power consumption is 84.51% less than CMOS 6T SRAM cell, 27.33% less than the 8T CMOS SRAM cell and 17.74% less than the stacked CMOS SRAM cell.

Table 3 represents the comparison table for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 45 nm technology. Figure 11 represents the bar chart representation for power consumption results in micro watts of CMOS 6T SRAM cell, 8T CMOS SRAM cell, stacked CMOS SRAM cell and hybrid model SRAM cell in Hold mode, Read mode and Write mode at 45 nm technology. Different modes of operations of SRAM cell are taken on X-axis and power consumption in micro watts taken on Y-axis.

Table 2. Power consumption results of different SRAM topologies at 90 nm technology

	Hold	Read 0	Read 1	Write 0	Write 1
6T SRAM cell	4.52	4.58	5.27	2.79	2.84
8T SRAM cell	1.9	1.97	0.82	0.6	0.60
Stacked SRAM cell	1.34	1.46	1.08	0.53	0.53
Hybrid SRAM cell	1.01	1.1	0.31	0.436	0.436

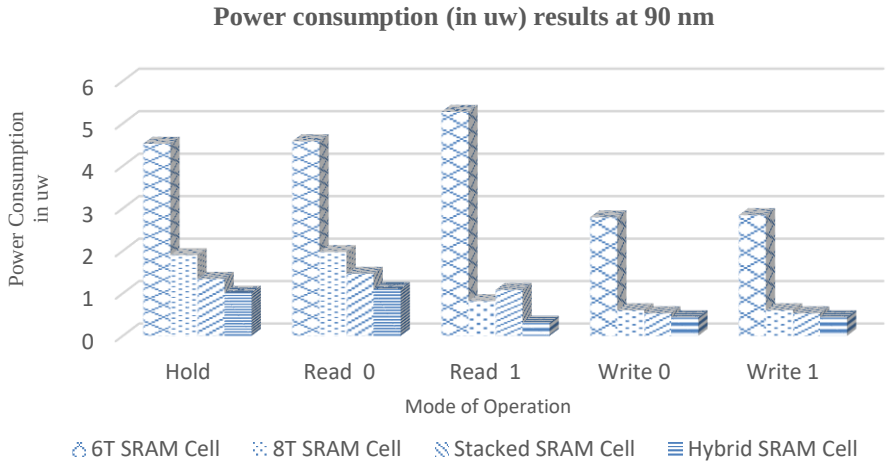

Figure 10. Power consumption results of different SRAM topologies at 90 nm technology

Table 3. Power consumption results of different SRAM topologies at 45 nm technology

	Hold	Read 0	Read 1	Write 0	Write 1
6T SRAM cell	1.41	1.41	1.04	0.75	0.75
8T SRAM cell	0.48	0.51	0.33	0.41	0.41
Stacked SRAM cell	0.41	0.44	0.06	0.16	0.16
Hybrid SRAM cell	0.25	0.27	0.01	0.11	0.11

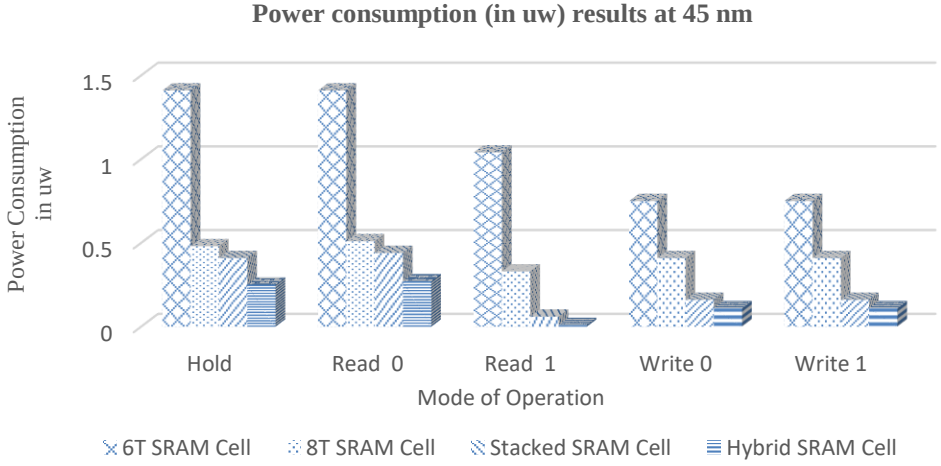

Figure 11. Power consumption results of different SRAM topologies at 45 nm technology

At 45 nm technology the hybrid model SRAM cell the Hold mode power consumption is 82.3% less than CMOS 6T SRAM cell, 47.9% less than the 8T CMOS SRAM Cell and 39% less than the stacked CMOS SRAM cell. In Read mode power consumption is 89.9% less than CMOS 6T SRAM cell, 72.01% less than the 8T CMOS SRAM cell and 60.98% less than the stacked CMOS SRAM cell. In Write mode power consumption is 85.3% less than CMOS 6T SRAM cell, 73.2% less than the 8T CMOS SRAM cell and 31.3% less than the stacked CMOS SRAM cell.

7. CONCLUSION

In this paper proposed hybrid model SRAM cell got less power consumption compared to the CMOS 6T SRAM cell, 8T CMOS SRAM Cell and stacked CMOS SRAM cell at three different technology nodes. The power results are simulated at 180, 90 and 45 nm technologies using tanner tool. At 180 nm technology hybrid model SRAM cell got average power consumption 75.72%, 49.32% and 32.34% less than the CMOS 6T SRAM cell, 8T CMOS SRAM Cell and stacked CMOS SRAM cell respectively. At 90 nm technology hybrid model SRAM cell got average power consumption 82.39%, 42.43% and 30.08% less than the CMOS 6T SRAM cell, 8T CMOS SRAM Cell and stacked CMOS SRAM cell respectively. At 45 nm technology hybrid model SRAM cell got average power consumption 85.83%, 64.37% and 43.76% less than the CMOS 6T SRAM cell, 8T CMOS SRAM Cell and stacked CMOS SRAM cell respectively. This low power SRAM cell is used in cache memory of CPU and accelerator for AI algorithms.

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BIOGRAPHIES OF AUTHORS

Seerapu Venkatesh is a research scholar from Andhra University Trans-Disciplinary Research HUB, Andhra University, presently working as an assistant professor at Engineering and Technology Program, Gayatri Vidya Parishad College for Degree and PG Courses (A) (GVPCDPGC (A)). He has completed his MTech in VLSI system design in 2012 and BTech in electronics and communication engineering in 2009. He has 11 years of teaching experience in various engineering colleges. He has eight research publications in international journals. His areas of research include VLSI design, low power VLSI. He is a member of IFERP and IAENG. He can be contacted at email: venkateshseerapu2019@gmail.com.

Krishna Veni Sahukara obtained her PhD in 2016 and Master of Technology in 2008 from Andhra University College of Engineering (A), Visakhapatnam. She has 15 years of teaching and research experience. Presently, she is working as a professor in the Department of ECE, GVPCDPGC(A), Visakhapatnam. She has published 25 research articles in various peer reviewed international journals and conferences. She has three patents. Her research interests include antenna arrays optimization, antenna design for 5G communications, EMI/EMC, internet of things and VLSI. She is a member of IEI and life member of SEMCE (India) and IETE. Currently, she is guiding seven research scholars. She can be contacted at email: drkrishnaveni@gvpcdpgc.edu.in.