Cascaded AC-DC parallel boost-flyback converter for power factor correction

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Article Info

ABSTRACT

A two-stage power factor correction (PFC) topology achieves a higher power factor quality and lower harmonic distortion than a single-stage converter. This paper introduces a two-stage PFC topology using a parallel boost and flyback converter which is employed as a voltage regulator The main boost converter is used for PFC and the other is the active filter circuit. The filter is implemented to improve the quality of phase-current and eliminate the switching loss. Furthermore, a reaction curve of Ziegler-Nichol's method determines the controller parameter for cascaded PFC converter circuit. Simulated and experimental results are presented to validate the proposed method. The total harmonic distortion (THD) value decreases significantly from 83.35% become 0.98% in the simulation. In addition, experimental results show that the current response has good performances, including less harmonics, higher power factor, and lower THD value compared to without a PFC circuit. The PF increased from 0.43 become 0.96, the THD value decreased from 49.4% become 16.2%, and contains a small number of harmonics. The proposed controller method has better responses than the conventional one, including small steady-state error, fast rise time and settling time. A microcontroller (MCU), type STM32F407VG, produced by STMicroelectronics is used to execute the proposed control in both converters.

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1. INTRODUCTION

Direct current (DC) voltage is gained over a rectifier. Then, the capacitor filter is necessary to produce a small ripple of DC voltage. However, the huge value of the capacitor leads to the current waveform being distorted and harmonics contaminated. The harmonics cause rapid deterioration and malfunction of electronic equipment, overheating, and the power factor is decreased [1], [2]. As the power factor decreases, power loss and harmonics increase causing other devices connected to the line to be interfered. In non-linear load, the power factor is influenced by the distortion factor and displacement power factor, which has quite a crucial impact on the system. Hence, a power factor correction (PFC) method was developed based on the standard of input current harmonics [3]–[6]. A PFC circuit utilizes the shapes of input current and voltage waveform to be in phase. Therefore, the system is considered a pure resistance load and

obtains a unity power factor even though a non-linear load is used [7]. Generally, the PFC method eliminates huge harmonics using an inductor filter with a hefty size. Hence, the PFC converter is classified into passive and active converters. The active PFC obtains a higher power factor, slighter size, and smaller form factor than the passive converter [8], [9]. The operation modes of active PFC converter are continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM) [10]. These modes are based on the inductor current flow. On the other hand, based on the stages number of converter type, an active PFC can be defined as a single-stage and a two-stage [11]. The single-stage achieves high power factor and efficiency but has an energy imbalance issue [12]. Thereafter, the two-stage PFC topology replaces the single-stage because it achieves a higher power factor and fulfills the harmonic standard regulation.

Many DC-DC converters can be used as PFCs, such as boost converters, buck converters, Cuk converters, and flyback [13], [14]. Boost converter is commonly used due to its simplicity, low cost, and ease of control [15]–[18]. Many researchers have examined boost converter utilization for PFC. For example, Ali *et al.* [19] proposed a three-phase boost converter using a proportional-integral and a resonant controller (PI-RC) controller. This system obtains a total harmonic distortion (THD) reduction of 1.68% and improves harmonics accentuation potency. A discontinuous conduction mode (DCM) flyback converter for the input voltage range of 90-264 V AC with an output voltage of 80 V DC was implemented in [20]. The system was operating in a constant duty cycle and offered the benefit of achieving a high-power factor using CRM combined with adaptive off-time (AOT). The results show that the efficiency is higher by 87.6% than the conventional one. The DC-DC buck-flyback PFC converter is proposed in [21]. The buck converter was employed as a PFC circuit in DCM mode. It obtained satisfactory performances, including small output voltage and current ripple, 91.08% efficiency, and 0.956 PF. Given the absence of previous studies regarding cascaded AC-DC PFC converters, this paper aims to address this research gap. It marks the inaugural investigation into this matter [1]-[21].

The outline of the primary contributions of this paper: i) a new two-stage PFC topology of parallel boost-flyback converter is proposed. The main PFC converter is a parallel boost converter, and the flyback converter is for the output voltage regulator; ii) a simple DCM mathematical analysis is proposed to design the parallel boost converter as the main PFC circuit; and iii) a simple PI controller design using Ziegler-Nichol's curve is proposed for the flyback converter. The curve of open-loop response determines the controller gain. The related PI gain is used when the open-loop response has no overshoot and oscillation. Compared to previous research [1]-[21], the ideas in this paper, which include the investigation of parallel boost and flyback converter for PFC systems with Ziegler-Nichols-based PI controller tuning, are original.

2. METHOD

The PFC system consists of a parallel boost converter and flyback converter in a series connection. The input voltage of the parallel boost converter is from the rectifier and step-down transformer. The configuration of the PFC system is shown in Figure 1. The details of DC-DC converters design used in the PFC systems are explained.
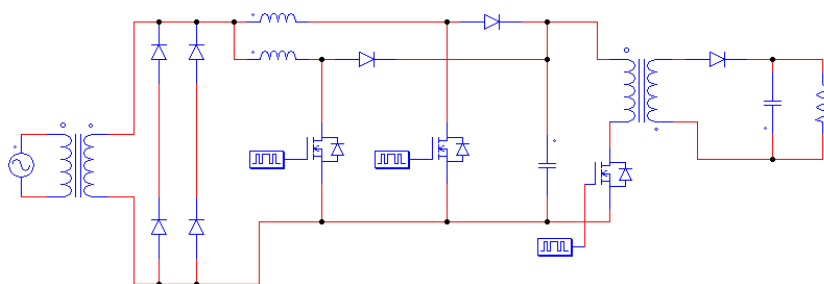

Figure 1. AC-DC parallel boost-flyback converter for PFC converter

2.1. Parallel boost converter

A parallel boost converter replaces a single boost converter for the PFC circuit. Figure 2 shows the parallel boost converter circuit. The switching control of the parallel boost converter is phase-shifted by 180º. The main topology of the boost converter is for the PFC circuit, and the additional circuit is for the active filter. The use of the filter is to improve the phase current quality and eliminate the switching loss. The PFC

boost converter analysis is in DCM in 3 steps [22]. Figure 3 shows the converter analysis when the switching component closed and the diode reversed.
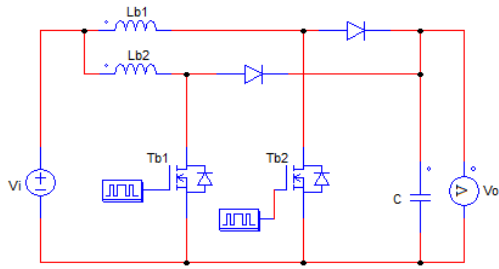

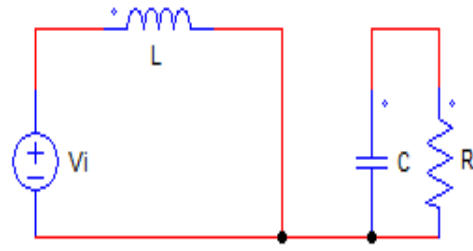Figure 2. DC-DC parallel boost converter topology

Figure 3. Switch closed and diode reversed

The analysis is derived as (1), (2):

$$V_L = V_i \tag{1}$$

$$i_c = \frac{-V_o}{R} \tag{2}$$

where V_L is the inductor voltage, i_c is the capacitor current, and R is the load. Second, Figure 4 shows the converter analysis when the switching component opened and the diode forwarded.
It is defined as (3), (4):

$$V_L = V_i - V_o \tag{3}$$

$$i_i = i_c + \frac{-V_o}{R} \tag{4}$$

where i_i is the input current. Figure 5 shows the last analysis when the switching component opened and the diode reversed. It is represented as (5), (6), (7),

$$V_L = 0 \tag{5}$$

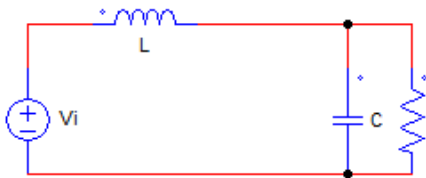$$i_i = 0 \tag{6}$$

$$i_c = \frac{-V_o}{R} \tag{7}$$

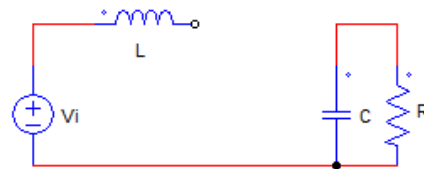Figure 4. Switch opened and diode forwarded

Figure 5. Switch opened and diode reversed

According to (1)-(7), the DCM mode responses are shown in Figure 6. Figure 6(a) shows the inductor voltage, Figure 6(b) presents inductor current, and Figure 6(c) demonstrates the diode current. To make the PFC model, the analysis can be derived as (8),

$$r_i = \frac{V_i}{i_i} \tag{8}$$

and

$$i_i = \frac{\left(\frac{1}{2}t\right)i_L DT}{T} \tag{9}$$

where V_i and i_i are the input voltage and current, i_L is the inductor current, r_i is the input resistance, D is the duty cycle of the parallel boost converter, and T is the load. Then, the inductor current i_L can defined as (10).

$$i_L = \frac{V_i}{L}DT \tag{10}$$

Substituting (10) into (9), one can derive.

$$i_i = \frac{V_i D^2 T}{2L} \tag{11}$$

By using (11) and substitute it into (8), yields

$$r_i = \frac{2L}{D^2 T} \tag{12}$$

where L is the inductor value. According to (12), the value of the inductor, duty cycle, and period are supposed to be constant. As a consequence, the input resistance is constant. Then, based on the boost converter analysis, the power factor become unity because the system supplied the resistive load. The output voltage can be defined as (13) [23].

$$V_o = \frac{V_i}{1-D} \tag{13}$$

In DCM mode, the inductor value is smaller than L^{min}, which can be defined as (14) [24].

$$L = \frac{1}{2}\frac{D(1-D)^2 R}{2f_{sw}} \tag{14}$$

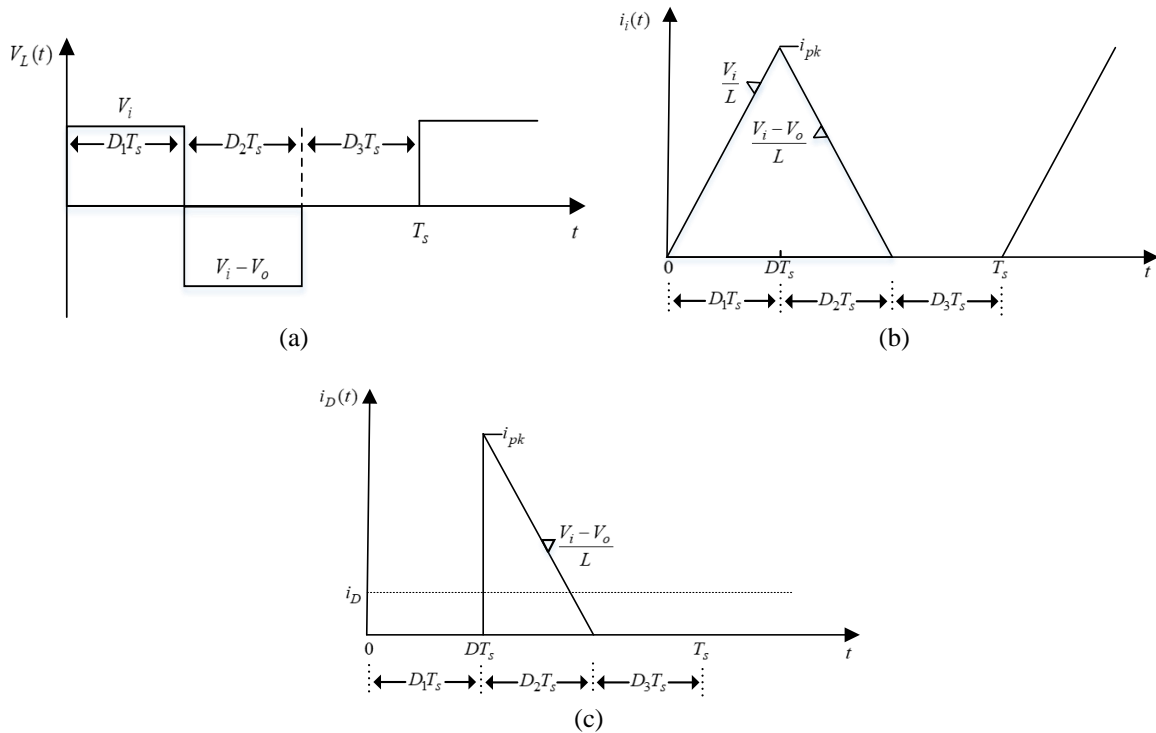where f_{sw} is the switching frequency.

Figure 6. The responses in DCM mode (a) inductor voltage (b) inductor current and (c) diode current

2.2. Flyback converter

The flyback converter is an isolated converter in which the circuit consists of a transformer and a switching component. Unlike an ideal transformer, the current does not flow simultaneously on the secondary side due to the reversed polarities of the transformer. The voltage source flows to the magnetization inductor when the switching component turns ON. Then, when the switching component is OFF, the voltage source flows to the load. The flyback converter is implemented as a voltage regulator in the system. The output voltage of flyback is defined as (15) [25],

$$V_{o\_flyback} = V_{i\_flyback}\left(\frac{D_{flyback}}{1-D_{flyback}}\right)\left(\frac{N^{sec}}{N^{prim}}\right) \tag{15}$$

where $V_{o\_flyback}$ and $V_{i\_flyback}$ are the output and input voltage of the flyback converter, $D_{flyback}$ is the duty cycle, N^{prim} is the primary winding of the transformer, and N^{sec} is the secondary winding of the transformer. The operation of the flyback converter is in continuous conduction mode (CCM). The value of the magnetization inductor is defined as (16) [26]:

$$L_m = \frac{V_{DC}^{\min} D_{flyback}^{\max}}{2 P i f_{sw} K_R} \tag{16}$$

where L_m is the magnetization inductor, V_{DC}^{min} is the minimum input voltage in the DC component, $D_{flyback}^{max}$ is the maximum duty cycle, P_i is the input power, and K_R is the ripple factor. Then, the maximum current through the switching component is derived as (17),

$$I_{\max} = 1.12\left(\Psi + \frac{\Pi}{2}\right) \tag{17}$$

According to (17), Ψ and Π are represented as (18),

$$\Psi = \frac{P_i}{V_{DC}^{\min} D^{\max}} \tag{18}$$

and,

$$\Pi = \frac{V_{DC}^{\min} D^{\max}}{L_m f_{sw}} \tag{19}$$

3. SIMULATED RESULTS

In this paper, a cascade PFC system uses mathematical analysis to obtain the value of each component. The simulation and controller design uses MATLAB Simulink. Figure 7 presents the block diagram of the PFC system. The supply of the PFC system is a 220 V source from the grid. Then, the voltage source is dismounted by low-frequency transformers becoming 32 V. In addition, the rectifier produces the DC voltage after the secondary side of the transformer. After that, the proposed DC-DC parallel boost – Flyback PFC converter improves the system quality. The parameters for the proposed system are described in Table 1.

For the controller design, the determination of the PI control parameter uses a Ziegler-Nichols method based on the reaction curve of an open-loop system. The plant is treated as an open-loop system subject to a unit step function signal. The system response will be an S-shape if the plant does not contain integrator elements or complex poles at a minimum. The S-shaped curve has two constants, which are dead time and time delay. The determination of proportional–integral–derivative (PID) parameters is based on obtaining these two constants. Therefore, the Zeigler-Nichols methods are easy to implement because it does not require complicated mathematical analysis. The reaction curve in open loop mode determines whether the system belongs to the 1st or 2nd order. The voltage response, which has no overshoot and oscillation, is assigned to be 1st order. As a result, the system only needs a PI controller. Then, the transfer function (TF) in open-loop mode can be obtained as (20):

$$\frac{Y(s)}{X(s)} = \frac{K}{\tau s + 1} \tag{20}$$

where $Y(s)$ is the output function, $X(s)$ is the input function, K is the constant, and τ is the time constant. According to (20), the settling time parameter determines the time constant as (21):

$$\tau = \frac{t_s}{5} \tag{21}$$

where t_s is the settling time.

Figure 8 shows the output voltage response of the flyback converter. Figure 8(a) shows the reaction curve in open-loop mode. The mathematical analysis of the response system determines the parameters of the PI controller. The proportional and integral gain is derived as (22), (23):

$$k_p = \frac{\tau_i}{\tau^* K} \tag{22}$$

$$k_i = \frac{k_p}{\tau_i} \tag{23}$$

where k_p is the proportional gain, k_i is the integral gain, τ_i is the integral time constant where the value is assumed $\tau_i = \tau$, and τ^* is the desired time constant. The difference between τ and τ^* is the settling time value. τ is obtained from the open-loop condition while τ^* is obtained based on the desired settling time, t_s. Figure 8(b) shows the response curve in a closed loop compared to Zieger-Nichol and the conventional method. Table 2 presents the comparison between the two methods. The responses show that the proposed method has better performance than the conventional method. The parameters include rise time, settling time, and error steady-state. According to Table 2, the Zieger-Nichol's has a faster rise time, faster settling time, and smaller error steady-state error than the conventional method. Then, the simulation of the integration system is also carried out in Figure 9. The simulation is conducted with two cases. The first case is the circuit with a rectifier and flyback converter only. Second, the complete circuit uses a PFC and regulator circuit without a DC-link capacitor on the rectifier side. Figure 9(a). shows the response without a PFC circuit at 50 Hz 220 V. As we can observe, the input current consists of a huge ripple and some points do not in phase with voltage responses. Such an input current response caused large harmonics in THD. Figure 9(b) shows the simulation result with PFC circuits. The voltage and current input have better responses compared with those without PFC circuits in Figure 9(a), including smaller input current harmonics and the responses tracked the input voltage as well. Figure 10 presents the harmonics spectrum of the input current side. In Figure 10(a) has a huge THD value of 83.35% when without a PFC circuit. When using the PFC circuit in Figure 10(b), as can be observed, the THD decreased significantly from 83.35% to 0.98%.
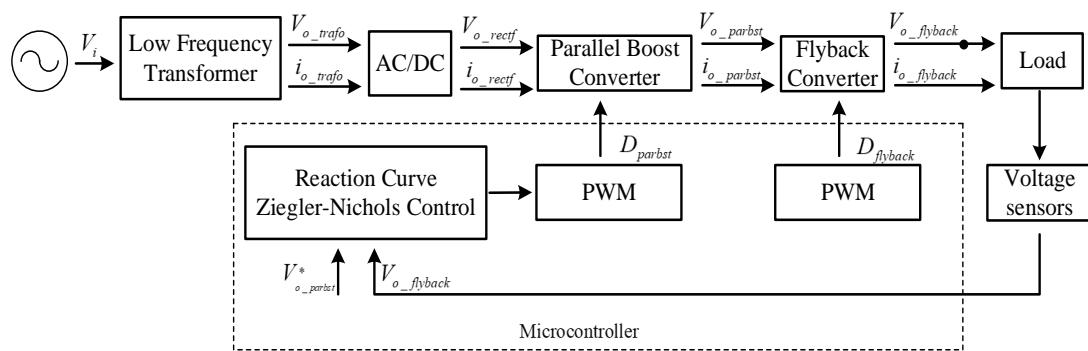

Figure 7. Block diagram of PFC system

Table 1. The parameter description

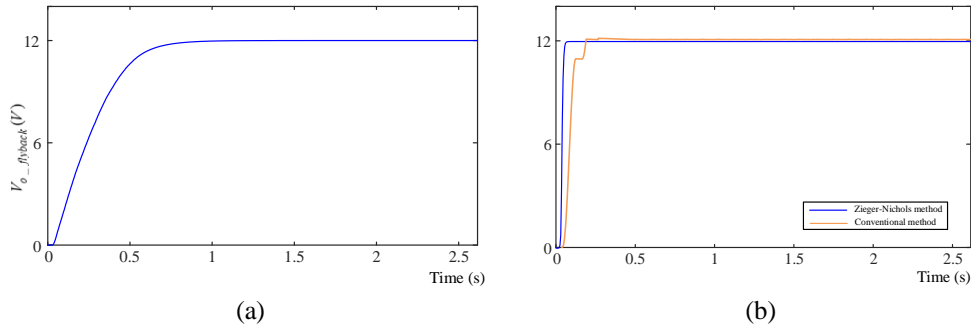| Parameters	Values	Parameters	Values	Parameters	Values	Parameters	Values
V_i	220 V	$V^*_{o\_flyback}$	12 V	i_{o_rectf}	1.651 A	f_{sw}	40 kHz
V_{o_trafo}	32 V	$i_{o\_flyback}$	3.3 A	V_o^{min}	40 V	K_R	0.5
i_{o_trafo}	5 A	D	0.52	V_o^{max}	60 V	B_{sat}	0.25 T
V_{o_rectf}	28.82 V	$D_{flyback}$	0.5	i_{o_boost}	0.78 A	A_c	1.96 cm² (PQ3535)

Figure 8. The output voltage response of flyback converter (a) open-loop and (b) closed-loop control

Table 2. The parameter comparison

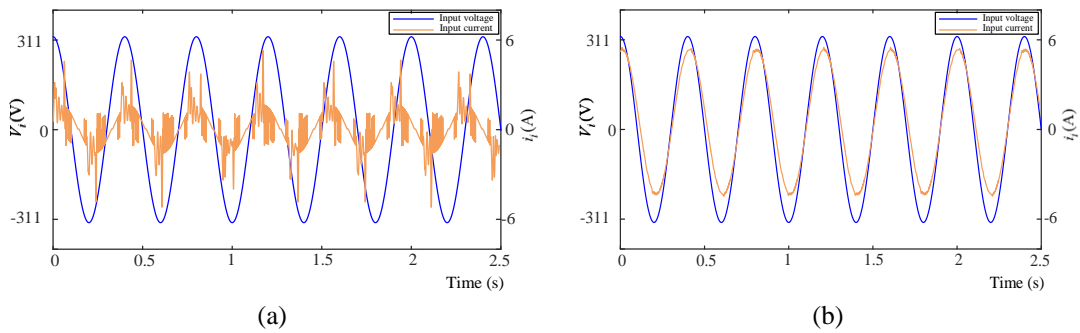|	Zieger- Nichols's method	Conventional method
Rise-time (s)	0.06	0.1
Settling time (s)	0.1	0.6
Error steady-state (%)	0.8	4.2

Figure 9. Simulation result (a) without PFC circuit and (b) with PFC circuit
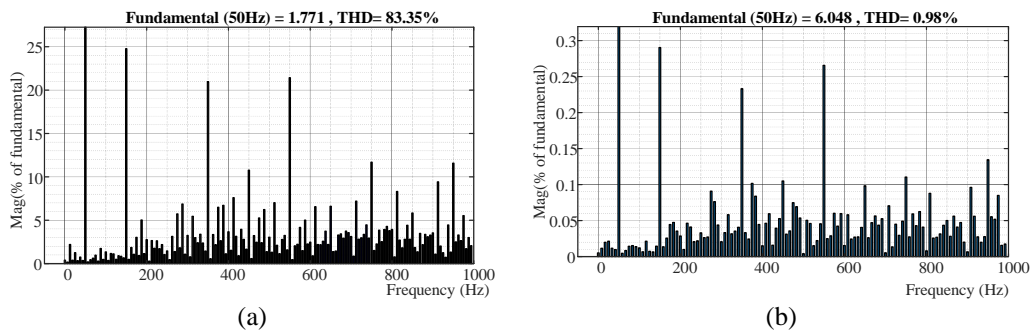

Figure 10. Simulation result of current input spectrum harmonics (a) without PFC circuit and
(b) with PFC circuit

4.   EXPERIMENTAL RESULTS

Figure 11 shows the photograph of the experimental bench test. A microcontroller unit (MCU) from STMicroelectronics, type STM32F407VG, is used to execute the proposed control for both converters. The duty cycle of the parallel boost converter is 52%. The voltage set point of the flyback converter is 12 volts due to the load requirement. Both converters use a 40 kHz switching frequency and a 25 µs sampling period. Power harmonic analyzer 43B is used to collect data and waveform in experimental results, such as voltage and current responses, THD, and PF values. Figure 12 demonstrates the voltage and current input responses with PFC and without PFC using 220 V, 100 W series load. Figure 12(a) shows the response of the

parameters without a PFC circuit. The current response with the PFC circuit in Figure 12(b) has better performances, including fewer harmonics, and the PF has significantly increased from 0.43 to 0.96. In addition, the input voltage is in phase with the input current waveforms when the PFC circuit is utilized. Figure 13 shows the current input spectrum harmonics responses. The THD value decreased from 49.4% in Figure 13(a) to 16.2% in Figure 13(b). Also, it contains fewer harmonics compared to those without a PFC circuit. Figure 14 shows the current and voltage waveforms when the system uses a couple of 220 V and 100 W loads in parallel. Figure 14(a) shows the waveform without a PFC circuit, in which the PF is 0.67, and its current harmonics are very high. On the other hand, as we can observe in Figure 14(b), the PF is increased to 0.96 when the PFC circuit is utilized. Therefore, the high current harmonics could affect the THD. Then, Figure 15 presents the harmonic responses of current input when the system uses a couple of 220 V, 100 W loads. Figure 15(a) shows the THD waveform without using a PFC circuit, which is 30%. Then, the THD decreased to 15.4% when using a PFC circuit, as shown in Figure 15(b). As a result, it proves that the parallel boost PFC circuit improves the performance of the system, including enhancement of power factor and suppression of THD, as shown in Table 3.
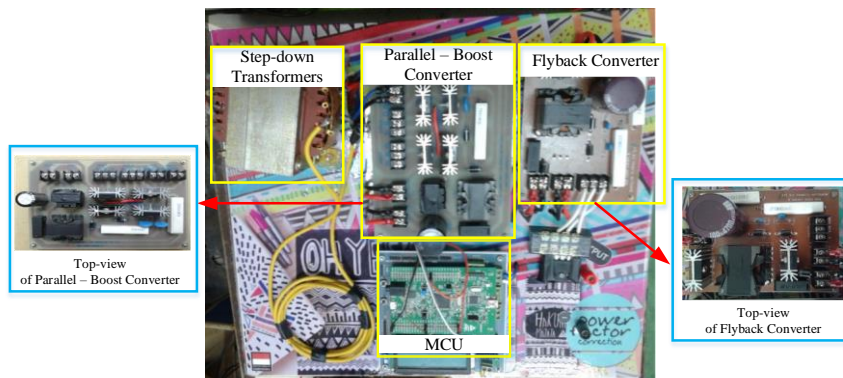

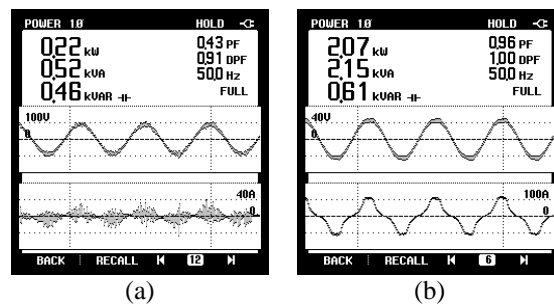Figure 11. Photograph of parallel boost-flyback PFC converter

(a)   (b)

Figure 12. The voltage and current responses using 220 V, 100 W load (a) without PFC circuit and (b) with proposed PFC circuit
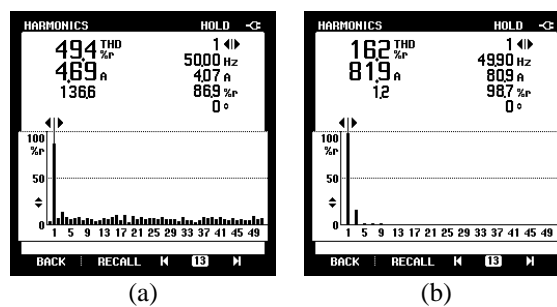

(a)   (b)

Figure 13. Responses of current input spectrum harmonics using 100 W load (a) without PFC circuit and (b) with proposed PFC circuit

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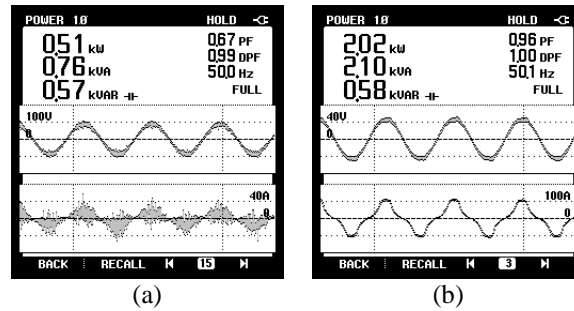
Figure 14. The voltage and current responses using a couple of 220 V, 100 W parallel load (a) without PFC circuit and (b) with proposed PFC circuit
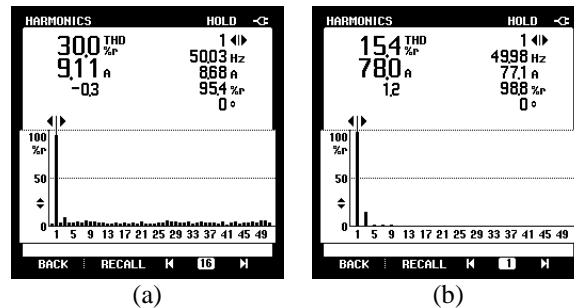

Figure 15. Responses of current input spectrum harmonics using a couple of 220 V, 100 W parallel load without PFC circuit and (b) with proposed PFC circuit

Table 3. The comparative result

Load	Without PFC circuit		With PFC circuit	
	THD (%)	PF	THD (%)	PF
Single 12 V, 20 W	43.1	0.74	16.1	0.95
A couple of 12 V, 20 W	35.7	0.75	15.3	0.95
Single 220 V, 100 W	49.4	0.43	16.2	0.96
A couple of 220 V, 100 W	30	0.67	15.4	0.96

5.   CONCLUSION

This paper introduced AC-DC parallel boost-flyback for the power factor correction converter. Improving from a single-stage to a two-stage PFC circuit using a parallel boost converter fulfills the harmonic standard regulation. In two-stage converter consists of a PFC parallel boost converter as the main stage and another flyback DC-DC converter as an additional converter. This additional converter could be a canceling line frequency ripple and voltage regulator. Simulated and experimental results show that the proposed PFC circuit has better performances, which are less current harmonics, higher PF, and lower THD value compared to those without the PFC system. In addition, compared with the conventional method, the Zieger-Nichols method has better performance, including faster rise time, faster settling time, and fewer steady-state errors. Therefore, the proposed reaction curve Ziegler-Nichols exhibits sufficient performance of power converter for industrial application.

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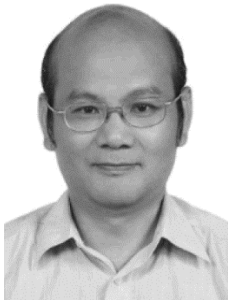
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