International Journal of Electrical and Computer Engineering (IJECE)
Vol. 15, No. 1, February 2025, pp. 208~223
ISSN: 2088-8708, DOI: 10.11591/ijece.v15i1.pp208-223

Optimizing power consumption in novel electrical design for single ended comparator circuit

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Article Info

Article history:

Received May 16, 2024
Revised Sep 17, 2024
Accepted Oct 1, 2024

Keywords:

Analog to digital converter
Complementary metal oxide semiconductor
Flash analog to digital converter
Single ended comparator
Switching voltage

ABSTRACT

Contemporary society electronic technology has evolved into a pivotal component across various facets of our lives. Its indispensability is particularly evident in the advancement of medical, agricultural, industrial, and other sectors. As this technology continues to play a crucial role, optimizing its performance in terms of speed, accuracy, and energy consumption becomes paramount. This paper introduces a novel electrical design for the threshold inverter quantization comparator circuit aiming to meet the evolving demands of modern electronic applications. The proposed design enhances the classic threshold inverter quantization comparator's performance by significantly reducing its power consumption. Through rigorous mathematical analysis and simulation results it is demonstrated that the proposed comparator design achieves a remarkable 50% reduction in power consumption compared to the conventional threshold inverter quantization comparator. Subsequently the newly devised design is applied to the construction of a 4-bit flash analog-to-digital converter using 0.35 μm complementary metal–oxide–semiconductor (CMOS) technology.

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1. INTRODUCTION

The comparator is the basic element in building analog-to-digital converters (ADCs). The ADC is the bridge between the digital systems and the real world. The astonishing demand for high performance ADCs is pushing towards designing new comparator topologies to optimize power dissipation, size and speed trade-offs. The comparator is an electrical circuit that is used in comparing two input signals and produces a digital output signal, which its value depends on the comparison result. The comparator could be a voltage comparator or a current comparator according to the comparison technique that has been used. Voltage comparators are more popular than current comparators because it is easier to distribute voltage rather than current. Voltage comparators could be classified into three main types; the open loop comparator [1], pre-amplifier latched comparator [2]–[5], and full dynamic latched comparator [6]–[9]. A single comparator could be considered a 1-bit ADC. The performance of the comparator has a consequential effect on the overall performance of the ADC [10]. Power consumption, size and DC bias requirements in ADCs are a prime concern for mobile devices and standalone systems. Lowering the power consumption, decreasing the size and eliminating the need for different bias voltages by using a new type of comparators which are called single ended comparators is the key answer to these issues.

In their paper, Rai *et al.* [11] designed a 5-bit flash ADC using the threshold inverter quantization (TIQ) method to achieve high speed and low power consumption. The ADC is implemented in 0.18 μm

complementary metal–oxide–semiconductor (CMOS) technology with a system voltage of 1.8 V. The design incorporates a multiplexer as a code converter to enhance speed. The authors conducted a comparative analysis among various ADCs. Power dissipation, differential non-linearity (DNL), integral non-linearity (INL), and gain error were assessed. They found that their proposed ADC outperforms traditional ADCs in terms of speed and power efficiency. Specifically, the TIQ-based design eliminates the need for a passive resistor array for reference voltage. The results showed improved performance with lower power dissipation. Their design is suitable for modern communication systems that demand high-speed and low-power ADC solutions.

The comparator is the basic element in building ADCs. The astonishing demand for high-performance ADCs is pushing towards designing new comparator topologies to optimize power dissipation, size, and speed trade-offs. In their paper, Pavan *et al.* [12] designed a 5-bit flash ADC utilizing 45 nm CMOS technology. The design consists of a binary encoder, comparator, resistive ladder network, and thermometer code generation. The comparator is an operational amplifier that goes through two stages. Optimizing the encoder circuit to increase bit count while lowering power consumption was the main goal. In order to do this, the authors used CMOS, pass transistor, and transmission gate logic to construct a 2:1 multiplexer-based encoder. The results demonstrated significant improvements in resolution and power efficiency. The study successfully demonstrated that a well-optimized encoder could significantly reduce power consumption and improve overall performance in Flash ADC designs.

A current comparator using source coupled logic (SCL) and positive feedback source coupled logic (PFSCL) styles was designed by Bhatia *et al*. [13]. The designed comparator comprises three stages: a current-to-voltage converter, an SCL inverter, and a PFSCL inverter. The design was Implemented using 0.18 μm Taiwan semiconductor manufacturing company (TSMC) CMOS technology. After conducting simulations to evaluate the comparator's performance, they found that their design achieved a power consumption of 28 μW. The design is highly suitable for current mode ADC applications.

There are several types of comparators used in literature. Time-interleaved analog-to-digital converters are common [14]. They often suffer from timing mismatches at high frequencies. Recent work has addressed this issue. Σ-Δ ADCs are also used in many applications, such as ECG signals [15]. Their complexity and high-power consumption are drawbacks. Recent efforts have improved DC Σ-Δ ADCs for ECG signals. These circuits, and many others, use complementary metal oxide transistors [16].

The single ended comparator compares the analog input signal with the switching voltage. The variation of the switching voltage values is made by the variation in the length and the width of the P-type metal oxide semiconductor (PMOS) and the N-type metal oxided semiconductor (NMOS) transistor of the comparator [17]. In flash ADCs a resistor array circuit is used in order to provide the variation in the reference voltage. By using the single ended comparator the resistor array circuit is eliminated, which can be considered as a great improvement to the flash ADC [18]. Also, the sample and hold circuit will be eliminated, thus will reduce the power dissipation and the size of the comparator. An N-bit flash ADC requires a $2^N - 1$ different reference voltages, thus a $2^N - 1$ comparators with different switching voltages are needed.

The use of conventional TIQ comparators has been effective. Unfortunately, the conventional TIQ comparators often suffer from high power dissipation. The key issues include high short-circuit power dissipation, dynamic power consumption, and leakage power.

Single ended comparator circuit could be modified by using a cascaded stage of a CMOS inverter, this circuit called the TIQ comparator [18]–[23]. The TIQ comparator enhances the accuracy of the single ended comparator. The accuracy of the TIQ comparator can be furthermore improved by connecting another TIQ as a second stage. The cost of improving the accuracy is an increase the power dissipation and an increase in the area of the comparator [24]–[26]. To reduce the power dissipation for the TIQ comparator an NMOS and a PMOS transistor are added and both act as a resistive loads [27], [28]. This circuit reduces the power dissipation but it also reduces the gain. In order to achieve both high gain and low power dissipation a new TIQ topology is proposed in this paper. The mathematical analysis and simulation result will show that the proposed TIQ comparator reduces the power dissipation of the classic TIQ comparator to half while having the same gain.

We introduce a novel design for the TIQ comparator that significantly reduces power dissipation by 50% compared to the classic TIQ comparator. The design maintains the same gain. This efficiency is achieved by utilizing stacked NMOS and PMOS transistors. Additionally, the new TIQ design is applied to a 4-bit flash ADC. By implementing the 4-bit flash ADC using the designed comparator demonstrates an improved performance metrics.

This paper will be organized as follows: section 2 of this paper reviews the operation of the classic TIQ comparator and the analysis of its gain and power dissipation. The mathematical gain and power dissipation analysis of the proposed TIQ comparator and it is operation will be shown in also in section 2. In section 2 the proposed TIQ is employ in a 4-bit flash ADC. The simulation result of the proposed comparator

design and the 4-bit flash ADC employ the propose comparator will be discussed in section 3, finally the conclusion in section 4.

2. METHOD

In single ended comparators the input signal is compared with the switching voltage of the inverter. If the input signal is higher than the switching voltage the output of the comparator is "1" otherwise, the output of the comparator is "0". One of the most popular single ended comparator designs is the TIQ comparator, which is shown in Figure 1. The first stage is used to select the quantization level, while the second stage is used to amplify the gain of the comparator.

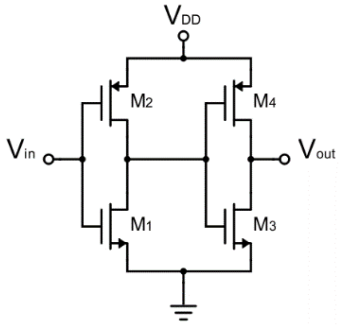


Figure 1. Classic TIQ comparator

In the first stage, the quantization level is determined by adjusting the width and length of the PMOS and the NMOS. Usually, the lengths of both NMOS and PMOS transistors are equal so, the quantization level depends only on the width of the transistors. Since the mobility of the electrons is greater than the mobility of the holes by a factor of three, the switching voltage is equal to:

$$V_{SP} = \frac{\sqrt{\frac{3W_2}{W_1}}(V_{DD}-V_{tp})+V_{tn}}{1+\sqrt{\frac{3W_2}{W_1}}} \quad (1)$$

where, V_{SP}, V_{thp}, V_{thn}, W_1, and W_2 are the switching voltage, the PMOS threshold voltage, NMOS threshold voltage, width of the transistor M_1 and M_3 and width of the transistor M_2 and M_4. The next subsections show the mathematical analysis of the gain and power consumption of the classic TIQ comparator.

2.1. Gain analysis for the classic TIQ comparator

The small signal equivalent circuit for the TIQ comparator in Figure 1 is shown in Figure 2, which can be used to find the gain of the can TIQ comparator.

$$v_{out} = \left(gm_4.v_{sg4} - gm_3.v_{gs3}\right).(r_{o3}||r_{o4}) \quad (2)$$

$$v_{gs3} = -v_{gs4} = \left(gm_2.v_{gs2} - gm_1.v_{gs1}\right).(r_{o1}||r_{o2}) \quad (3)$$

$$v_{gs1} = -v_{gs2} = v_{in} \quad (4)$$

Substituting the value of vin from (4) into (3):

$$v_{gs3} = -v_{sg4} = -v_{in}(gm_1 + gm_2)(r_{o1}||r_{o2}) \quad (5)$$

By substituting (5) into (2) the gain of the TIQ comparator is found to be:

$$A_v = \begin{bmatrix}(gm_2 + gm_1).(gm_3 + gm_4) \\ .(r_{o1}||r_{o2}).(r_{o3}||r_{o4})\end{bmatrix} \quad (6)$$

Both branches have the same switching voltage, thus, the transconductance of transistors M_1 and M_3 is equal to:

$$g_{m1} = g_{m3} = 2c_{ox}\mu_n \left(\frac{W}{L}\right)_n \left[V_{sp} - V_{thn}\right] \quad (7)$$

The transconductance of transistors M_2 and M_4 is equal to:

$$g_{m_2} = g_{m4} = 2c_{ox}\mu_p \left(\frac{W}{L}\right)_p \left[V_{DD} - V_{sp} - |V_{thp}|\right] \quad (8)$$

The finite output resistance of transistors M_1 and M_3 is equal to:

$$r_{o1} = r_{o3} = \frac{1}{\lambda c_{ox}\mu_n [V_{sp} - V_{thn}]^2} . \left(\frac{L}{W}\right)_n \quad (9)$$

The finite output resistance of transistors M_2 and M_4 is equal to:

$$r_{o2} = r_{o4} = \frac{1}{\lambda c_{ox}\mu_p [V_{DD} - V_{sp} - |V_{thp}|]^2} . \left(\frac{L}{W}\right)_p \quad (10)$$

Thus, the gain is equal to:

$$A_v = \left[\left(gm_{2,4} + gm_{1,3}\right).\left(r_{o2,4} || r_{o1,3}\right)\right]^2 \quad (11)$$

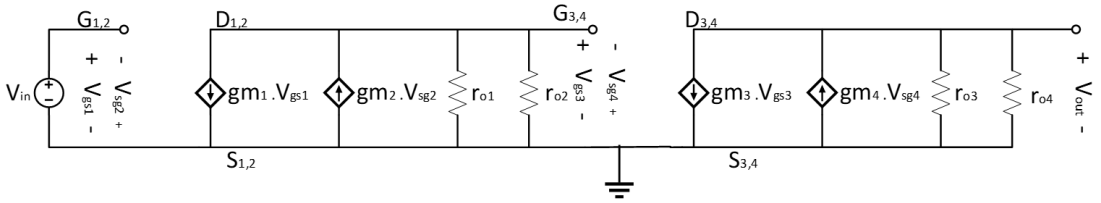


Figure 2. Small signal equivalent circuit of classic TIQ comparator

2.2. Power consumption analysis of the classic TIQ comparator

There are three type of power consumption that contribute the total power dissipation of the TIQ comparator. The short circuit power dissipation P_{SC}, the dynamic power dissipation P_D and the leakage power dissipation P_L. The leakage power dissipation has a neglected effect in the total power dissipation which equal to:

$$P_{total} = P_{SC} + P_D \quad (12)$$

2.2.1. Short circuit power dissipation

When both of the PMOS and the NMOS transistors are simultaneously on, a direct current path between the power supply and ground will be built which lead to produce a static power dissipation called short-circuit power dissipation. This direct path is built when the input voltage equal to $V_{thn} < V_{in} < V_{DD} - V_{thp}$. The short-circuit power dissipation is found using two methods; the square-law MOS models and the α-power metal oxide semiconductor field effect transistor (MOSFET) model. In this research, the square-law MOS models will be used.

Let us assume that the input voltage is a pulse function with rising and falling delay time equal to $\tau_r = \tau_f = \tau$ And it has a period time equal to T as shown in Figure 3. Also, let us assume that the switching point voltage equal to 0.5 V_{DD}. Then, the time that takes short circuit current to increase from its minimum value to its maximum value will equal to the time that take the short circuit current it decrease from its maximum value to its minimum value which equal $t_2 - t_1$. During $t_2 - t_1$. Period the NMOS transistor M_1 will be in the saturation region and the first stage short circuit current will equal to:

$$I_{S.C1} = c_{ox}\mu_n \left(\frac{W}{L}\right)_n . [V_{GS} - V_{thn}]^2 \quad (13)$$

The average short circuit current of the first stage will equal to:

$$I_{avg1} = 2.\frac{2}{T}.\int_{t_1}^{t_2} c_{ox}\mu_n\left(\frac{W}{L}\right).[V_{GS} - V_{thn}]^2.dt \quad (14)$$

where:

$$V_{GS} = V_{in} = \frac{V_{DD}}{\tau}.T \quad (15)$$

$$t_1 = \frac{V_{thn}.\tau}{V_{DD}} \quad (16)$$

$$t_2 = \frac{[V_{DD} - |V_{thp}| + V_{thn}].\tau}{2.V_{DD}} \quad (17)$$

To simplify the derivation, let assume $|V_{thp}|$=V_{thn}, the average first stage short circuit current will equal to:

$$I_{avg1} = \frac{4K_n}{T}.\int_{\frac{V_{thn}}{\tau}}^{\frac{\tau}{2}}\left[\frac{V_{DD}}{\tau}.t - V_{thn}\right]^2 dt$$

$$I_{avg1} = \frac{c_{ox}\mu_n.\tau}{6.V_{DD}.T}.\left(\frac{W}{L}\right)(0.5V_{DD} - V_{thn})^3 \quad (18)$$

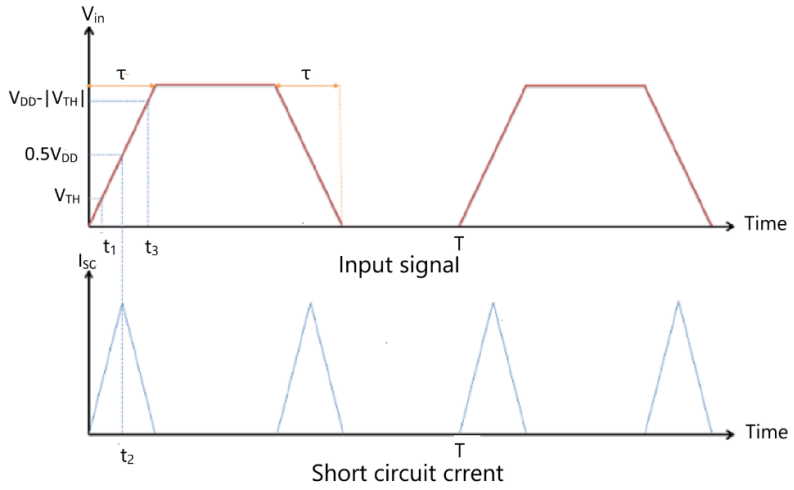


Figure 3. Short circuit current of the TIQ comparator

The short circuit current of the second stage will be equal to the drain current of the PMOS transistor M_4, the PMOS transistor M_4 act in the saturation region during the time between t_1 and t_2. The input voltage of the transistor M_4 is the first stage output $\bar{V}_{out}$. The first stage output during the time t_1 and t_2 will equal to:

$$\bar{V}_{out} = V_{in} - V_{thp} + \sqrt{V_{DD}^2 - 2V_{in}.V_{DD} + 2.V_{DD}.V_{thp}} \quad (19)$$

The second stage short circuit current during the time between t_1 and t_2 is equal to:

$$I_{SC2} = c_{ox}\mu_p\left(\frac{W}{L}\right)_P.\left[V_{DD} - \bar{V}_{out} - |V_{thp}|\right]^2 \quad (20)$$

The average short circuit current of the second stage is equal to:

$$I_{avg2} = \frac{4c_{ox}\mu_p}{T}.\left(\frac{W}{L}\right)_P\int_{t_1}^{t_2}\left[V_{DD} - \bar{V}_{out} - |V_{thp}|\right]^2 dt$$

$$I_{avg2} = \frac{4c_{ox}\mu_p\tau}{T}.\left(\frac{W}{L}\right)_P.V_{DD}^2\begin{bmatrix}\frac{1}{3}\left(1-\frac{V_{thn}}{V_{DD}}\right)^3+\left(\frac{V_{thn}}{V_{DD}}\right)^2\\-\frac{2V_{thn}^2}{V_{DD}}-0.325+\frac{2V_{thn}}{3V_{DD}}\\-\frac{2}{15}\left(\frac{2V_{thn}}{V_{DD}}\right)^{\frac{5}{2}}+\left(\frac{2V_{thn}}{V_{DD}}\right)^{\frac{3}{2}}\end{bmatrix} \quad (21)$$

The total short circuit power dissipation will be equal to:

$$P_{SC} = V_{DD}.\left(I_{avg1}+I_{avg2}\right) \quad (22)$$

It can be notes from equation above that the short circuit positively depends on the transistor size, the transistor threshold voltage and the input signal speed.

2.2.2. Dynamic power consumption of the classic TIQ comparator

Dynamic power refers to the power that dynamically varies with time. In the classic TIQ comparator circuit the dynamic power consumption is produced from charging and discharging the output load. Let assume that the output load is equal to c_{load}, as shown in Figure 4, and the input voltage is a pulse wave with period time equal T. When the input voltage moves from zero to V_{DD}, the loaded capacitor will start to charge its voltage from zero to V_{DD}, the output load charging power consumption equal to:

$$P_{charge} = \frac{1}{T}.\int_0^{\frac{T}{2}} i_{out1}(t).[V_{DD}-V_{out}].dt \quad (23)$$

where

$$i_{out}(t) = c_{load}\frac{d(V_{DD}-V_{out})}{dt} \quad (24)$$

So, the average charging dynamic power consumption will equal to:

$$P_{charge} = \frac{1}{T}\int_0^{\frac{T}{2}} c_{load}\frac{d(V_{DD}-V_{out})}{dt}(V_{DD}-V_{out}).dt$$
$$P_{charge} = \frac{1}{2T}c_{load}V_{DD}^2 \quad (25)$$

The output will discharge to zero when the input signal move from V_{DD} to zero, the discharging power consumption will equal to:

$$P_{dischage} = \frac{1}{T}\int_{\frac{T}{2}}^{T} i_{out2}(t)V_{out}dt \quad (26)$$

where

$$i_{out2}(t) = -c_{load}\frac{dV_{out}}{dt} \quad (27)$$

By substitution (28) in (27), the average discharging power consumption will equal to:

$$P_{discharge} = \frac{1}{T}\int_{\frac{T}{2}}^{T} -C_{load}\frac{dV_{out}}{dt}dt$$
$$P_{discharge} = \frac{1}{2T}c_{load}V_{DD}^2 \quad (28)$$

The average dynamic power dissipation will equal to:

$$P_D = P_{charge} + P_{discharge}$$
$$P_D = \frac{1}{T}c_{load}V_{DD}^2 \quad (29)$$

It could be noted that dynamic power consumption is independent of the circuit design. Dynamic power consumption depends positively on the input signal speed and the output load.

2.3. Proposed TIQ comparator design

The proposed low power dissipation TIQ comparator is shown in Figure 4. The schematic captured from the simulator for the proposed TIQ comparator is shown in Figure 5. The circuit is implemented in 0.35 um technology. The symmetrical NMOS transistors Q1, Q3 act as a single NMOS transistor, called stacked NMOS transistor, where the width of this transistor has the same width of transistors Q1 and Q3 but the length of this transistor is double the length of transistors Q1 and Q3. The same thing for the PMOS transistors Q2 and Q4 act as a single PMOS transistor, called stacked PMOS transistor. The stacked transistor idea is employed to reduce the power dissipation of the classic TIQ comparator to half without any effect in the comparator gain as will be proven in the next subsections.

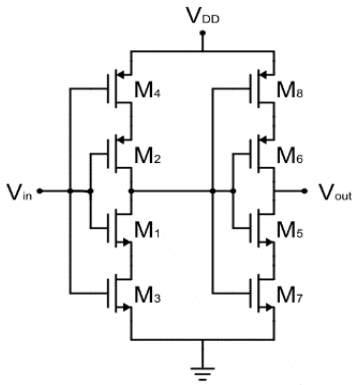


Figure 4. Proposed TIQ comparator circuit

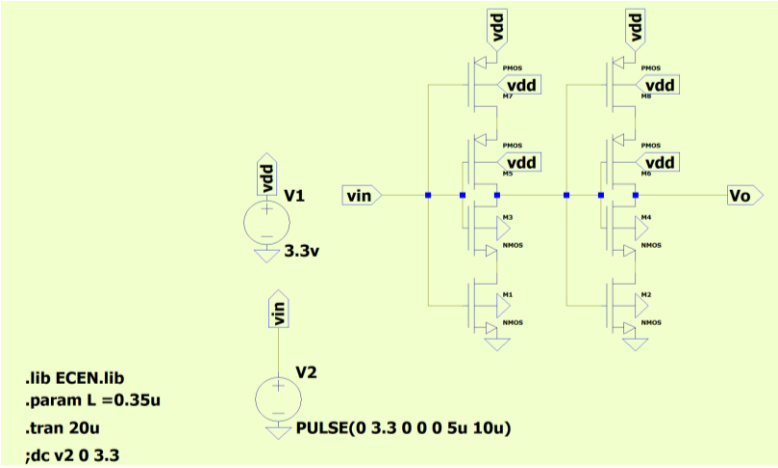


Figure 5. Schematic of the proposed TIQ comparator

2.3.1. Gain analysis for the proposed TIQ comparator

The equivalent circuit of the proposed TIQ comparator is shown in Figure 6, where the stacked NMOS $S1$ and $S3$ transconductance is equal to:

$$gm_{s1} = gm_{s3} = 0.5gm_{n1,3,5,7}$$
$$gm_{s1} = gm_{s3} = 2c_{ox}\mu_n\left(\frac{W}{2L}\right)_n\left[V_{sp} - V_{thn}\right] \quad (30)$$

And the transconductance of the stacked PMOS transistor $S2$ and $S4$ is equal to:

$$gm_{s2} = gm_{s4} = 0.5gm_{p2,4,6,8}$$
$$gm_{s2} = gm_{s4} = 2c_{ox}\mu_p\left(\frac{W}{2L}\right)_p\left[V_{DD} - V_{sp} - |V_{thp}|\right] \quad (31)$$

The finite output resistance of NMOS stacked transistors $S1$ and $S3$ is equal to:

$$r_{os1} = r_{os3} = 2r_{on1,3,5.7}$$
$$r_{os1} = r_{os3} = \frac{1}{\lambda c_{ox}\mu_n[V_{sp}-V_{thn}]^2}.\left(\frac{2L}{W}\right)_n \quad (32)$$

The finite output resistance of PMOS stacked transistors $S2$ and $S4$ is equal to:

$$r_{os2} = r_{os4} = 2r_{op2,4,6,8}$$
$$r_{os2} = r_{os4} = \frac{1}{\lambda c_{ox}\mu_p[V_{DD}-V_{sp}-|V_{thp}|]^2}.\left(\frac{2L}{W}\right)_p \quad (33)$$

The small signal equivalent circuit of the circuit shown in Figure 5 is shown in Figure 6. The gain of this circuit is equal to:

$$A_v = \left[\left(gm_{s2,s4} + gm_{s1,s3}\right).\left(r_{os2,s4}||r_{os1,s3}\right)\right]^2$$
$$A_v = \left[\left(0.5gm_{2,4,6,8} + 0.5gm_{1,3,5,7}\right).\left(2r_{o2,4,6,8}||2r_{o1,3,5,7}\right)\right]^2$$
$$A_v = \left[\left(gm_{2,4,6,8} + gm_{1,3,5,7}\right).\left(r_{o2,4,6,,8}||r_{o1,3,5,7}\right)\right]^2 \quad (34)$$

From (34) it can be noted that the proposed TIQ comparator has the same gain as the classic TIQ comparator.

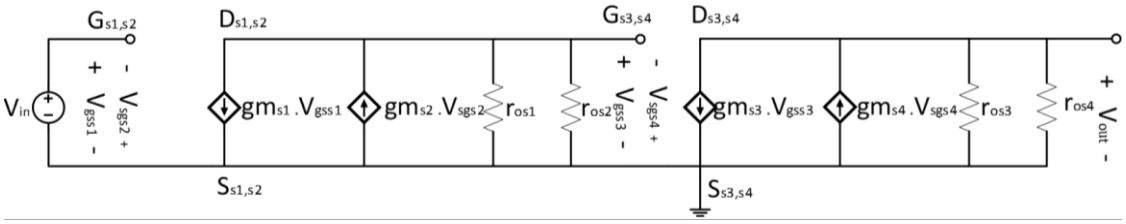


Figure 6. Small signal equivalent circuit of the proposed TIQ comparator

2.3.2. Power consumption analysis for the proposed TIQ comparator

From the previous section, there are two affected types of power consumption that contribute to the total power dissipation of the comparator: short circuit power consumption and the dynamic power dissipation. The dynamic power dissipation depends on the output load and the input signal speed only, does not depend on the circuit design. While the short circuit current is affected positively with the width to the length ratio of each transistor. As mention before, the proposed TIQ comparator double the length of each transistor. Let us consider the effect of this in the short circuit power consumption.

As the assumption in section 2, the input voltage is a pulse function with rising and falling delay time equal to $\tau_r = \tau_f = \tau$ and it has a period time equal to T. The stacked NMOS transistor $S1$ will be in the saturation region during the time between t_1 and t_2, shown in Figure 3, the first stage short circuit current during this period is equal to:

$$I_{S.CP1} = c_{ox}\mu_n\left(\frac{W}{2L}\right)_n.[V_{GS} - V_{thn}]^2 \quad (35)$$

The average first stage short circuit current is equal to

$$I_{avgP1} = 2.\frac{2}{T}.\int_{t_1}^{t_2} c_{ox}\mu_n\left(\frac{W}{2L}\right).[V_{GS} - V_{thn}]^2.dt$$
$$I_{avgP1} = \frac{c_{ox}\mu_n.\tau}{12.V_{DD}.T}.\left(\frac{W}{L}\right)(0.5V_{DD} - V_{thn})^3 \quad (36)$$

It can be seen from (36) and (18) that the average first stage short circuit current of the proposed TIQ comparator is half the average first stage short circuit current of the classic comparator.

$$I_{avgP1} = 0.5I_{avg1} \quad (37)$$

The PMOS stacked transistor $S4$ will be at the saturation region during the time between t_1 and t_2. Thus, the second stage short circuit current during the time between t_1 and t_2 is equal to:

$$I_{SCP2} = c_{ox}\mu_p \left(\frac{W}{2L}\right)_P . \left[V_{DD} - \bar{V}_{out} - \left|V_{thp}\right|\right]^2 \tag{38}$$

The average short circuit current of the second stage is equal to:

$$I_{avgP2} = \frac{4c_{ox}\mu_p}{T} . \left(\frac{W}{2L}\right)_P \int_{t_1}^{t_2} \left[V_{DD} - \bar{V}_{out} - \left|V_{thp}\right|\right]^2 dt$$

$$I_{avgP2} = \frac{2c_{ox}\mu_p\tau}{T} . \left(\frac{W}{L}\right)_P . V_{DD}^2 \begin{bmatrix} \frac{1}{3}\left(1 - \frac{V_{thn}}{V_{DD}}\right)^3 + \left(\frac{V_{thn}}{V_{DD}}\right)^2 \\ -\frac{2V_{thn}^2}{V_{DD}} - 0.325 + \frac{2V_{thn}}{3V_{DD}} \\ -\frac{2}{15}\left(\frac{2V_{thn}}{V_{DD}}\right)^{\frac{5}{2}} + \left(\frac{2V_{thn}}{V_{DD}}\right)^{\frac{3}{2}} \end{bmatrix} \tag{39}$$

Also, the average second stage short circuit current of the proposed TIQ comparator is equal to half the average second stage short circuit current.

$$I_{avgP2} = 0.5 I_{avg2} \tag{40}$$

Let us consider the effect of the proposed TIQ comparator in the short circuit power dissipation.

$$\frac{P_{SCP}}{P_{SC}} = \frac{V_{DD}.(0.5I_{avg1} + 0.5I_{avg2})}{V_{DD}.(I_{avg1} + I_{avg2})} = 0.5 \tag{41}$$

As can be seen in (41), the proposed TIQ comparator reduces the short circuit power dissipation of the classic TIQ comparator to half. The proposed TIQ comparator has no effect in the dynamic power dissipation of the classic TIQ comparator, because the dynamic power consumption is independent of the circuit design.

2.4. 4-Bit flash ADC employing the proposed TIQ comparator

Usually, the flash ADC is consists of three phases; the sample and hold phase, quantization phase and the encoding phase. This is not the case when the TIQ comparator is employed in the flash ADC design, because TIQ comparator eliminates the need of sample and hold phase. Not only the sample and hold phase will be eliminated when the TIQ comparator is employed in the flash ADC design; also, the resister array circuit will be eliminated. This will reduce the size, the design complexity and the power dissipation of the ADC. The flash ADC employ TIQ comparator consist of two stages are the quantization stage and the encoding stage.

The quantization stage will be built only from the TIQ comparators. For N-bit flash ADC, $2^N - 1$ TIQ comparators with different switching voltages are requiring. The switching voltage could be adjusted by varying PMOS transistor to NMOS transistor width ratio as in (1). In this paper a 4-bit flash ADC will be design with input voltage range from 0.9 to 2.3 V, this flash ADC require a 15 different proposed TIQ comparators with different NMOS transistor to PMOS transistor width ratio.

The quantization phase has 15 outputs signal denoted by y_i, where $0 \leq i \leq 14$. This 15-output signal will be matched with 4-bit binary code in the encoding phase. The output bits of the encoding phase are denoted by B_j, where $0 \leq j \leq 3$. The encoding phase will be built from 2×1 MUX circuit. Figure 7 shows the 4-bit flash ADC circuit [29], [30].

The accuracy of the ADC can be investigated by determining the ADC signal to noise ratio (SNR), DNL and INL. Signal to noise ratio refers to the output signal power to the noise signal power ratio. The SNR can be found using (42):

$$SNR = 20\,log\left(\frac{2^N V_{LSB}}{2\sqrt{2}AVQ}\right) \tag{42}$$

where,

$$AVQ = E[V_r - V_i] \tag{43}$$

where N, V_{LSB}, AVQ, V_r, and V_i R refer to the number of the output code bit, the voltage difference between two successive code, the average quantization error, the real code transition and ideal code transition respectively. As the SNR increase the immunity of the ADC against the noise is increase. The DNL or the differential nonlinearity refers to the difference between the ideal and the actual input code width and it given by (44). The INL or the integral nonlinearity refers to the deviation the ideal output code and the actual output code and it given by (45). The DNL and INL value must be below 0.5 V_{LSB} or the ADC will give wrong output code.

$$DNL = \frac{V_i - V_{i+1}}{V_{LSB}} - 1 \quad (44)$$

$$INL = \frac{V_i - V_{min}}{V_{LSB}} \quad (45)$$

where V_i is the voltage at the i[th] code where $0 \leq i < 2^N$, N refers to the number of bit in the output code, and V_{min} refers to the minimum voltage code. Next section will show the simulation result of the 4-bit flash ADC employing proposed TIQ comparator design.

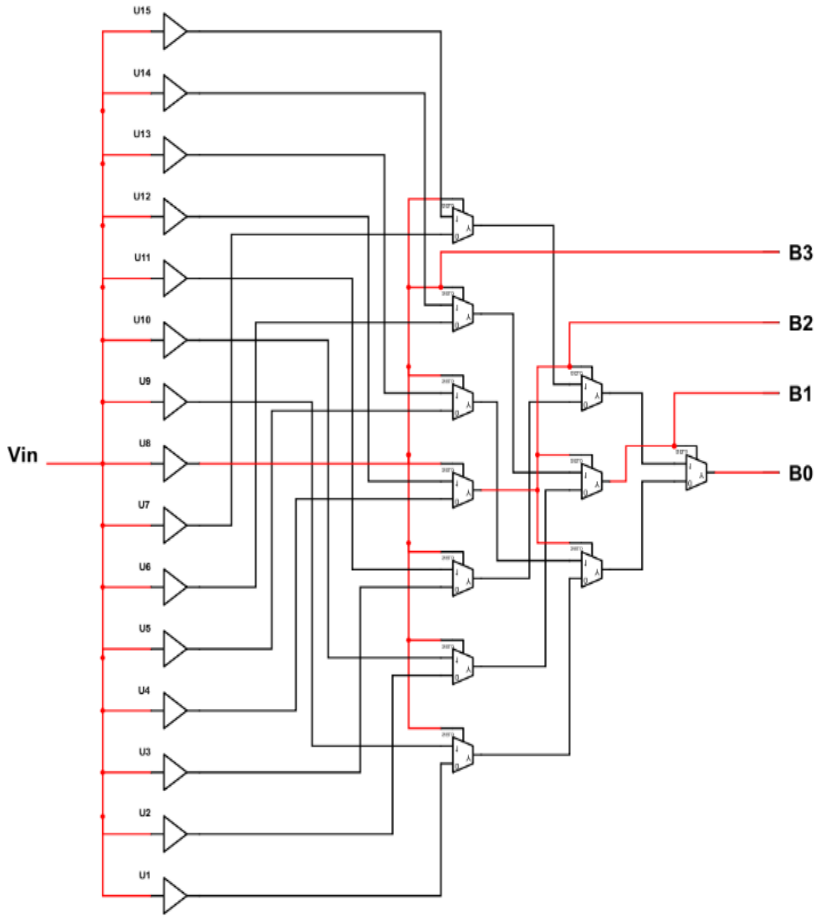


Figure 7. 4-bit flash ADC circuit

3. RESULT AND DISCUSSION

The optimum comparator design has low power dissipation, high accuracy, and high speed. These features could be investigated by mathematical analysis or by simulation. In the previous sections, the mathematical analysis of the proposed TIQ comparators was performed. In this section, the simulation result of the proposed comparators designs will be shown. 0.35 µm CMOS technology is used for simulation with 3.3 V power supply, the PMOS threshold voltage equal to 0.657 V and the NMOS threshold voltage equal to 0.4979 V.

The flash ADC design with proposed TIQ comparator decrease DNL, INL and increase SNR. The proposed TIQ comparator design enhances the accuracy of the flash ADC. Figure 8 shows the input signal and the output code of the 4-bit flash ADC that employs the proposed TIQ comparator design the input in Figure 8(a), the bit 3 in Figure 8(b), the bit 2 in Figure 8(c), the bit 1 in Figure 8(d), and bit 0 in Figure 8(e).

The performance results are shown in Figure 9. Where the maximum INL shown in Figure 9(a) is equal to 0.02 least significant bit (LSB) and the maximum DNL shown in Figure 9(b) is equal to 0.03 LSB. In Figure 10 the total power dissipation is shown.

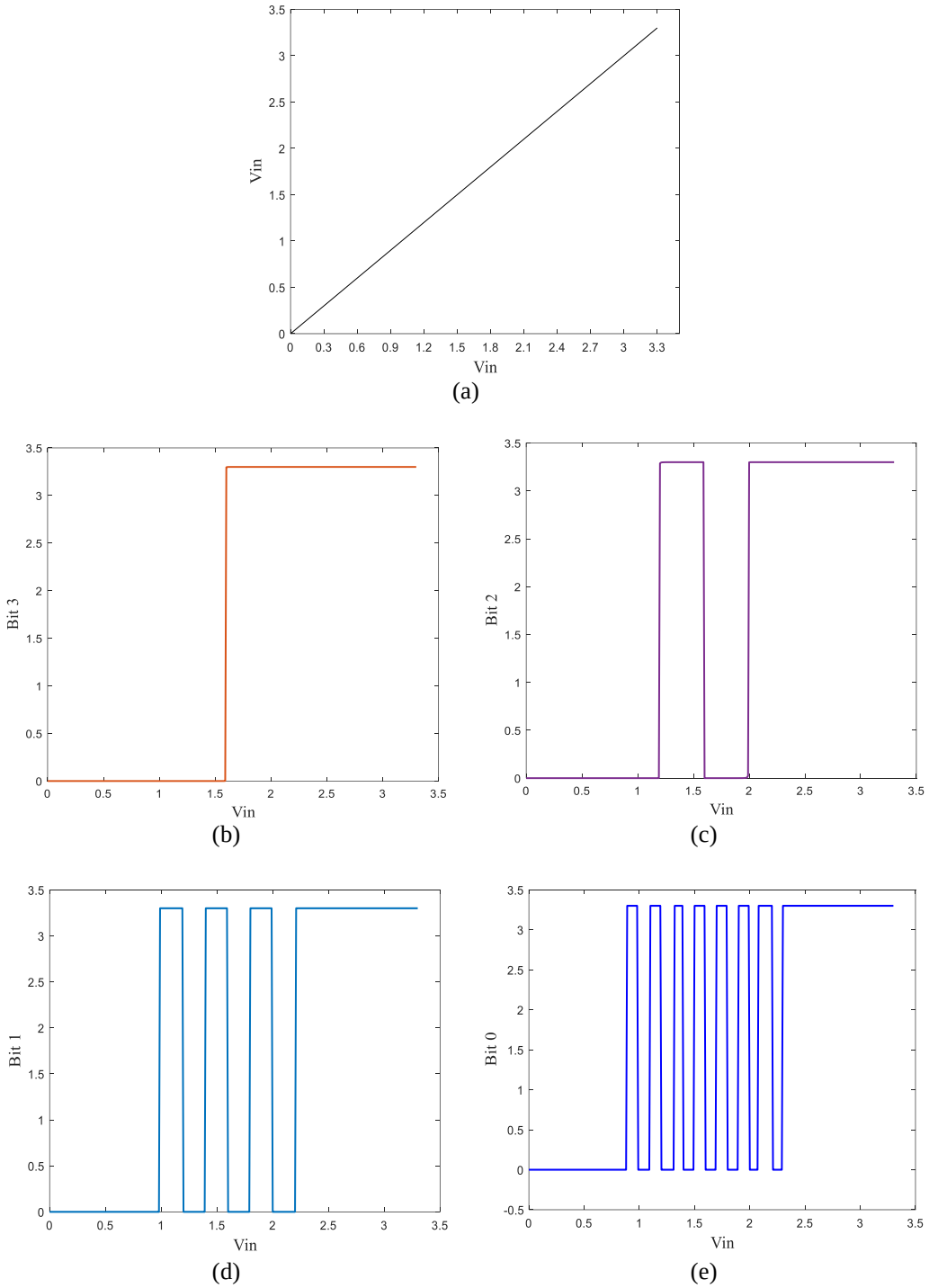


Figure 8. Analog input signal and digital output code for 4-bit flash ADC employing proposed TIQ comparator (a) input signal, (b) bit 3, (c) bit 2, (d) bit 1, and (e) bit 0

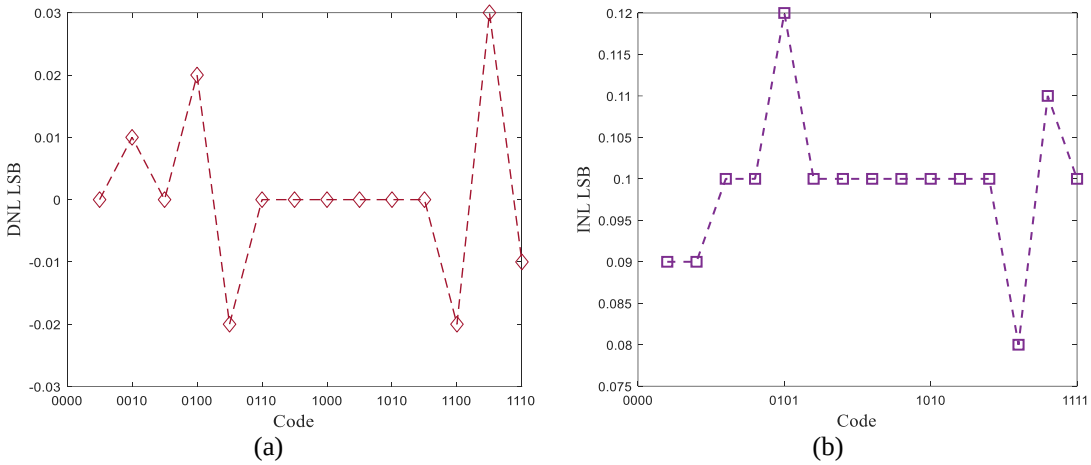


Figure 9. Accuracy of the 4-bit flash ADC employing proposed TIQ comparator (a) DNL of the ADC and (b) INL of the ADC

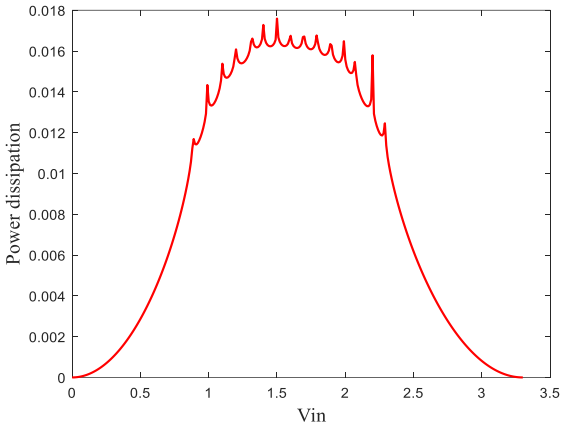


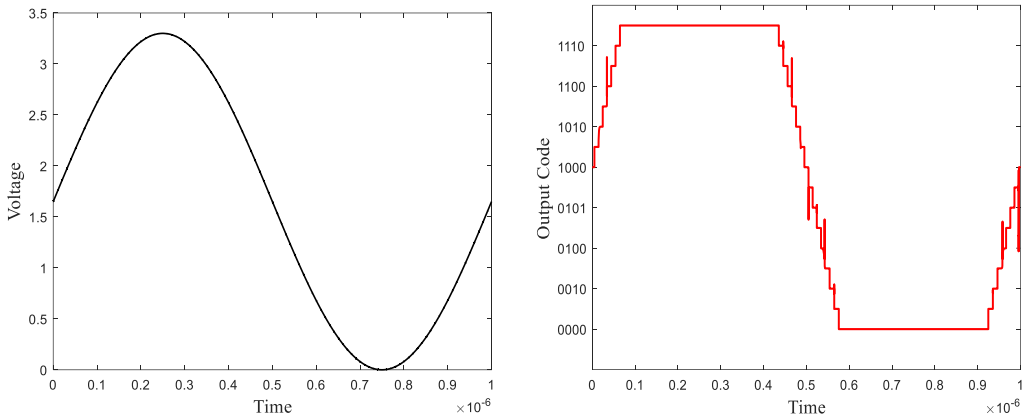
Figure 10. Power dissipation for 4-bit flash ADC employing proposed TIQ comparator

Figure 11 shows the simulation digital output code from the 4-bit flash ADC when the input signal is a sin wave with 10 MHz frequency shown in Figure 11(a), Figure 11(b) shows the output. The average power dissipation is equal to 12.8 mW, the SNR is equal to 35.6751 dB, the DNL is equal to 0.0875 LSB and the average INL is equal to 0.0453 LSB. Figure 12 shows the simulation digital output code of the flash ADC when the input shown in Figure 12(a) is a triangle signal with a 10 MHz frequency, Figure 12(b) shows the output. The average power dissipation is equal to 12.8 mW and the SNR is equal to 37.7928 dB, the DNL is equal to 0.0330 LSB and the average INL is equal to 0.0999 LSB. The layout of the TIQ comparator is shown in Figure 13.

As mentioned before, the transistors width is used to determine the reference voltage, and it affects the comparator performance. Table 1 shows the effect of the transistor size in comparator performance, where the input signals are a ramp function with 1 MHz frequency. As shown in Table 1, if the PMOS to NMOS width ratio gets closer to one the performance of the comparator enhances. In Table 2 the efficiency of the new TIQ comparator is compared with previous TIQ comparators. This comparison is made when PMOS to NMOS width ratio equals one and the input signal is a ramp function with 1 MHz speed.

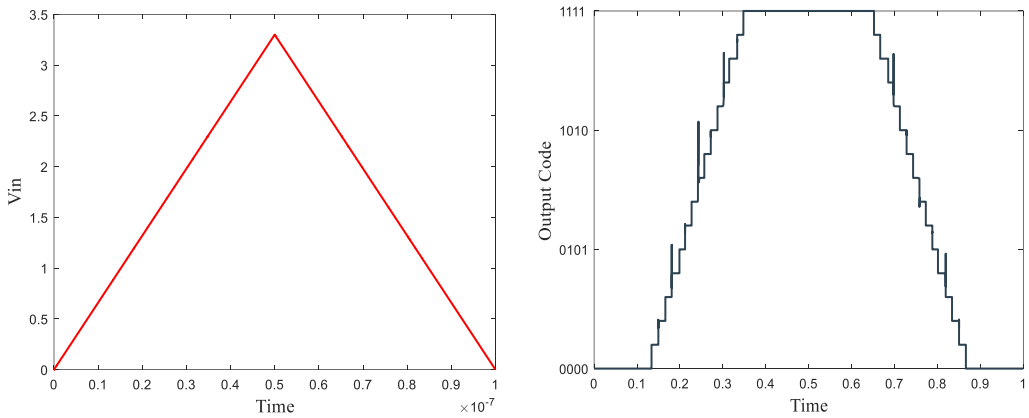
As shown in Table 2, the proposed TIQ comparator circuit reduces the power dissipation compared to the classic TIQ comparator by half. Also, this comparator reduces the offset voltage and the time delay. On the other hand the TIQ comparator design in [28] reduces the power dissipation more than the new TIQ comparator; while it has a worse accuracy and speed which affects the performance of 4-bit flash ADC. The DC sweep analysis, in Table 3, shows the performance comparison of the 4-bit flash ADC, where the 4-bit flash ADC is designed using these three comparators.

The proposed TIQ comparator reduces power consumption by 50% while maintaining gain using stacked NMOS and PMOS transistors. Applying this design to a 4-bit flash reduces DNL and INL. However, further optimization is needed to balance power efficiency and performance, address offset voltage issues, and improve robustness against transistor mismatches.



(a) (b)

Figure 11. Input and the output signal of 4-bit flash ADC employing proposed TIQ comparator with sin wave input signal (a) input signal and (b) output signal



(a) (b)

Figure 12. Input and output signal of 4-bit flash ADC employing proposed TIQ comparator with rectangle wave input signal (a) input signal and (b) output signal

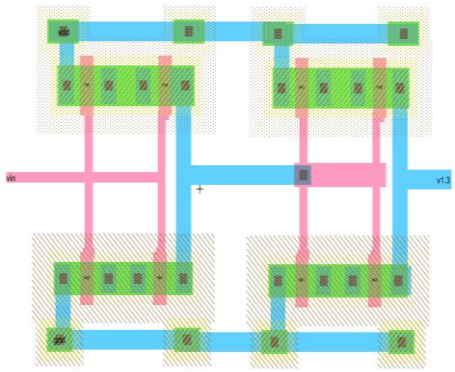


Figure 13. Layout circuit of the proposed TIQ comparator

Table 1. Effect of NMOS to PMOS width ratio in the performance of the proposed comparator

W_N/W_P	Mid-point voltage	Peak power dissipation	Time delay
7	0.9	3.77 mW	1.36 ns
5.5	1	3.48 mW	1.467 ns
4	1.1	3.174 mW	1.351 ns
3	1.2	2.897 mW	1.2 ns
2.5	1.3	2.633 mW	0.887 ns
2	1.4	1.97 mW	0.740 ns
1.5	1.5	1.696 mW	0.474 ns
1	1.6	1.9 mW	0.665 ns
0.9	1.7	1.511 mW	0.893 ns
0.7	1.8	1.729 mW	0.911 ns
0.5	1.9	1.914 mW	1.24 ns
0.4	2	2.257 mW	1.06 ns
0.3	2.1	2.362 mW	2.7 ns
0.25	2.2	2.699 mW	1.3 ns
0.2	2.3	3.471 mW	3.4 ns

Table 2. Comparison result is between the proposed TIQ comparator circuit and previous circuits

Type of the TIQ	Classic TIQ	TIQ in [21]	Proposed TIQ
Average power dissipation	0.782 mW	0.230 mW	0.392 mW
Delay time	52 ps	49.1 ps	25 ps
offset	5.15 mv	5.17 mv	5.123 mv
Gain	250	160	256

Table 3. Performance result of the4-bit flash ADC employing different TIQ comparators design

Performance issue	Classic TIQ	TIQ in [28]	Proposed TIQ
Power dissipation	16.4 mW	6.1 mW	8.3 mW
DNL	0.0186 LSB	0.0136 LSB	0.0079 LSB
INL	0.0136 LSB	0.0543 LSB	0.01 LSB
SNR	35.0431 dB	24.6997 dB	58.8093 dB

The results showing improved performance with lower power dissipation refer to several key performance metrics of the proposed TIQ comparator and its application in a 4-bit flash ADC. Power dissipation is reduced by half compared to the classic TIQ comparator. The offset voltage and time delay were decreased which improved DNL and INL. The improved DNL and INL enhances the accuracy of the 4-bit flash ADC. Potential future research directions for this work include several key areas. Firstly, further optimization of the TIQ comparator design can be pursued. Investigating methods to address offset voltage issues. Improving robustness against transistor mismatches is crucial. Additionally, exploring the scalability of this design for higher bit ADCs. Implementing the design in different CMOS technologies and assessing its performance across various applications can also be beneficial.

4. CONCLUSION

In this research, the 0.35 µm CMOS technology is used to propose new TIQ comparator design. This design modified the classic TIQ comparator by employing the sacked transistor idea. The mathematical analysis and simulation results show that the proposed TIQ comparator reduces the power dissipation of the classic TIQ comparator to half without any effect on the comparator gain. Moreover, the proposed TIQ comparator enhances the accuracy of the 4-bit flash ADC by improving the ADC SNR and reducing the ADC DNL and INL. The future implications of this work are significant for the advancement of ADC technology. The proposed TIQ comparator design demonstrates a 50% reduction in power dissipation compared to the classic TIQ comparator. This efficiency is achieved through stacked NMOS and PMOS transistors. The design is highly suitable for modern communication systems that require high speed and low power consumption. Additionally, the DNL and INL were improved. The overall performance and accuracy of the ADC is This work paves the way for further research into optimizing power efficiency and performance in ADC designs

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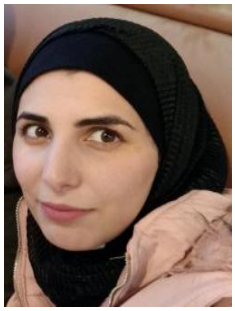

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